TOWARDS AN INDUSTRIAL FABRICATION PROCESS FOR ELECTROWETTING CHIP USING STANDARD MEMS TECHNOLOGY

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ABSTRACT

Reliability of Electrowetting on Dielectric (EWOD) microsystems partly relies on the hydrophobic layer. A process for depositing a SIOC (organosiloxane molecule) material fitting all the needs was firstly established on a laboratory equipment, then further transferred on an industrial machine devoted to microelectronics fabrication. For packaging purposes, this layer has to be patterned on the EWOD chip. A lift-off process was investigated and showed promising results. Simplifying the packaging steps is essential for a rapid cycle fabrication to test. In this way, an experimental setup was developed in order to directly make electrical contact on the EWOD chip.

KEYWORDS: Electrowetting, SIOC layer, packaging

INTRODUCTION

In a few years, EWOD has become a major tool for lab-on-chip applications in research laboratories [1,2,3,4,5]. Multiple teams have worked on a cheap way to produce EWOD microsystems [6]. Silicon technology has been extensively used for microsystems fabrication, but barely studied for an industrial fabrication process for EWOD chip. In this work, choices of materials, processes and experimental setup were driven by trying to obtain fabrication processes compatible with actual microelectronics/MEMS industrial cleanrooms.

RESULTS AND DISCUSSION

One of the key materials allowing EWOD behavior is the final hydrophobic layer, which must show particular wetting properties: elevated static contact angle and low contact angle hysteresis. Teflon® is widely used and commonly deposited by spin-coating and solvent evaporation. Moreover, patterning using classical microfabrication processes can be difficult. Based on materials originally developed for microelectronics, an original SIOC material was fabricated, using a Plasma Enhanced Chemical Vapor Deposition (PECVD) process with the OctaMethylTetraSilOxane as precursor [7].

Table 1 – Comparison of SIOC properties and main process parameters between a laboratory equipment and the Precision 5000 machine

	Contact Angle (°)	Hystersis (°)	Deposition rate (nm/min)	Temperature (°C)	Uniformity (%)
Lab. Equipment	105	5	50	57	4
Precision 5000	105	5	70	96	7

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Its elevated hydrophobicity (110°) and very low hysteresis (10°) makes it a perfect hydrophobic layer for EWOD. This deposition process was firstly developed on a laboratory equipment and then transferred on a Precision 5000 machine from Applied Material Company on 200mm silicon wafers, as a last step for EWOD chip fabrication (Table 1). This SIOC is currently used for both EWOD chip and cover plate, replacing the previous Teflon layer. Moreover, aiming at industrial process, a patterning process was developed using standard microfabrication tools, allowing SIOC removal both on top of spacer walls and electrical pads (Figure 1).

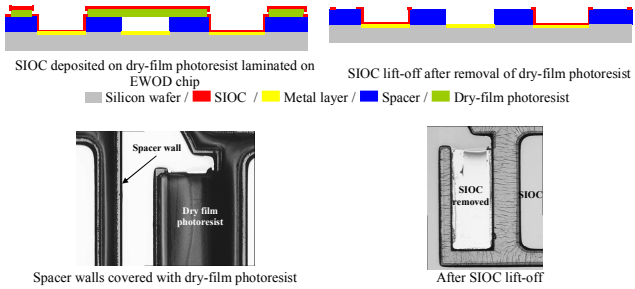

Figure 1 – Principle of SIOC lift-off and associated pictures

In conclusion, the whole fabrication process (from silicon wafer to final SIOC layer) was realized in MEMS cleanroom with industrial machines at 200mm wafer scale.

A specific experimental setup was designed and fabricated with an objective of making rapid and reproducible electrical connections, without using classical Printed Circuit Board technology involving multiple steps such as chip gluing or wire bonding (Figure 2).

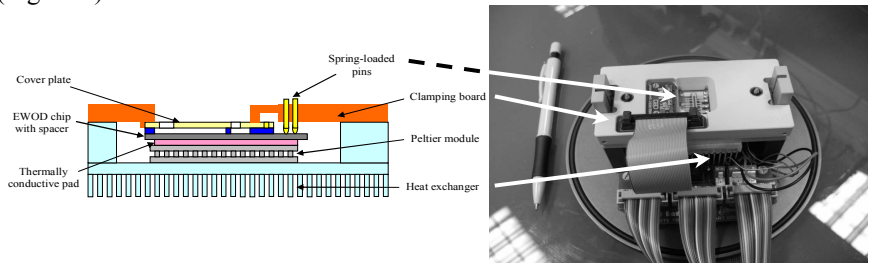

Figure 2 – Schematic side-view and picture of the experimental setup for simultaneous clamping of the cover plate and electrical connections with EWOD chip

The EWOD chip is manually placed on a heat regulation module (comprising a Peltier module and a heat exchanger with fans) with a thermally conductive pad, then the cover plate is placed on top of the chip and a final board is clamped on top of the cover plate. This board comprises spring-loaded pins for electrical connections. Alignment of chip and cover plate is done with mechanical references. Using this

experimental setup, both packaging time (between final steps in cleanroom to effective test) and cost are drastically reduced.

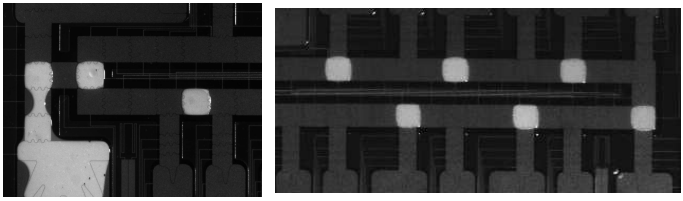

Figure 3 – Droplets created and moved using EWOD chip fabricated on 200mm wafers using standard MEMS processes

The surface quality obtained in this way permits non-stop EWOD at 46Vrms over 48 hours without apparent degradation of materials on EWOD chip. Moreover, thin film processes (such as PECVD) allow exploration of new experimental range, particularly concerning thicknesses. As an example, a 200nm SIOC layer was deposited on 600nm silicon nitride. This dielectric bi-layer allows functional EWOD (droplet formation, movement and splitting) at 19Vrms (Figure 3).

CONCLUSIONS

To conclude, these results pave the way toward industrial fabrication of EWOD chip for biological applications, such as real-time PCR. The experimental setup was specifically developed for an easy and intuitive use by biologist. Future work will be devoted to packaging, aiming at full wafer process for assembly of both fully functional EWOD and cover wafers, using SIOC localization.

REFERENCES

[1] Electrowetting-based actuation of droplets for integrated microfluidics, *Pollack et al.*, Lab on a Chip, 2, 96-101, 2002

[2] Creating, transporting, cutting, and merging liquid droplets by electrowetting-based actuation for digital microfluidic circuits, *Cho SK et al.*, Journal of Microelectromechanical Systems 12, 70-80, 2003

[3] Yi-Hsien Chang et al., Integrated polymerase chain reaction chips utilizing digital microfluidics, Biomed. Microdevices, 8, 215–225, 2006

[4] Digital microfluidics: is a true lab-on-a-chip possible? *Fair RB.*, Microfluidics and Nanofluidics 3, 245-81, 2007

[5] Digital microfluidic design and optimization of classic and new fluidic functions for lab on a chip systems, *Fouillet Y. et al.*, Microfluidics and Nanofluidics 4, 159-65, 2008

[6] Direct-referencing two-dimensional-array digital microfluidics using multilayer printed circuit board, *J.Giong and C.J. Kim*, Journal of Microelectromechanical Systems 17 (2), 257-264, 2008

[7] SIOC as a superhydrophobic layer for electrowetting on dielectric applications, *J.Thery et al.*, 2007, microTAS 2007, Paris, France