Supporting Information

Connecting wire-based solar cells without any transparent conducting electrode.

*Toan Le Duc, Eric Moyen, Mihai Robert Zamfir, Young Woo Kim, Jemee Joe, Young Hee Lee, Didier Pribat**

Growth of p-i-n Si wires

300 nm-thick aluminum (Al) thin films were evaporated onto 1.5 x 1.5 cm^2 quartz substrates. The quartz plates were first etched during 3 minutes in buffered HF, carefully rinsed and blown dry under a N_2 flow just before being loaded in the evaporator. This Al film will serve both as an electrode and as a catalyst for subsequent Si wire growth. Al, together with other "CMOS-friendly" catalysts[S1,S2] has been studied for the vapor-liquid-solid (VLS) or vapor-solid-solid (VSS) growth of Si wires over the past few years.[S3–S7] One of the peculiarities of the Al catalyst (a column III element) is that there is no need of dopant gas in the growth atmosphere (such as B_2H_6 or trimethyl boron), since it directly produces p-doped Si wires due to the incorporation of Al during growth.[S4,S7]

In the present work, we have use a plasma-enhanced chemical vapor deposition (PECVD) process to grow the Si wires from the Al thin films. The Al-coated quartz substrates were loaded on the bottom electrode (sample-holder/heater) of the PECVD reactor which was pumped down to ~ 10^{-6} torr. Once the base pressure reached, the temperature of the sample-holder was set to 550°C and H_2 gas was introduced into the chamber, at a flow rate of 250 sccm while the pressure was stabilized and maintained at 1 torr. Then, the plasma was ignited and sustained for the next 20 min, with a 20 W applied power. During this step, the H_2–based plasma generates atomic hydrogen, which helps cleaning the Al surface and reducing the native Al_2O_3. After 20 min, as the temperature had stabilized at 550°C, SiH_4 was introduced into the chamber at a 20 sccm flow rate, while the H_2 flow and the plasma power were kept unchanged; growth of the Si wires started to proceed. Since the growth temperature is below the Al-Si eutectic temperature (~ 577 °C), growth probably proceeds via a VSS mechanism. In the above conditions, the growth rate is approximately 200 nm/min (see figure S1 for some SEM pictures of those NWs). After the growth of the core Si NWs, the SiH_4 as well as the plasma power are stopped and the reactor temperature is decreased to 200 °C under H_2 flow. Once the temperature stabilized, SiH_4 is re-introduced in the reactor (20 sccm) and the plasma ignited again and set to 20W; the total pressure is fixed at 300 mTorr. In those conditions, a first shell of intrinsic, or rather non-intentionally doped (NID) hydrogenated amorphous Si (a-Si:H) is deposited all around the p-type Si wire cores. Once the desired thickness reached, (typically 150 nm, see fig. S2) all parameters were kept unchanged and PH_3 (0.05% diluted in H_2) was flown into the reactor (40 sccm), in order to realize a second n^+-doped shell layer, typically 50 nm-thick (fig. S1). Using the ImageJ software, we evaluate the area covered by p-i-n nanowires to ~ 97% of the footprint of the Al electrodes.

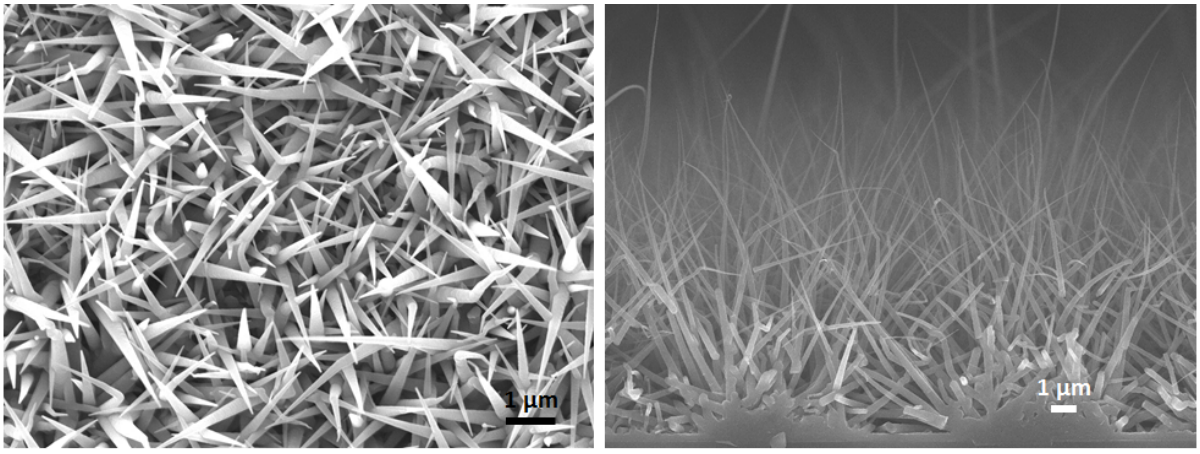

Figure S1: Scanning electron microscope pictures of the core p-Si NWs after growth.

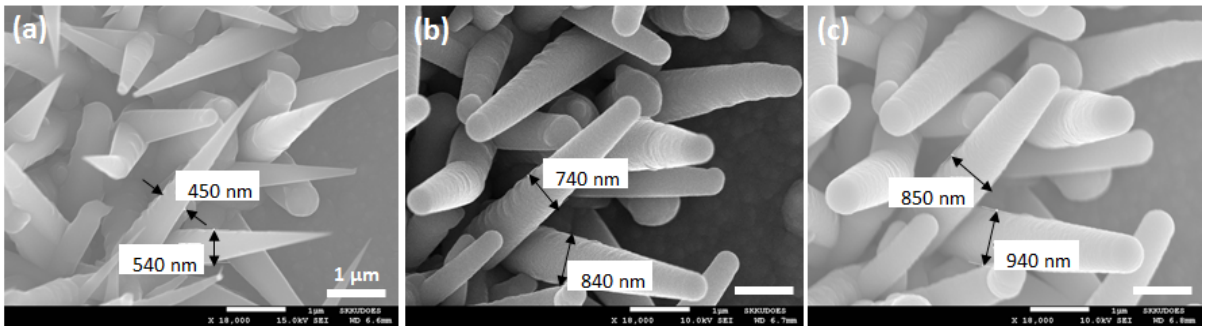

Figure S2: Determination of the thickness of the shell layers. (a): The core Al-doped Si wires. (b): After deposition of the a-Si:H shell. (c): After deposition of the second n^+ a-Si:H shell. All the scanning electron microscope (SEM) pictures are taken at the same place. The bar scale is 1 µm on all pictures.

Characterization of the p-type cores

After growth, the core Si NWs were separated from the substrate by sonication in ethanol. Some drops of the thus-obtained alcoholic suspension were then spread on highly-doped oxidized Si substrates (SiO_2 thickness = 100 nm) for electrical characterization. After drying, the positions of the Si NWs were recorded under an optical microscope and a lift-off process was used to deposit 150nm Ni + 50nm Au electrodes. Those electrodes were then annealed in a high vacuum environment at 300 °C, during 20 minutes. Before electrode deposition, the exposed parts of the Si NWs were etched in HF (1%) during 20s, in order to remove the native oxide. Figure S3 shows optical and SEM pictures of a device after electrode deposition and annealing.

Figure S4 shows various transistor characteristics of the Si NW shown on fig. S3, when the highly doped Si substrate is used as a back gate. The drain current (I_{DS}) is clearly seen to decrease as the gate voltage (V_{GS}) goes from negative to positive values, which is indicative of a p-type behavior (fig. S4-a). The output characteristics of the transistor are shown on fig. S4-b. The gate influence is very limited (the transistor cannot be turned off) and saturation is not reached, which indicates highly doped, metal-like wires.

We have evaluated the hole mobility using the classical formula: $\mu = g_m \frac{L^2}{V_{DS}\, C_{tr}}$, where g_m is the transconductance of the device ($g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$), L is the channel length of the transistor (here, 3 µm), V_{DS} is the drain voltage (0.2 V) and C_{tr} is the gate capacitance of the transistor.

Because we have a nanowire (which we assimilate to a cylinder) lying on a plane, the gate capacitance can be approximated by:

$C_{tr} = \frac{2\pi L \varepsilon_0 \varepsilon_r}{\mathrm{Ln}(4t_{ox}/d)}$, where ε_0 is the vacuum permittivity, ε_r is the dielectric constant of the gate insulator (here, we took $\varepsilon_r \approx 2.5$, *i.e.*, an average value between air and SiO_2), t_{ox} is the thickness of the gate insulator and d is the nanowire diameter. If we take an average value of d = 190 nm ($\{150 + 230\}/2$, see fig. S3), we get $C_{tr} \approx 5.60 \times 10^{-16}$ F.

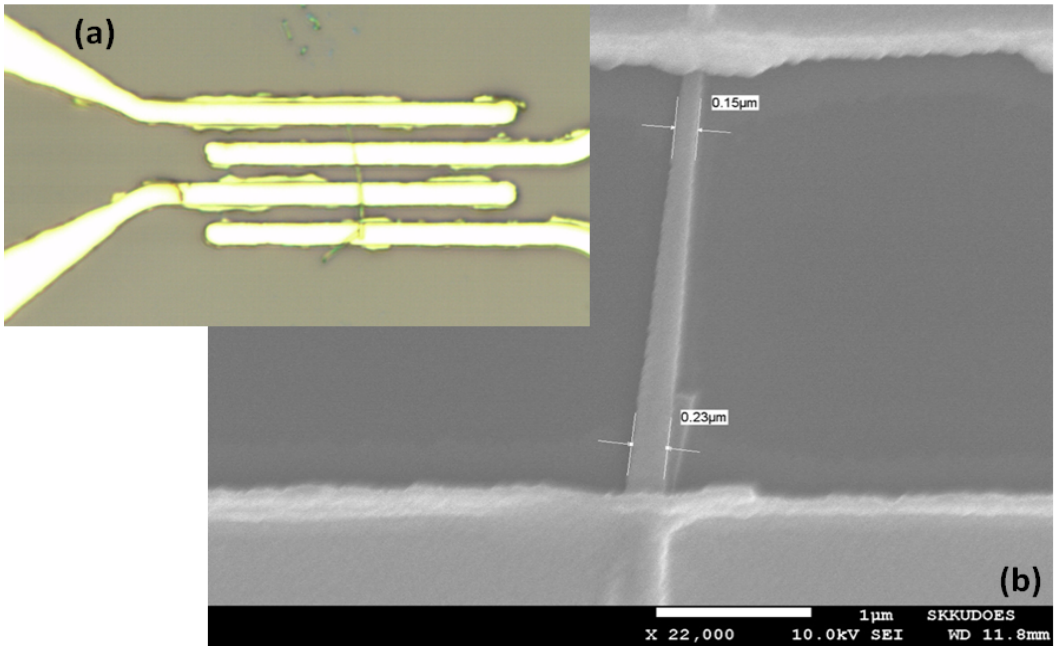

Figure S3: a typical Si NW ready for electrical measurements. (a): optical micrograph of the device (100X magnification). (b): SEM picture of a portion of the Si wire between two of the four electrodes. The electrode separation is 3µm. The bar scale on the picture is 1 µm. Because the Si NWs are tapered after growth, the diameter varies between ~ 150 and 230 nm.

The g_m value can be extracted from the slope of fig. S4-a; we find $g_m \approx \Delta I_{DS}/\Delta V_{GS} \approx 3.64 \times 10^{-8}$ A/V. With the above values, we find a hole mobility of ~ 29 cm^2/Vs, for d = 190 nm. Now, the resistance of the wire can be evaluated in the voltage interval between – 50 mV and + 50 mV where the output characteristic for V_{GS} = 0 is linear. We find R ≈ 3.75 kΩ. Still assuming a 190 nm average diameter wire, this yields ρ ≈ 282 Ω.cm. Hence, the carrier concentration is ~ $6 \times 10^{19}/cm^3$.

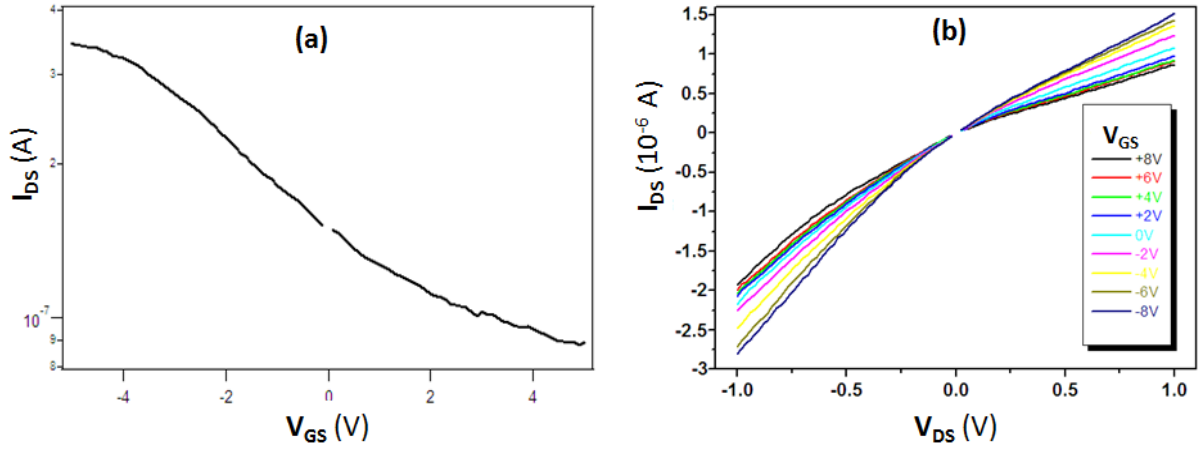

Figure S4: Electrical characterizations of the core Si NWs. (a): Transfer characteristic, with a V_{DS} voltage of 0.2 V. (b): Output characteristics.

We have measured the characteristics of 4 different Si wires and found carrier concentrations between ~ 4 and 6.7 x 10^{19}/cm^3.

Growth of the $NiSi_x$ nanowires

In order to minimize the degradation of the a-Si:H shells (whether doped or not), the $NiSi_x$ nanowires were grown at 380 °C in the same PECVD reactor, but without igniting the plasma. The growth process is therefore similar to a classical CVD one, but with a hot plate type furnace. From previous studies, it is well known that, in certain conditions, $NiSi_x$ NWs grow spontaneously when SiH_4 is flowing on top of a Ni film.[S8] Here, we used 250 nm-thick Ni films. The Ni-covered quartz samples were loaded in the PECVD reactor and once the temperature stabilized at 380 °C, the pressure was adjusted to 1 Torr, the H_2 flow was set to 250 sccm and the SiH_4 one to 2 sccm. The $NiSi_x$ NW growth time was typically 30min.

Structural characterization of the $NiSi_x$ nanowires

After growth, the $NiSi_x$ NWs were sonicated in ethanol and some drops of the alcoholic solution were deposited on a carbon coated copper grid for further TEM observations. High resolution TEM images and their fast Fourier transforms show that the wires are monocrystalline Ni_3Si_2 (Fig. S5).

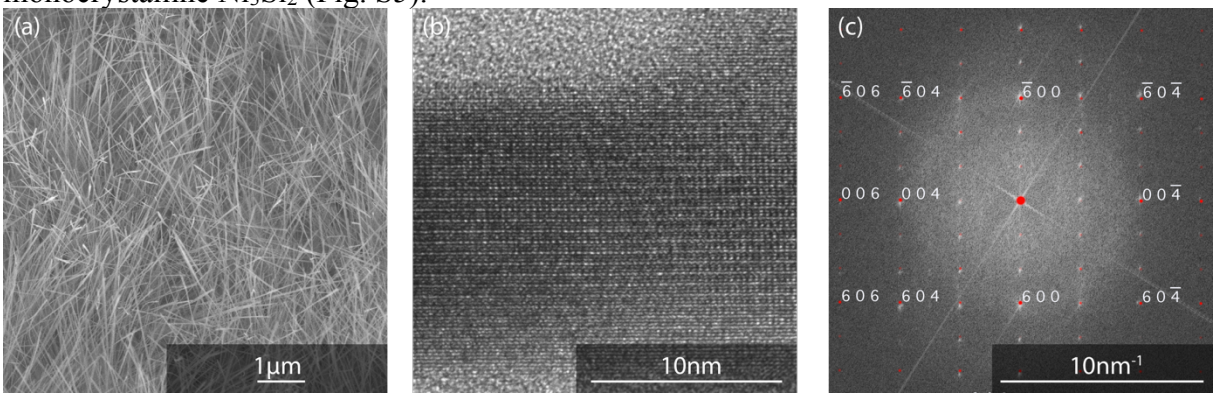

Figure S5: Structural characterizations of the $NiSi_x$ NWs. (a): SEM top view of the wires. (b): High resolution TEM image of a wire. (c): Fast Fourier Transform of (b). The simulated electron diffraction pattern of the Ni_3Si_2 compound (in red) fits the observations.

Electrical characterizations of the $NiSi_x$ nanowires

After growth, the $NiSi_x$ NWs were sonicated in ethanol and some drops of the alcoholic solution were deposited on an oxidized silicon wafer for electrical measurements. Contacts were taken in the same way as for the Si wires, except that we used e-beam lithography to define the electrodes, through again a lift-off process. A Cr-Au metallization was used. Fig. S6 shows a SEM picture of a device ready for measurements. We have measured 3 nanowires and the typical resistivity we find is ~ 80 µΩ.cm, in agreement with our former results.[S9]

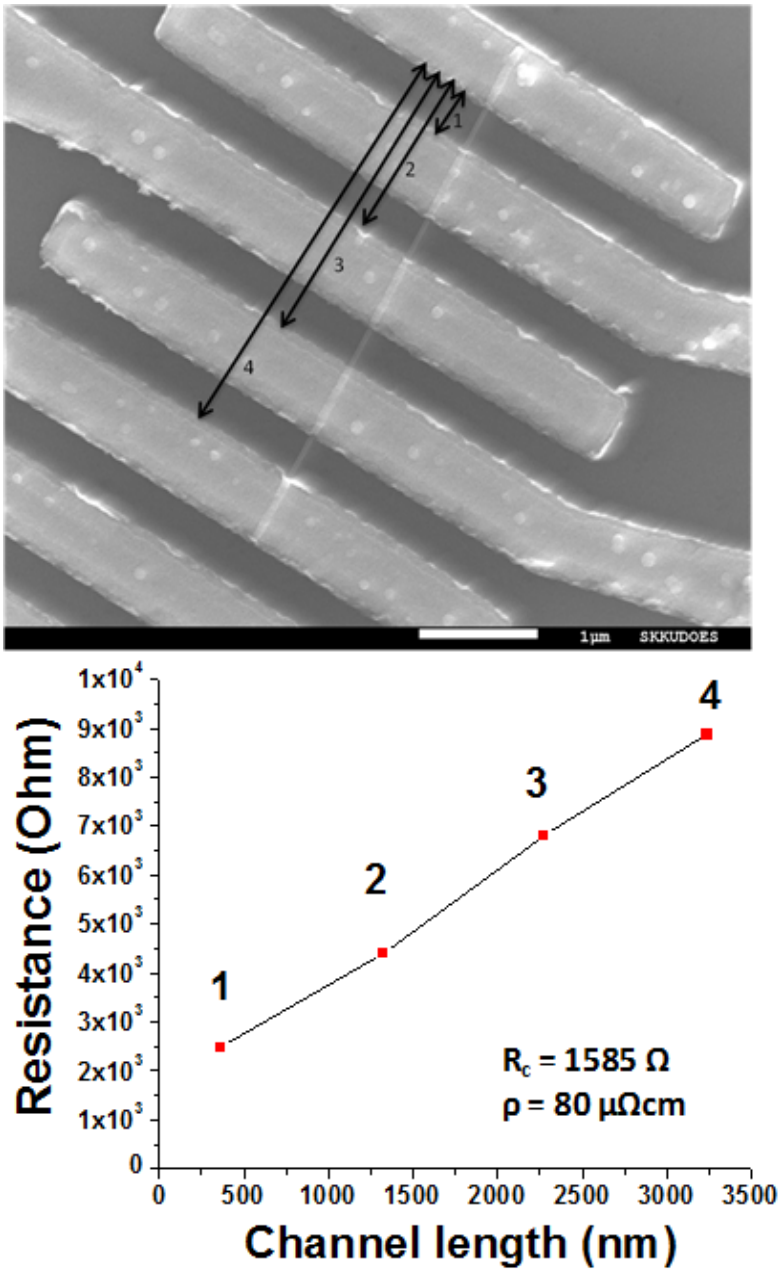

Figure S6: Electrical characterization of the $NiSi_x$ NWs. The top SEM picture shows a nanowire connected to 5 different electrodes. The bottom panel is a plot of the measured resistance between the different electrodes of the top picture. The resistivity value of ≈ 80 μΩ.cm corresponds to the Ni_3Si_2 compound.[S10]

SEM observations of the density of connections between $NiSi_x$ NWs and Si p-i-n wires.

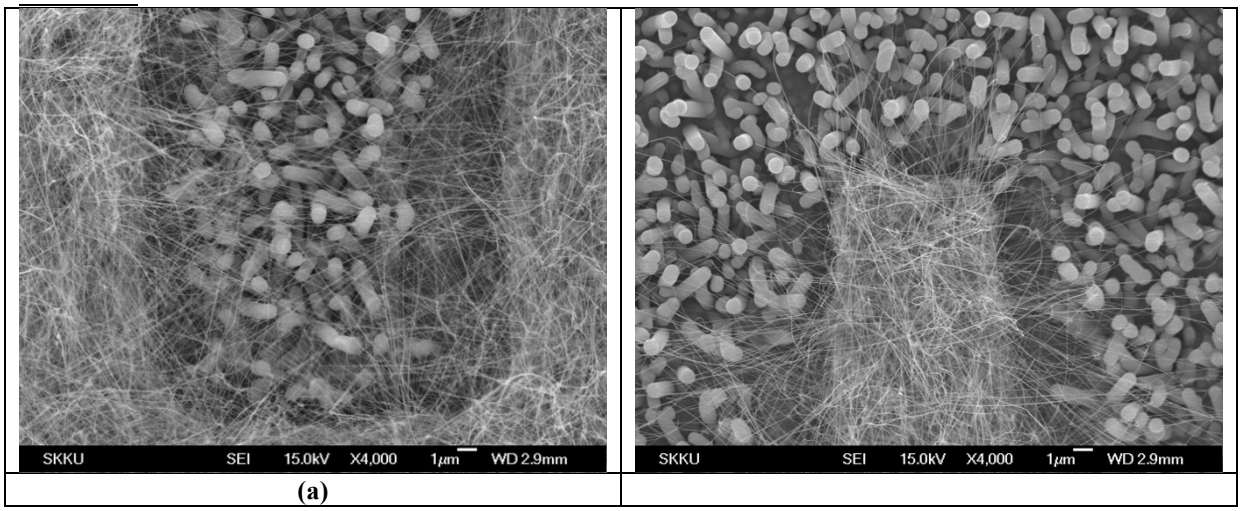

Figure S7: Various SEM pictures taken at different places of the interdigitated structure. Note the high density of connections between the $NiSi_x$ NWs and the p-i-n Si wires. (a): bottom part of one Al finger. (b): top part of a Ni finger.

Calculation of the active area of the solar cell and raw *I-V* characteristics.

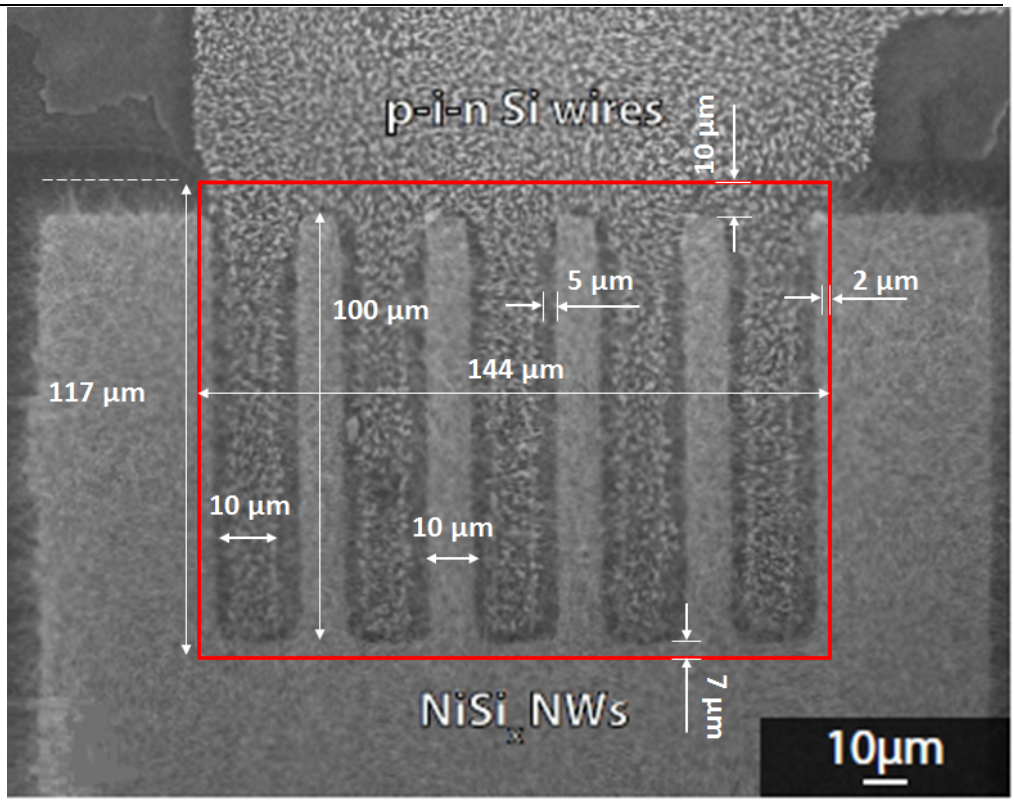

Figure S8: The various dimensions that have been used for the calculation of the active area of the solar cell.

For the calculation of the active area of the device, we have taken the surface area comprising (i) 5 Al fingers (50 μm wide), (ii) 4 Ni fingers (40 μm wide) and (iii) 10 separation intervals (each 5 μm wide). Moreover, we have taken an extra width of 2 μm on each side (corresponding to $NiSi_x$ NWs), which we judge sufficient for establishing good connections. On the other hand, each finger is 100 μm long and we have taken 10 μm extra on top (5 μm separation + 5 μm penetration of the $NiSi_x$ NWs inside the Si wire area). Figure

S8 summarizes the various dimensions of the device. So, altogether, the active area comes to 144 µm x 117 µm = 16 848 µm^2. Now, the short circuit current (I_{SC}) that we measure for the device of fig. S8 under 1 sun illumination is 1.5 µA (see fig. S9), so that we get: J_{SC} = 8.9 mA/cm^2.

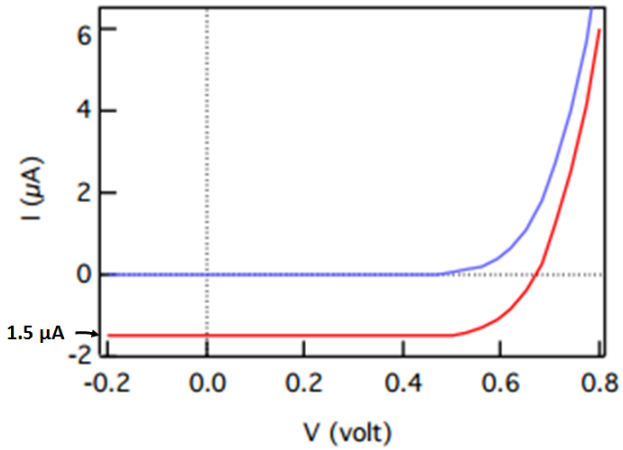

Figure S9: Raw I-V characteristic for the interdigitated device of fig. S8. The short circuit current is 1.5 µA.

Parameters used for the band diagram contruction

Table S1: The various parameters used for the construction of the band diagram of the device.

	Electron affinity (eV)	Forbidden gap (eV)	Work function (eV)
a-Si:H	3.95[a]	1.7[b]	
c-Si	4.05[a]	1.1[b]	
Ni_3Si_2			4.45[c]

[a] values from ref. S11; [b] Rounded values from ref. S11; [c] Reference S12.

Determination of the series resistance of the device [S13]

$$I = I_0\left[e^{\left(\frac{q(V-RI)}{nkT}\right)} - 1\right] \approx I_0 e^{\left(\frac{q(V-RI)}{nkT}\right)} \Rightarrow LnI = LnI_0 + \frac{V-RI}{nV_T} = LnI_0 + \frac{V - R\times e^{LnI}}{nV_T}$$

$$\Rightarrow \quad V = R\times e^{LnI} + nV_T LnI - nV_T LnI_0 \Rightarrow \frac{\partial V}{\partial LnI} = R\times e^{LnI} + nV_T = RI + nV_T$$

References

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