Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Magnetotransport across Metal-Graphene Hybrid Interface and its Modulation by Gate Voltage

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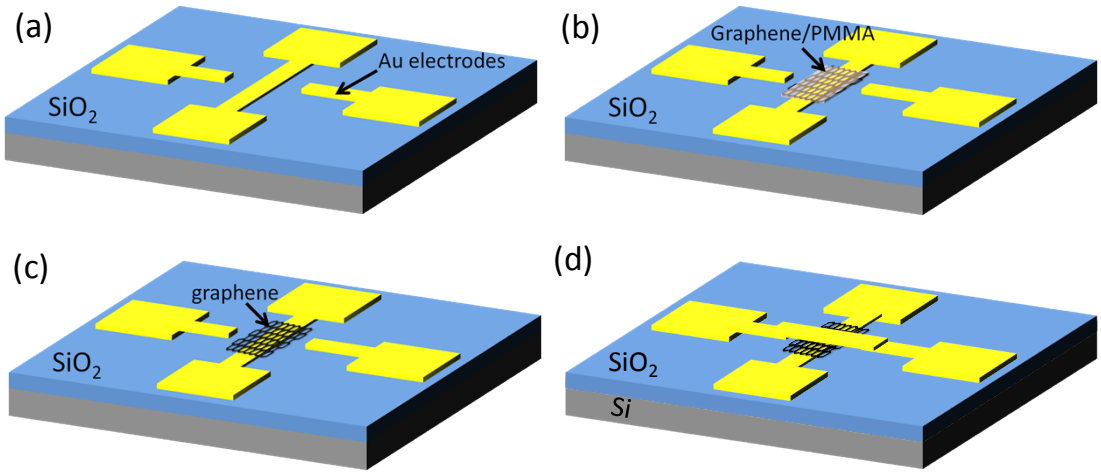

Figure S1. Sketches of fabricating the Au/graphene/Au device and TEM investigation of the interfacial region. (a) The bottom electrode was fabricated using EBL, followed by metal deposition of Ti/Au (5/25 nm) and lift-off process. (b) A monolayer graphene/PMMA microstamp was transferred onto the electrode strip. (c) Then the PMMA was removed by acetone and the PMMA residues were reduced further by annealing in a tube furnace at 350°C for 3 hours in the gas flow of 20 sccm H_2 and 100 sccm Ar. (d) A gold strip was transferred onto the graphene as a top electrode. The fabrications of the Au strips are as following. Au strips were prefabricated on SiO_2/Si substrate. A PMMA thin layer was then spin-coated on the substrate. The PMMA microstamps comprising Au strips were patterned via EBL. The SiO_2 was dissolved by HF solution and the Au/PMMA film floated on the solution surface. The Au/PMMA film was then cleaned using deionized water. The Au/PMMA film was then fished out by a copper mesh and can be transferred using the similar method as graphene.

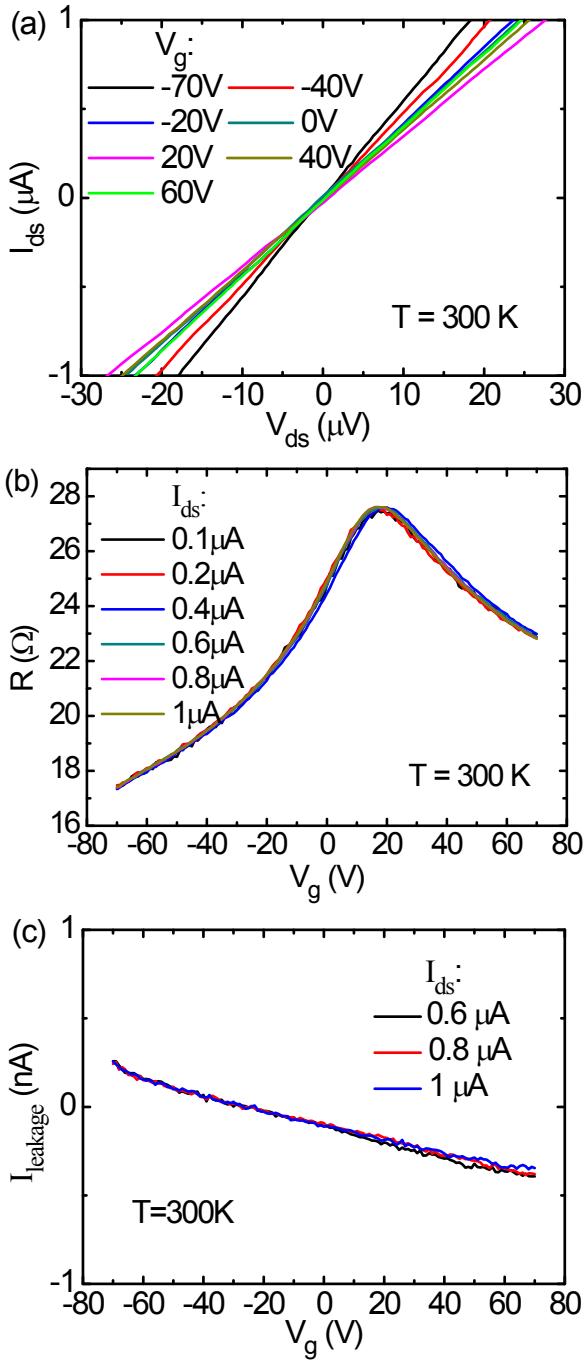

Figure S2. The basic behavior of one typical Au/monolayer Graphene/Au junction at 300 K. (a) Linear I_{ds}-V_{ds} curves under different gate voltages. (b) The transfer curves under different drain-source current I_{ds}. (c) The gate leakage current by sweeping the gate voltage under different I_{ds}.

Figure S3. The fabrication and properties of the comparison structure with graphene on SiO_2 substrate and uncovered by the top electrode. (a) The bottom electrode with a width of 10 μm was prepared on SiO_2 substrate. The graphene microstamp (70 μm × 30 μm) lies partly on the bottom Au electrode and partly on the SiO_2 substrate. An insulating Al_2O_3 layer with a window in the center was then deposited to define the graphene area on the Au bottom electrode that will contact directly with the top electrode. (b) The optical image of the device before fabricating the top electrode. (c) The resistance of the device as a function of gate voltage under 0 T and 14 T. (d) The magnetoresistance at 300 K.

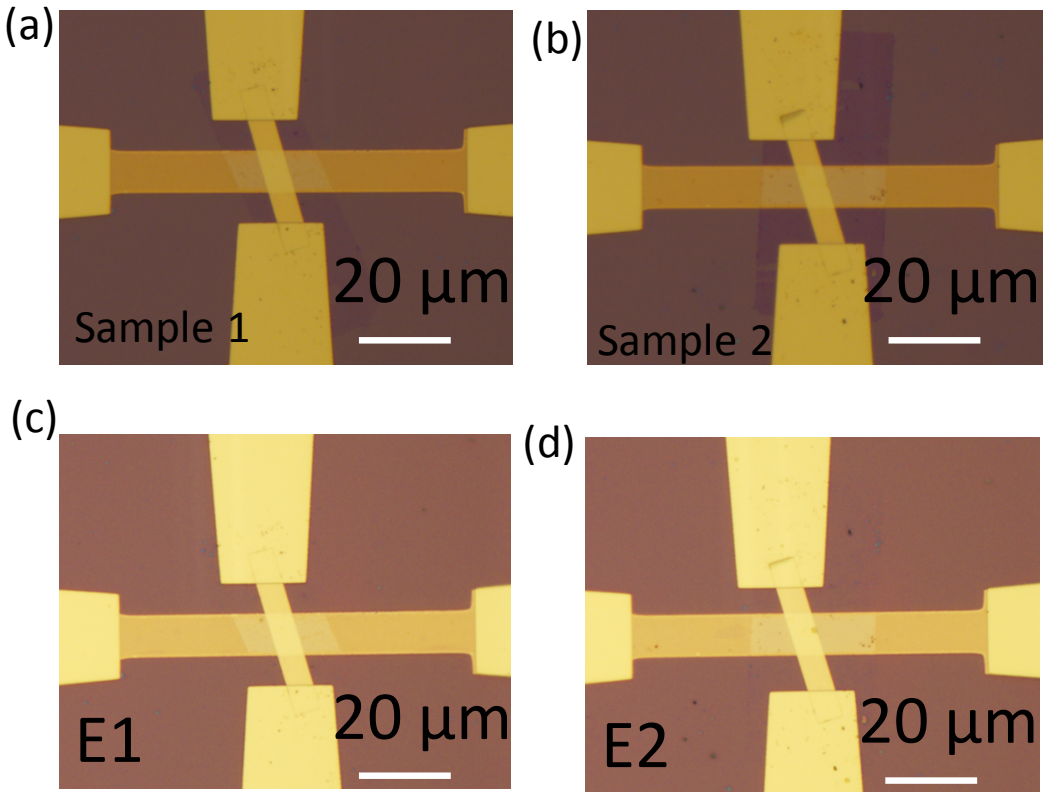

Figure S4. Optical images of samples before and after etching the graphene portion not covered by top electrode. (a, c) The Au/monolayer graphene/Au device before (a) and after (c) etching. (b, d) The Au/two-layer graphene/Au device before (b) and after (d) etching.

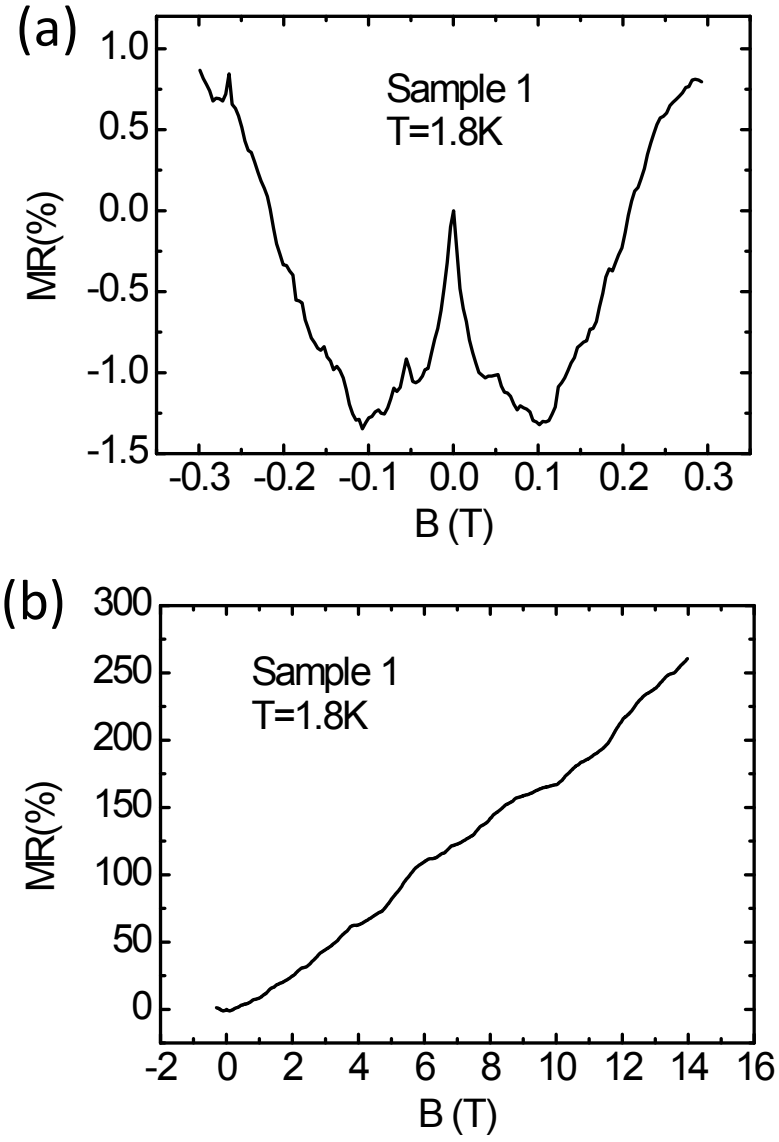

Figure S5. Magnetoresistance of **Sample 1** at 1.8 K with $V_g = 0$ V.