Supporting Information

Apparent pH Sensitivity of Solution-Gated Graphene Transistors

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Graphene Growth and Device Fabrication. Graphene film was grown on a Cu foil by chemical vapour deposition in a double walled quartz tube furnace according to a recipe described previously.[1] Briefly, a 25 μm-thick Cu foil (Alfa Aesar) was first inserted into a homemade double-walled quartz tube furnace. After degassing, temperature of the furnace was raised to 1000 °C with H_2 flow (10 sccm) and the temperature was maintained for 30 min. While holding the temperature for another 30 min, a mixture of CH_4 (15 sccm) and H_2 (10 sccm) was subsequently introduced into the tube. Finally, the delivery of CH_4 flow was cut off and the furnace was cooled down to room temperature quickly, which result in formation of monolayer graphene on both sides of the Cu foil. One side of the as-prepared graphene/Cu foil was then spin-coated with poly(methyl methacrylate) (PMMA) dispersed in chlorobenzene and the resulting film was heated at 70°C for 10 min for curing. Subsequently, the graphene monolayer grown on the other side of the foil was removed using O_2 plasma for 2 sec. Following, the remaining Cu layer was etched away using an aqueous solution of 0.1 M ammonium persulphate ($(NH_4)_2S_2O_8$). The resulting PMMA/graphene film was transferred onto Si/SiO_2 wafers which were pre-patterned with source/drain and coplanar gate electrodes (Cr/Au). After, rinsing away the top PMMA layer using acetone and deionized water, the active graphene channel was defined by by selective etching processes with the aid of photolithography. Subsequently, photoresist (PR) was deposited onto the wafer and patterned to from a photoresist bank (PR bank). Finally, series of pH buffer solutions were drop-casted onto the graphene channel through the exposed area of the PR bank.[1] Note that the insertion of the PR bank was intended to reduce undesired electrochemical reactions between the metal contacts and the pH buffer solution. The electrical measurements were carried out under dark, atmospheric conditions using a MST 5500B probestation connected with a Keithley 4200.

Application of ODTS Self-Assembled Monolayer. *n*-Octadecyltrimethoxysilane (ODTS) self-assembled monolayer was applied onto the Si/SiO_2 substrates with electrodes through the following processes. First, 40 μl of ODTS solution (Gelest) was added into 10 ml of trichloroethylene (TCE). The diluted ODTS solution was spin coated (3000 rpm for 30 s) onto the Si/SiO_2 substrates that were pre-exposed to UV-ozone for 1 hr. The substrate was vapor-annealed under ammonia condition for 12 hr inside a desiccator and then annealed on a hot plate for 20 min at 120°C. Finally, the substrates with ODTS layers were sonicated in toluene and rinsed using toluene.

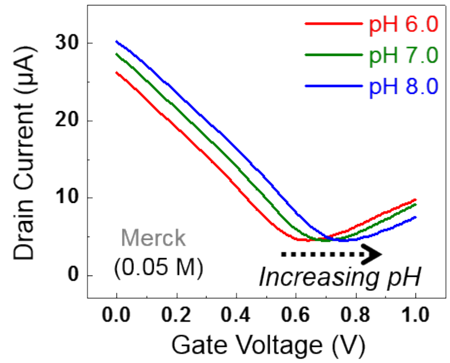

Fig. S1. Transfer characteristics of a graphene transistor (V_D = 0.05 V) operated with a reference pH buffer series (pH = 6-8) purchased from Merck.

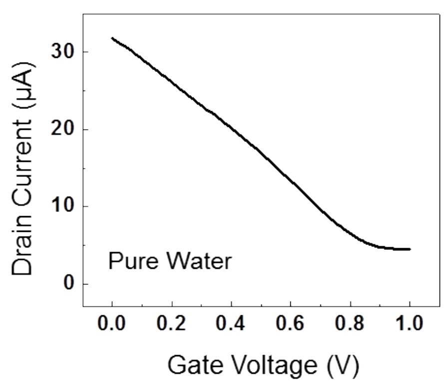

Fig. S2. A transfer characteristic of a graphene transistor (V_D = 0.05 V) operated with pure water.

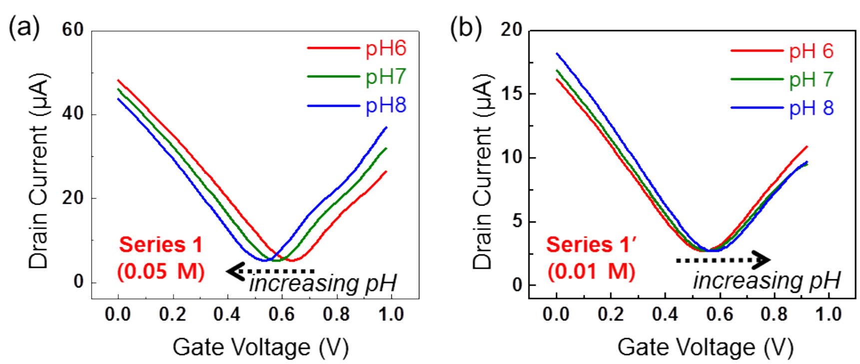

Fig. S3. Transfer characteristics of a graphene transistor (V_D = 0.5 V) operated with pH buffer solutions (a) Series 1 and (b) Series 1′ (pH = 6~8).

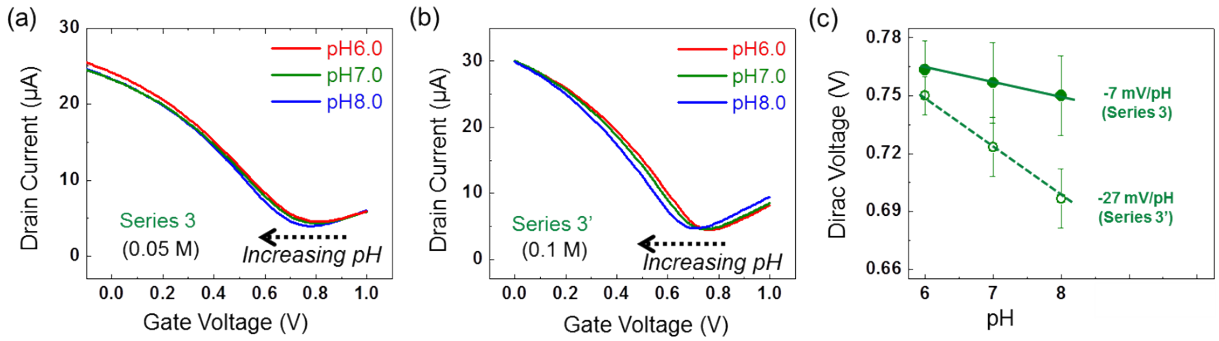

Fig. S4. Transfer characteristics of a graphene transistor (V_D = 0.05 V) operated with pH buffer solutions (pH = 6~8) Series 3 (a) and Series 3′(b). (c) Summary of the V_{Dirac} shift.

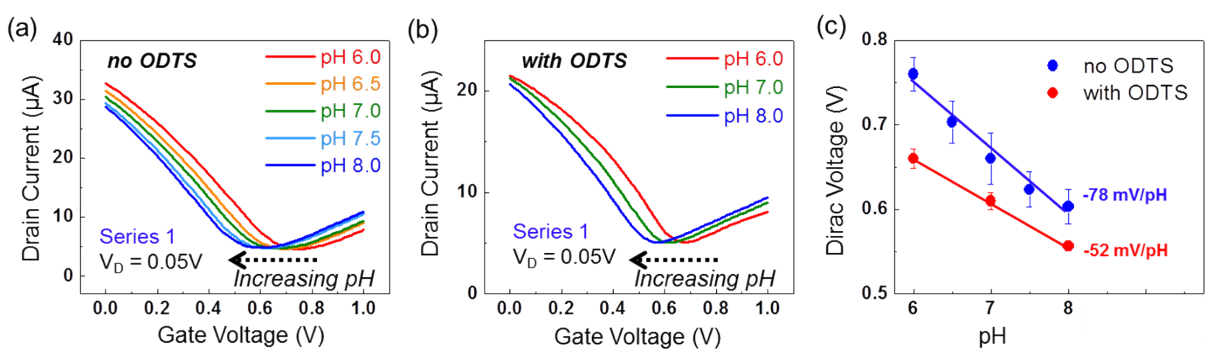

Fig. S5. (a) Transfer characteristics of a graphene transistor (V_D = 0.05 V) that was assembled onto bare SiO_2/Si substrate operated with pH buffer solutions Series 1 (pH = 6~8). (b) Transfer characteristics of a graphene transistor at V_D = 0.05 V that was assembled onto self-assembled monolayer (*n*-octadecyltrimethoxysilane, ODTS)-treated SiO_2/Si substrate operated with pH buffer solutions Series 1 (pH = 6~8). (c) Summary of the V_{Dirac} shift.

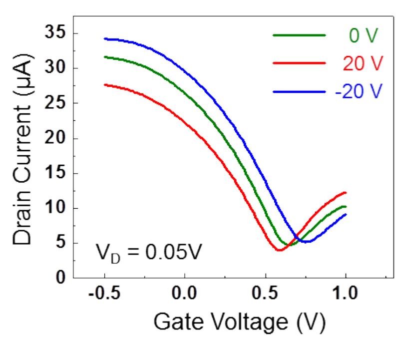

Fig. S6. Transfer characteristics of a solution/SiO_2 dual gateable graphene transistor operated with a buffer solution (pH = 7) of Series 1 under different constant V_{BG}s.

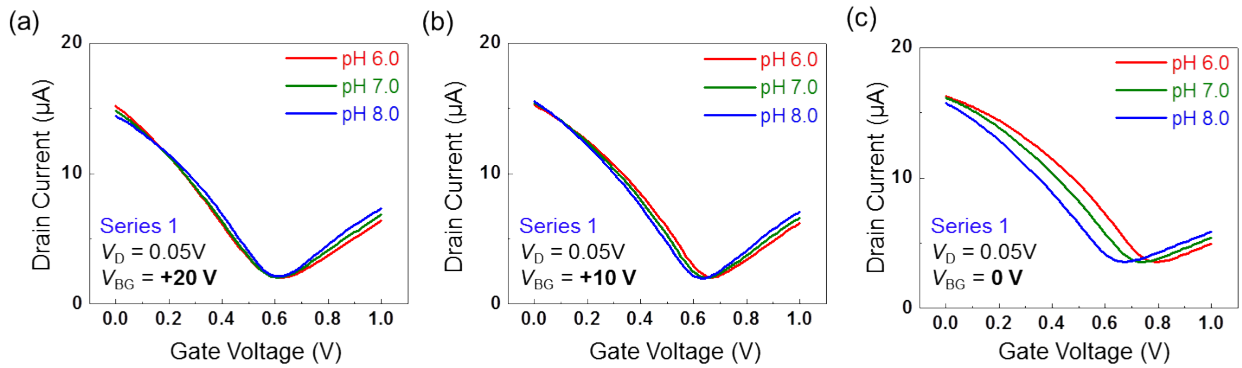

Fig. S7. Transfer characteristics of a solution/SiO_2 dual gateable graphene transistor (V_D = 0.05 V). The gate voltage applied to buffer solution (Series 1) under constant V_{BG}s to the bottom SiO_2/Si gate. (a) V_{BG} = 20 V, (b) V_{BG} = 10 V, and (c) V_{BG} = 0 V.

References

1. Kim, B. J.; Um, S. H.; Song, W. C.; Kim, Y. H.; Kang, M. S.; Cho, J. H., Water-Gel for Gating Graphene Transistors. *Nano Lett.* **2014,** *14* 5, 2610-2616.