Supporting Information

Two-dimensional molybdenum disulphide nanosheets covered metal nanoparticle array as floating gate in multi-functional flash memories

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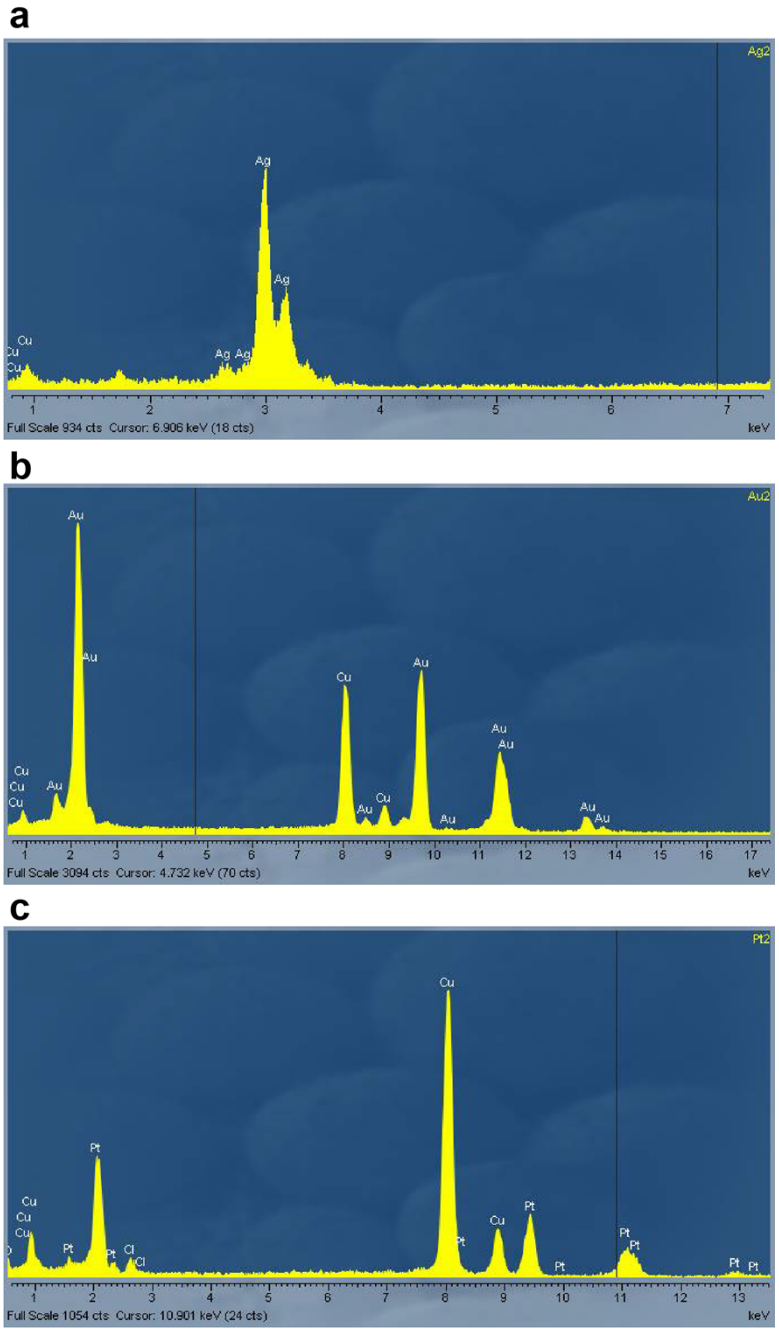

Figure S1. Energy-dispersive X-ray spectroscopy (EDS) spectra of (a) Ag NPs (b) Au NPs and (c) Pt NPs.

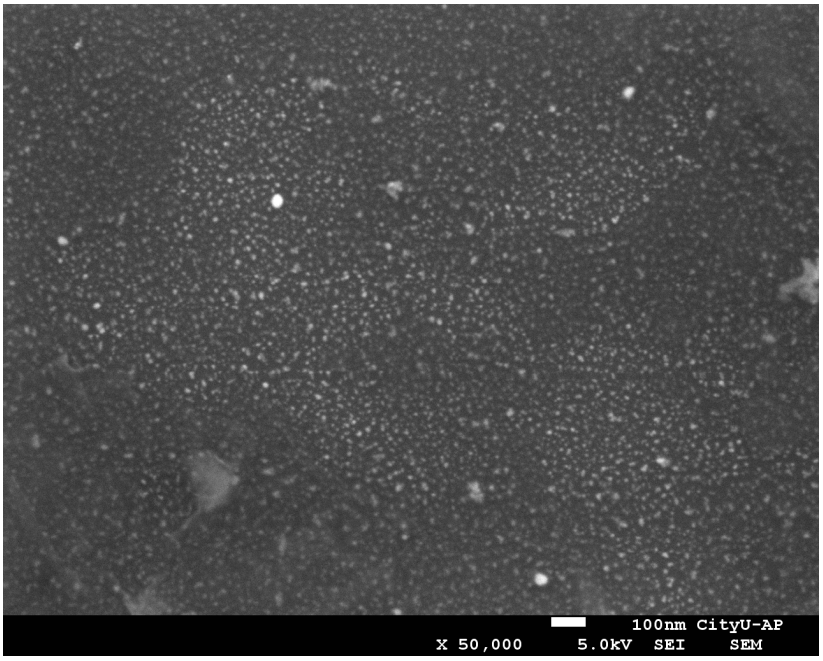

Figure S2. SEM image of the MoS_2 nanosheets self-aligned on the Au NPs monolayer

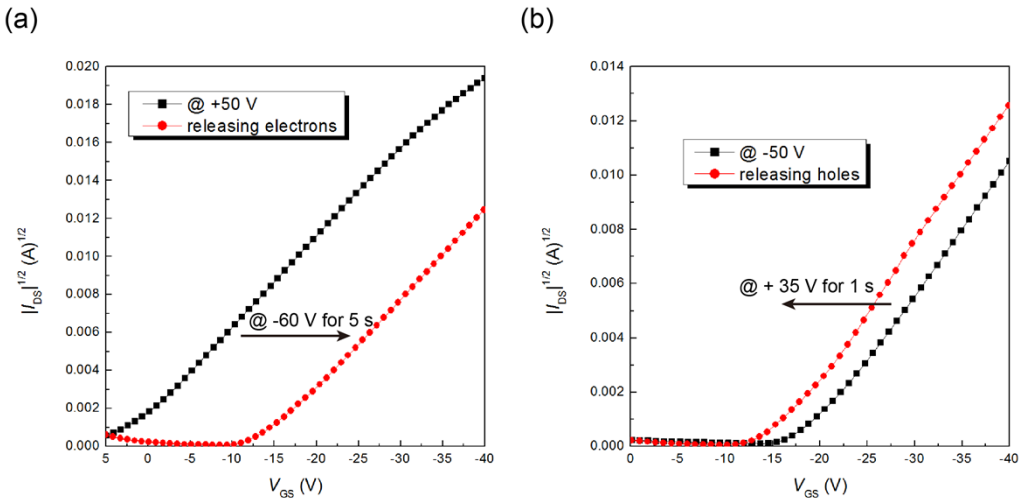

Figure S3. The erasing operation of Ag NPs-MoS_2 memory device. The gate bias of erasing operation to release electrons after positively programming operation is -60 V for 5 s and the gate bias to release holes after negatively programming operation is +35 V for 1 s.

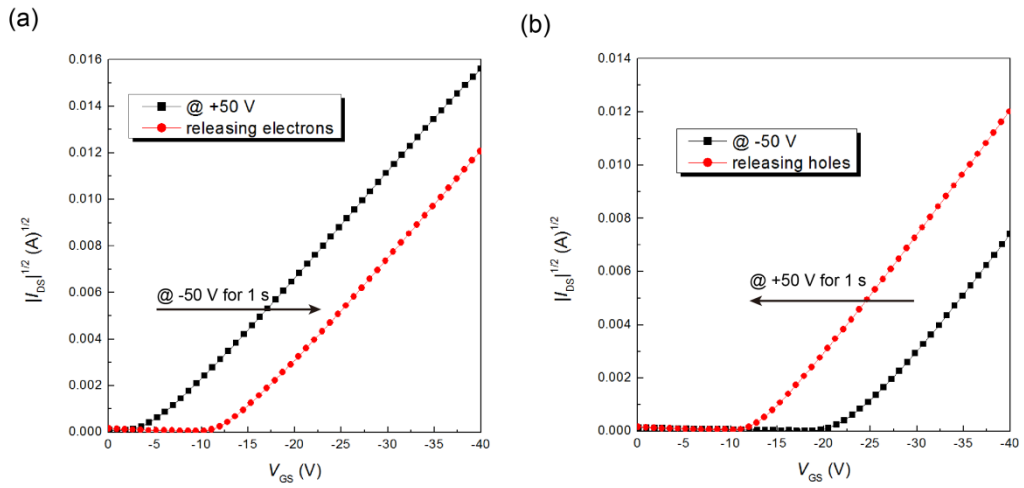

Figure S4. The erasing operation of Au NPs-MoS_2 memory device. The gate bias of erasing operation to release electrons after positively programming operation is -50 V for 1 s and the gate bias to release holes after negatively programming operation is +50 V for 1 s.

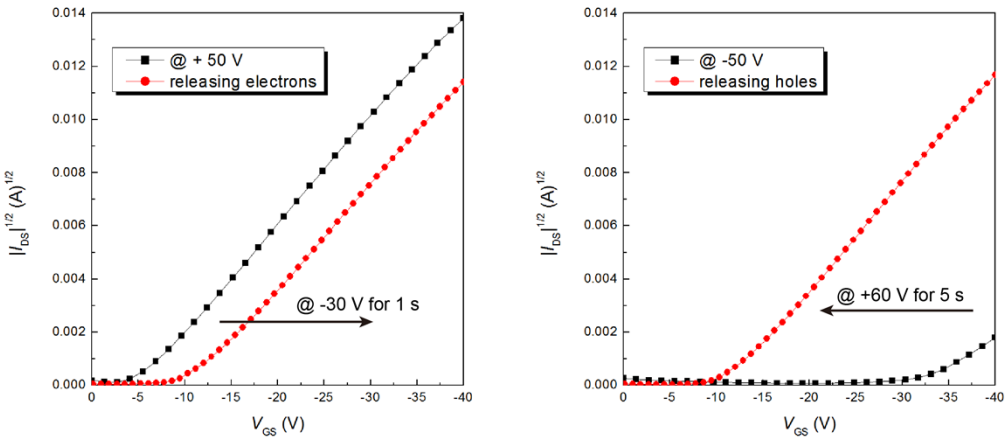

Figure S5. The erasing operation of Pt NPs-MoS_2 memory device. The gate bias of erasing operation to release electrons after positively programming operation is -30 V for 1 s and the gate bias to release holes after negatively programming operation is +60 V for 5 s.

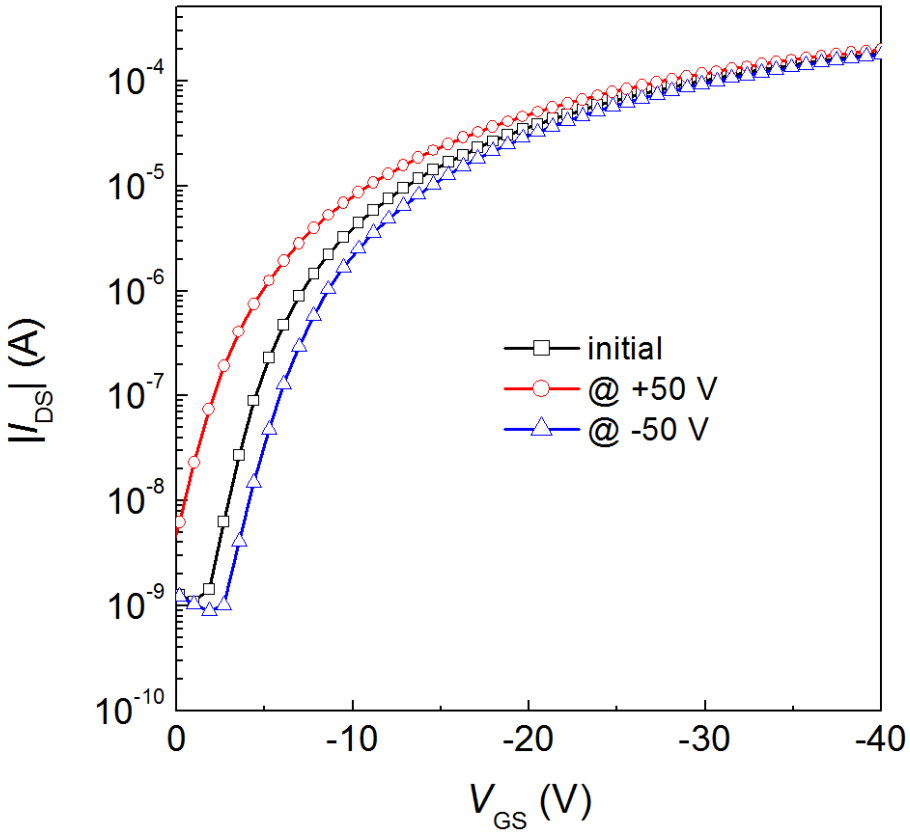

Figure S6. Transfer characteristics of the standard FET devices under programming operation. The positively programming gate bias is set as +50 V for 1 s and the negatively programming operation is set as -50 V for 1 s.

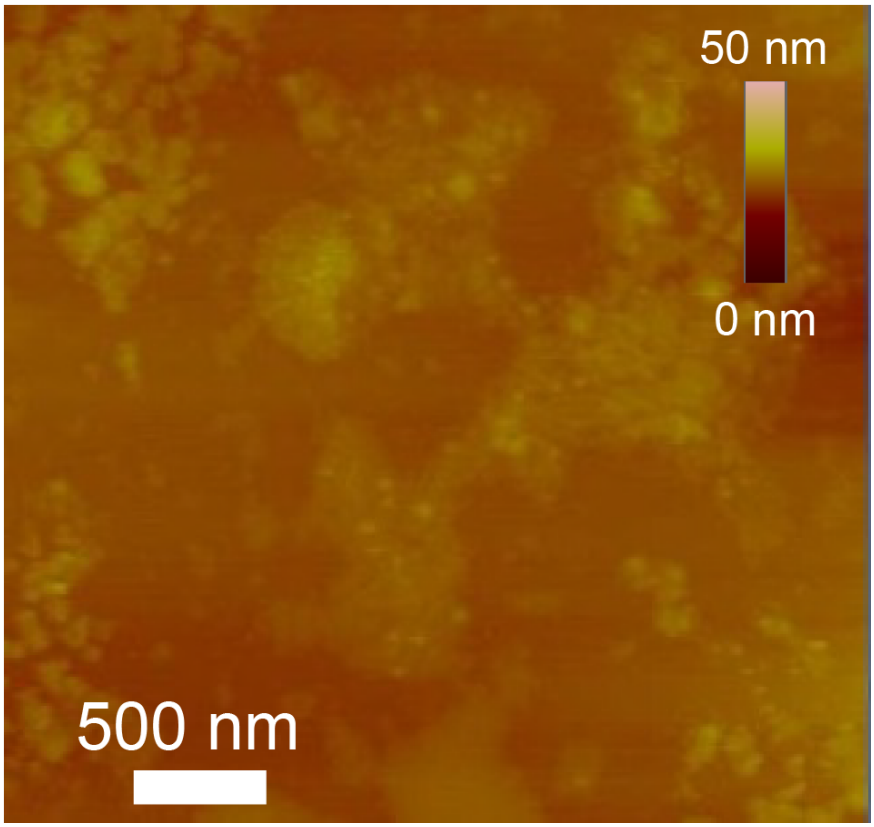

Figure S7. Tapping-mode AFM height image of fabricated MoS_2 film for pristine MoS_2 flash memory.

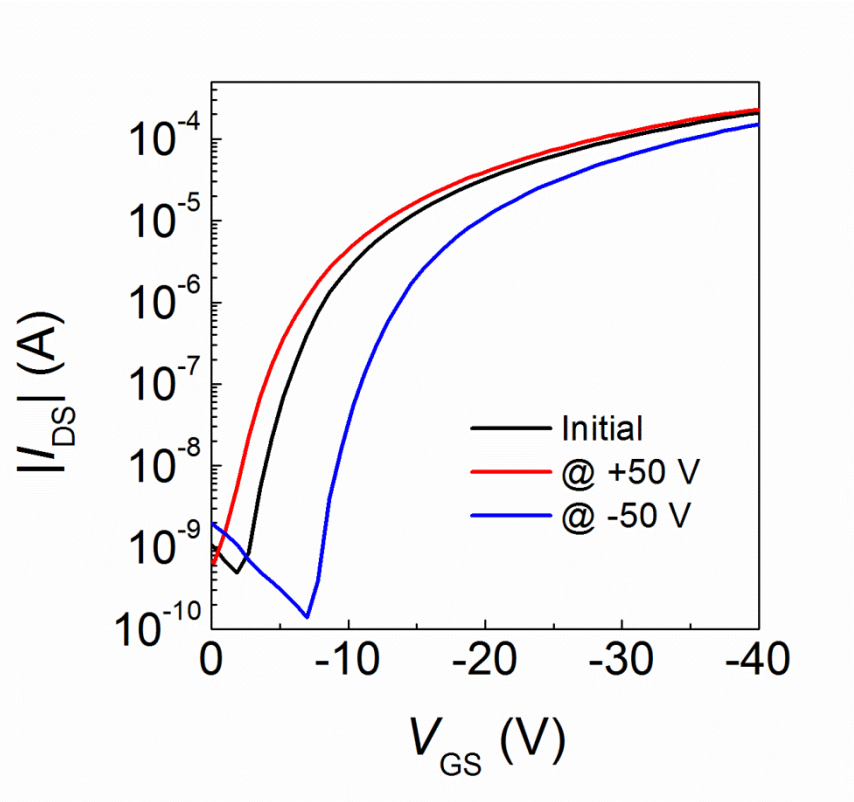

Figure S8. Transfer characteristics of the the memory devices with only Ag nanoparticles. The positively programming gate bias is set as +50 V for 1 s and the negatively programming operation is set as -50 V for 1 s.

Au NPs-MoS_2

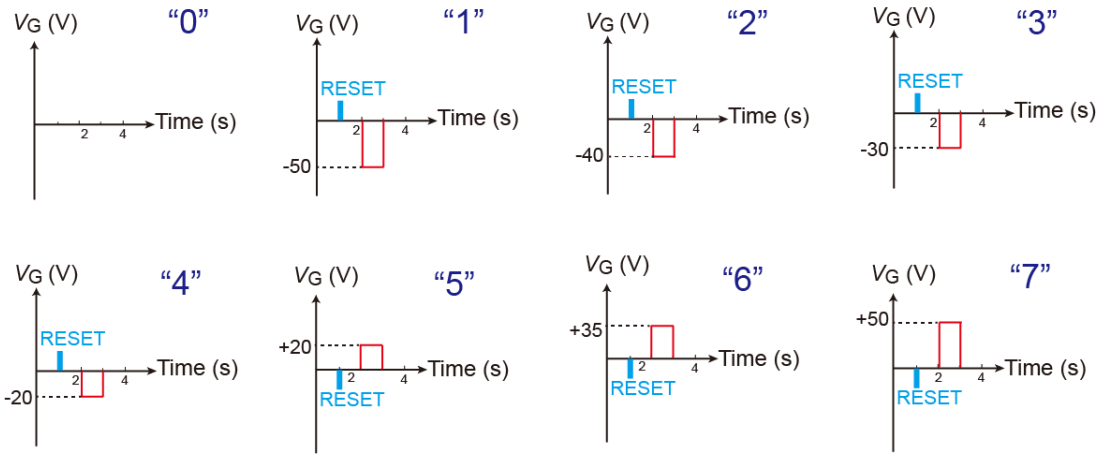

Figure S9. V_{GS} signals used for programming the flash memories into 8 data states ("0" to "7") in Au NPs-MoS_2 flash memories.

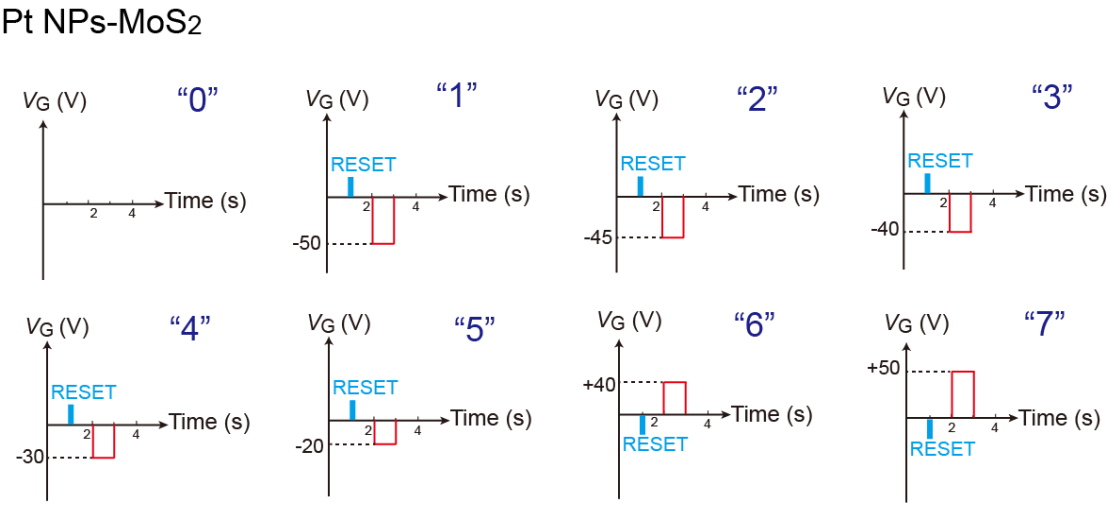

Figure S10. V_{GS} signals used for programming the flash memories into 8 data states ("0" to "7") in Pt NPs-MoS_2 flash memories.

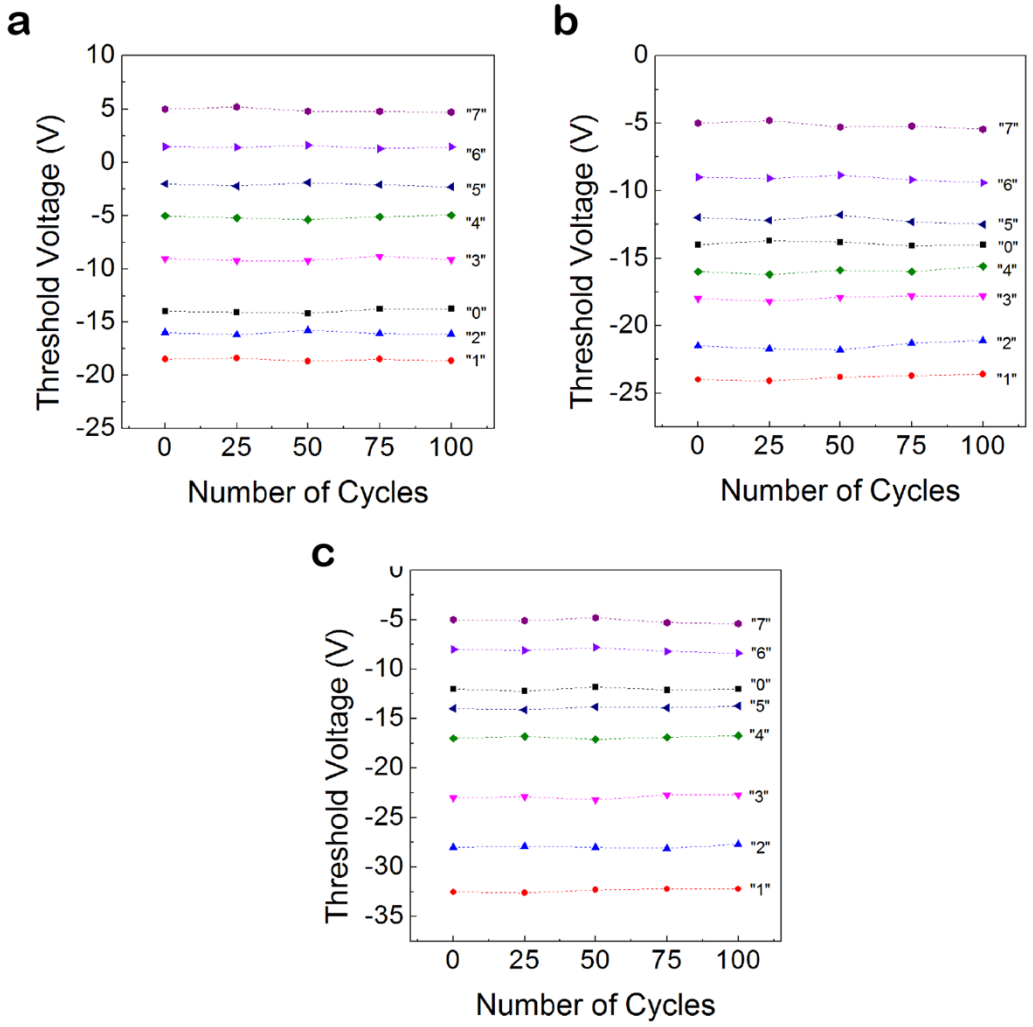

Figure S11. Data levels recorded for 100 sequential cycles of flash memories based on (a) Ag NPs-MoS_2 structure, (b) Au NPs-MoS_2 structure and (c) Pt NPs-MoS_2 structure.