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Electronic Supplementary Information for

Engineering Gate Dielectric Surface Properties for Enhanced Polymer Field-Effect Transistor Performance

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Experimental Section

Preparation of silane-SAMs

The silylating agents for forming silane-SAMs on SiO_2 surface, MTS (98%), PTS (98%) OTS-8 (97%), and OTS-18 (> 90%) were purchased from Sigma-Aldrich and used as received without further purification. Highly doped <100> p-Si wafers (SWI, ρ=0.001~0.005 ohm-cm) with a ~300 nm thick thermally grown SiO_2 layer were used as the gate substrate, with the top SiO_2 layer serving as the gate dielectric. The SiO_2 wafer substrate was first cleaned by sonication sequentially in deionized water, acetone, and 2-proponol, followed by cleaning with UV-ozone for 5 min. For silane-SAM formation via silylation with a single silylating agent, the cleaned Si wafer substrate was immersed in a 0.1 M solution of the silylating agent in toluene at 60 °C for 20~30 min, followed by rinsing with toluene and then 2-proponol, and subsequently blowing dry with nitrogen gas. This procedure had earlier been shown to yield a chemically robust silane-SAM on SiO_2 surface without the need for further thermal treatment. For dual-silane "hybrid" SAM formation, the modified SiO_2 substrate with the first silane-SAM was again treated with a dilute solution of another silylating agent in accordance with the same silylation procedure as before, thus creating a "hybrid" silane-SAM structure composed of two silanes.

Device fabrication

OFETs were fabricated in a staggered bottom-gate, top-contact configuration. Two different polymer semiconductors, mid-MW DPP-DTT (Mn ~ 90K; Mw ~ 299K) as previously reported[3] and *regio*-P3HT (98%; Rieke), were used as the channel semiconductors in the test devices. The DPP-DTT semiconductor solution was prepared in chlorobenzene at the concentration of 4 mg/mL while the *regio*-P3HT solution was prepared in chloroform at the same concentration. The channel semiconductor was prepared by spin coating the semiconductor solution on top of

bare SiO_2 surface (control device) or silane-SAM-modified SiO_2 surface at 1000 rpm, followed by annealing at an elevated temperature in an inert atmosphere. Subsequently, the gold source/drain electrode pairs were deposited on top of the semiconductor layer by vacuum thermal evaporation through a shadow mask to create OFETs with channel length (L) and width (W) of 80 μm and 1500 μm, respectively.

Characterization

The wettability of the silane SAM-modified SiO_2 surface was determined by measuring its water contact angle using a contact angle goniometer. The contact angle was obtained by a numerical fitting algorithm using the side view of a deionized water drop. The morphology and roughness of the solution-deposited polymer semiconductor on silane-SAM-modified SiO_2 substrate were characterized by atomic force microscopy. Wide-angle, out-of-plane XRD measurements were carried out on a Bruker D8 Advance system (Cu X-ray source, 40 kV and 30 mA). The electrical performance of OFET devices was characterized by measuring their transfer and output characteristics using a Keithley 2636B dual-channel SourceMeter in ambient environment. The field-effect mobility in the saturation regime was extracted from the following equation: $I_{ds} = \mu C_i (V_g - V_{th})^2 (W/2L)$, where I_{ds} is the drain current, μ is the field-effect mobility, C_i is the capacitance per unit area of the gate dielectric layer (C_i = 10 nF cm^{-2}), and V_g is gate voltage, respectively.

Table S1

Performance characteristics of OFET devices fabricated with DPP-DTT channel semiconductor on SiO_2 substrates modified with a mixture of OTS-8 and OTS-18 of different ratio.

Mole ratio of OTS-18:OTS-8	Average FET mobility ($cm^2/V{\cdot}s$)	On/off ratio	Off current (nA)	S.S. (V/decade)
1.0:0	1.89	3×10^4	4.6	3.3
0.9:0.1	1.87	8×10^4	2.2	3.0
0.8:0.2	1.79	1×10^5	1.7	3.0
0.6:0.4	1.41	2×10^5	0.4	2.5
0:1.0	0.79	5×10^5	0.2	2.7

Table S2

Performance characteristics of OFET devices fabricated with regio-P3HT channel semiconductor on various silane-modified SiO_2 substrates.

Silylating agents	Average FET mobility ($cm^2/V{\cdot}s$)	On/off ratio	Off current (nA)	S.S. (V/decade)
Untreated	3.5×10^{-4}	1×10^1	23	15
PTS	6.0×10^{-4}	7×10^1	6	12
OTS-8	0.004	1×10^3	2	5.8
OTS-18	0.019	2×10^2	26	6.9
OTS-18/PTS	**0.014**	$\mathbf{3\times10^3}$	**3**	**5.0**
OTS-18/OTS-8	**0.021**	$\mathbf{5\times10^3}$	**2**	**4.2**