Electronic Supplementary Material (ESI) for RSC Advances.

Spiral Growth Mode in DMDPC Organic Thin Film Transistors by Physical Vapor Deposition

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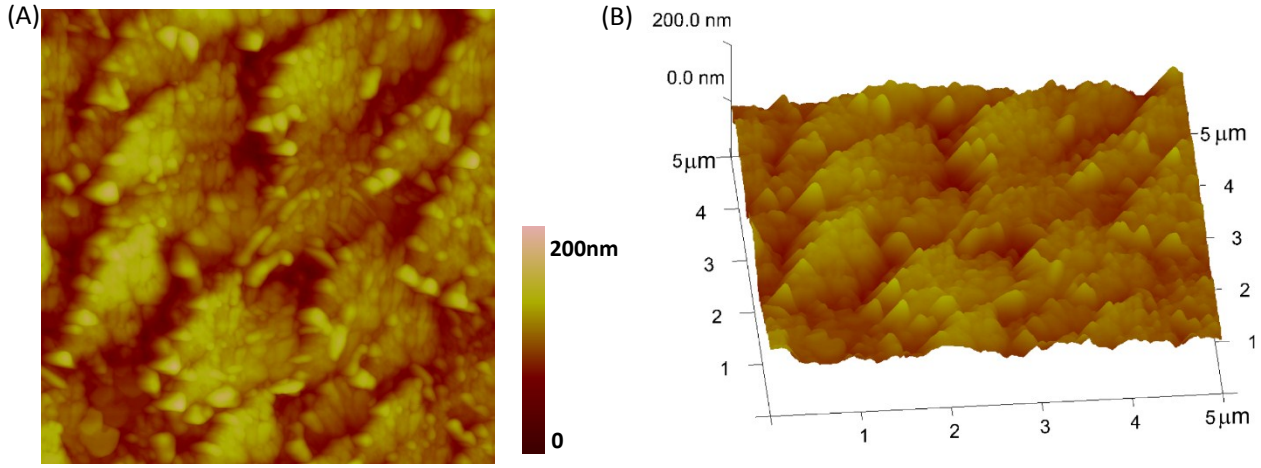
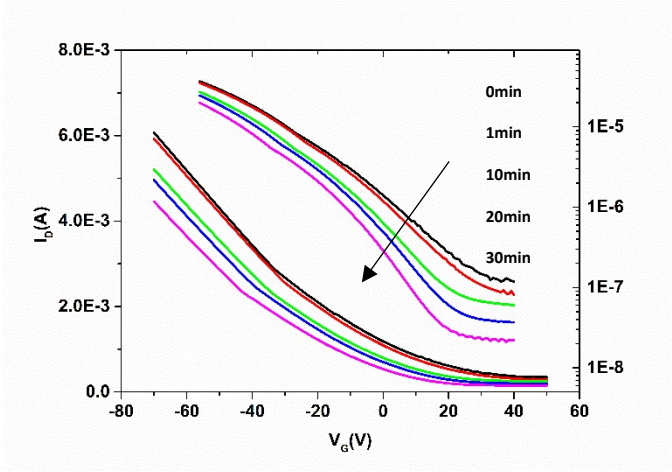
The DMDPC thin film morphology on bare SiO_2 substrate without modification was tiny island sharp with the same evaporation rate 0.2nm/min.



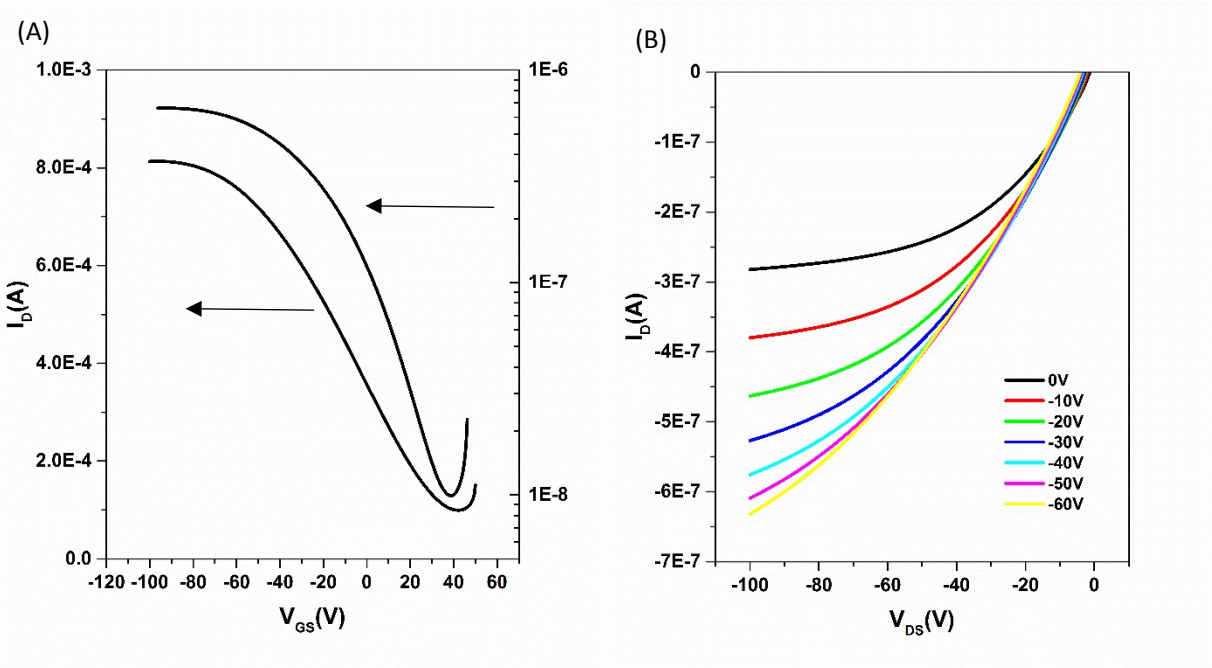
S1. (A) 5µm × 5µm AFM height image of DMDPC films namely thickness 45nm on bare Si/SiO_2, (B) A 3D view AFM image of the DMDPC films on bare Si/SiO_2.

The off current in OTFTs was usually dependent on the gate leakage current and the conductivity of the semiconductor layer. If the semiconductor layer was doped, the off current would increase. In our case, the SiO2 layer of 300nm was thick enough and the gate leakage current could be neglected. In fact, we have measured the electronical characteristics of the OFETs under vacuum. With the vacuum pumped for 30 minutes, the off current decreased from 1E-7 to 2E-8. One possible explanation is that the channel between the semiconductor and the substrate was doped by the air. The electron in the HOMO level was easy to jump to the trap level, thus the density of hole in HOMO level was high under zero gate voltage.



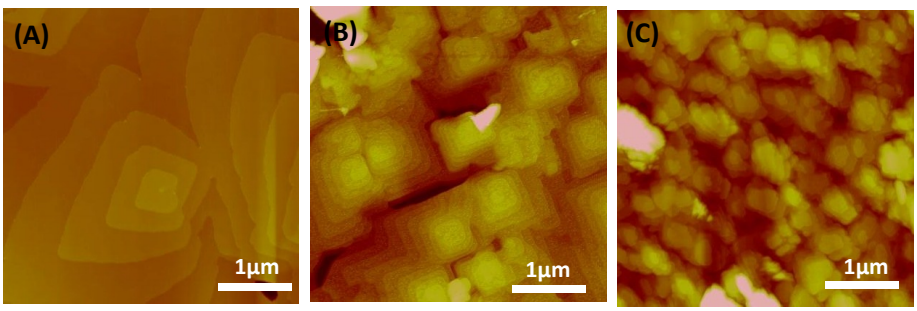
S2 The transfer curve of DMDPC OTFTs with the vacuum pumped for 30 minutes

As to the fabrication of TFTs, 45nm DMDPC films were deposited onto the bare SiO_2 substrate at room temperature in the deposition rate 1nm/min. Source and drain electrodes were formed by evaporating 50 nm gold films through a shadow mask with channel length L=50 μm and width W=1000 μm. Electrical characterization of devices was measured in air by a Keithley 4200 semiconductor analyzer.

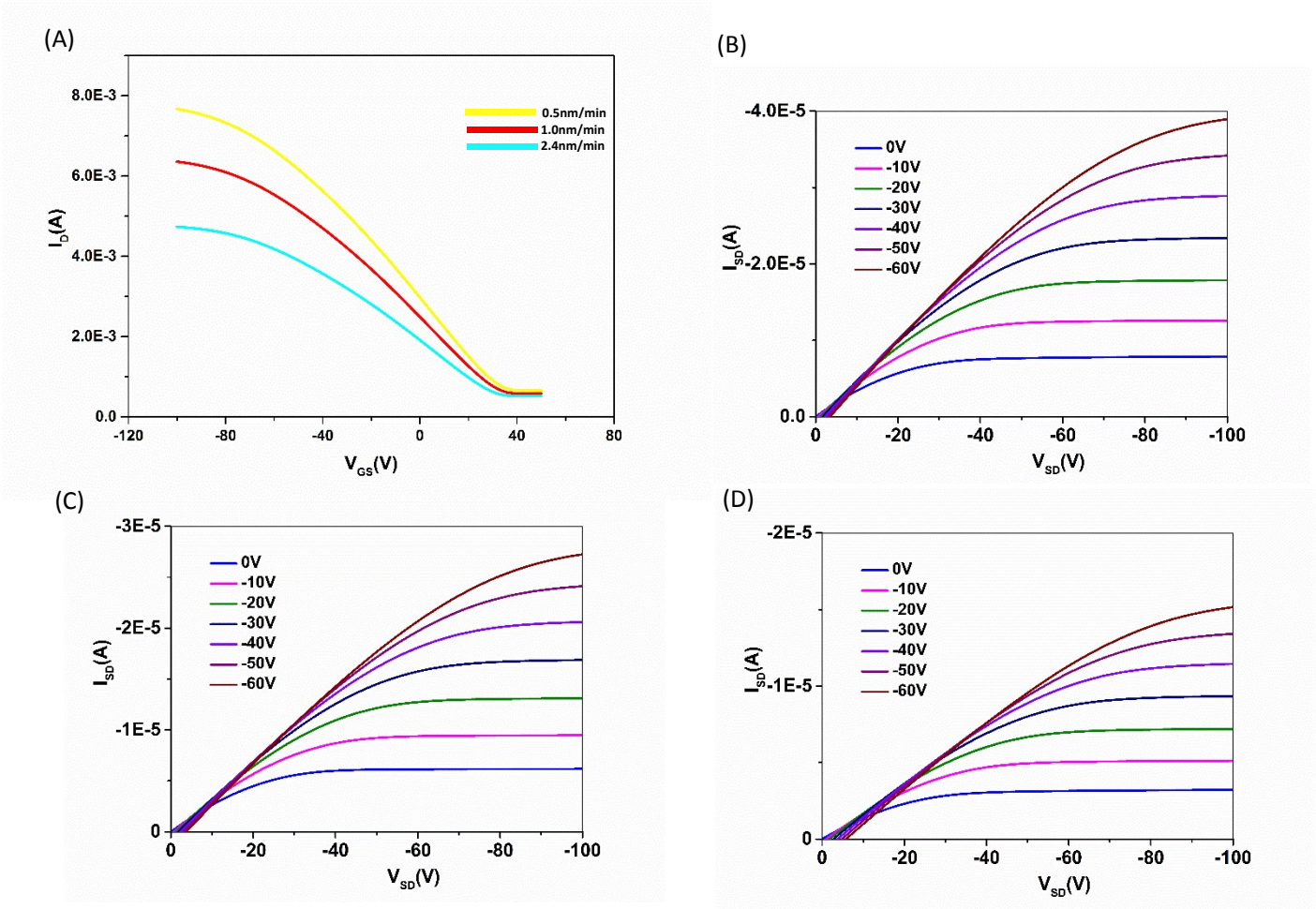


S3. Device performance of DMDPC thin film on bare SiO_2 substrate. (A) I_{DS}-V_{GS} characteristics at V_{DS}=-100V. (B) I_{DS}-V_{DS} characteristics of the device in (A). From top to bottom, V_G=0V, -10V, -20V, -30V, -40V, -50V and -60V, respectively.

The 45nm DMDPC films were deposited onto the OTS-SAM modified SiO2 substrate at room temperature in the deposition rate 0.5, 1.0 and 2.4nm/min. Source and drain electrodes were formed by evaporating 50 nm gold films through a shadow mask with channel length L=50 μm and width W=1000 μm. The transfer curves and output curves were shown in the below. The mobility of DMDPC film transistors decreased from 0.06 $cm^2V^{-1}s^{-1}$ (0.5nm/min) to 0.008 $cm^2V^{-1}s^{-1}$ (2.4nm/min). As the deposition rate increasing, the grain size decreased (shown in S4) and the relevant mobility decreased (shown in S5), which was complementary to explain the relationships between the fabrication conditions and the device performance.



S4 (A-C) 5μm × 5μm AFM images of DMDPC films with 45 nm deposited with different deposition rate 0.5, 1.0 and 2.4nm/min, respectively.



S5 (A) Transfer curve of DMDPC based TFTs under different deposition rate at V_{SD}=-100V. (B-D) Output characteristics of DMDPC based TFTs under different deposition rate 0.5, 1.0 and 2.4nm/min, respectively.