Electronic Supplementary Material (ESI) for RSC Advances.

Supporting Information

Role of annealing temperature on the sol-gel synthesis of VO_2 nanowires with *in situ* characterization of their metal-insulator transition

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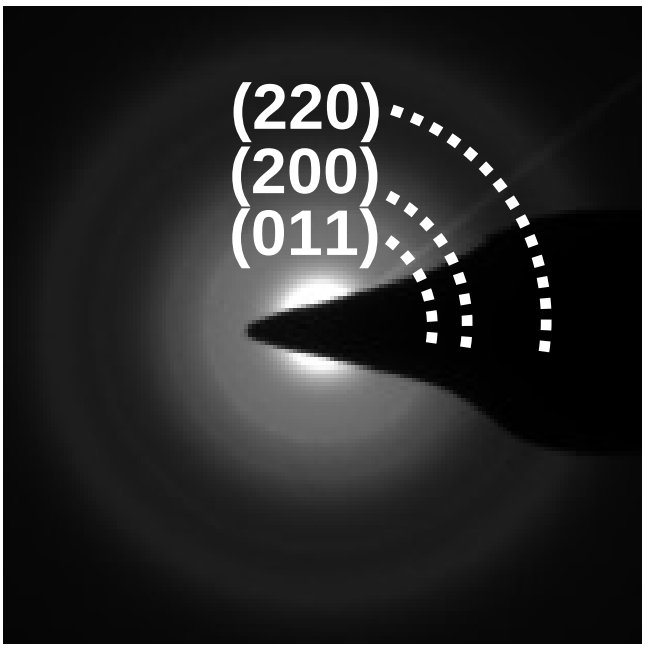

Figure S1. The SAED pattern including poly crystalline rings of (011), (200) and (220) lattice planes of VO_2 M1 phase as shown in Figure 2h.

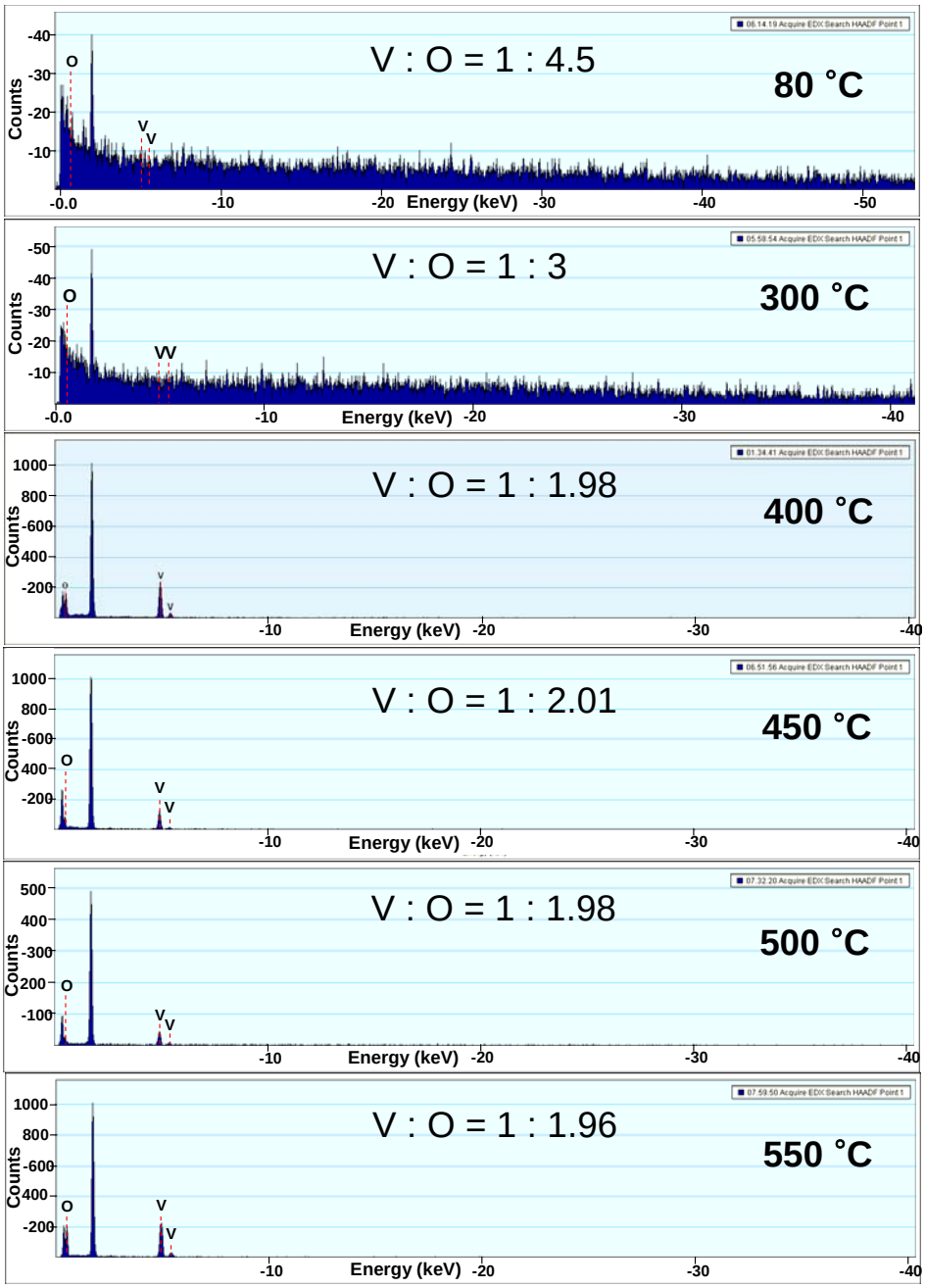

Figure S2. Representative EDS spectrum data of the samples annealed at various temperatures.

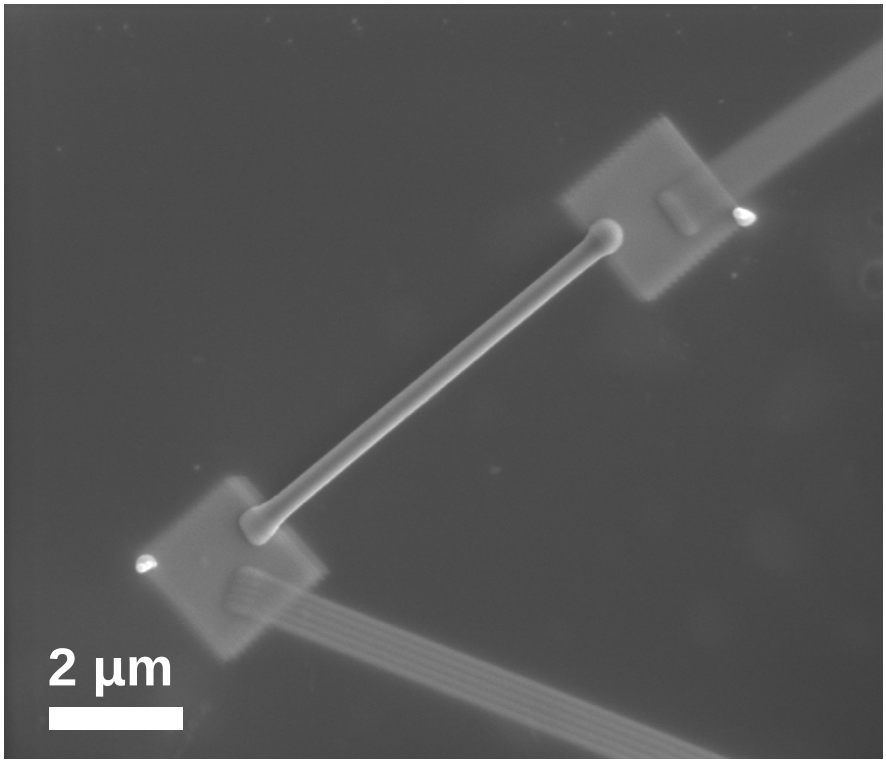

Figure S3. The SEM image of the individual VO_2 nanowire device fabricated on a customized Si_3N_4 TEM grid, and analyzed in Figures 4 and 5.

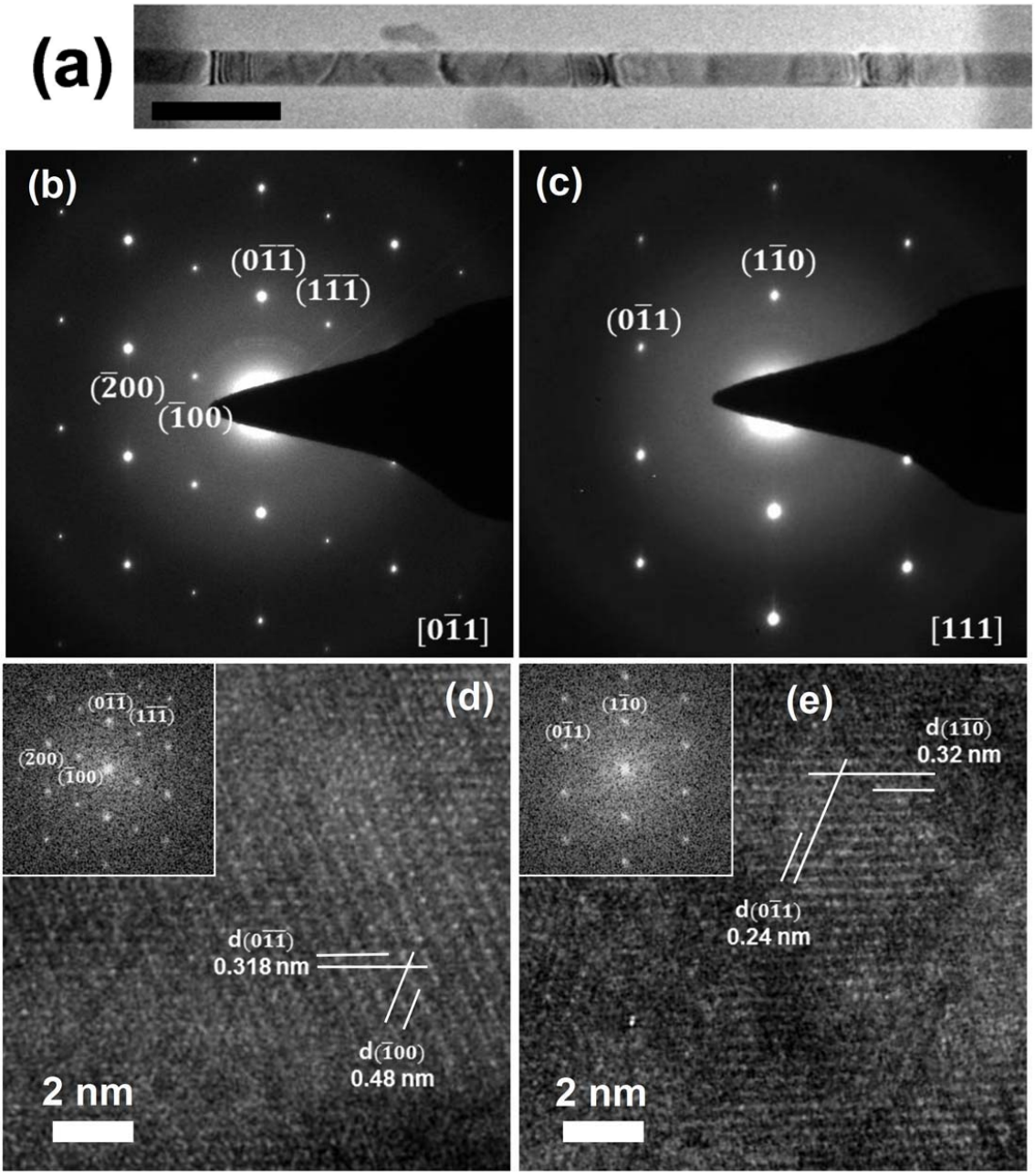

Figure S4. (a) The TEM BF image of the individual VO_2 nanowire device fabricated on a customized Si_3N_4 TEM grid, and analyzed in Figures 4 and 5. (b and c) The SAED patterns of the M1 and R phases of the nanowire in Figure S4(a), respectively. (d and e) The HRTEM images with their corresponding FFT patterns of the M1 and R phases of the nanowire in Figure S4(a), respectively. The growth direction of the wire is [100].