Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.
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Supporting Information

C-axis Oriented Crystalline IGZO Thin-Film Transistors by Magnetron Sputtering

Junpeng Zhang, Xizhang Wen, Luyao Hu, Wangying Xu*, Deliang Zhu*, Peijiang Cao, Wenjun Liu, Shun Han, Xinke Liu, Fang Jia, Yuxiang Zeng, Youming Lu

Guangdong Research Center for Interfacial Engineering of Functional Materials, Shenzhen Key Laboratory of Special Functional Materials, College of Materials Science and Engineering, Shenzhen University, Shenzhen 518060, China

*mail: wyxu@szu.edu.cn; dlzhu@szu.edu.cn

We have carried out the positive bias stress study of IGZO before and after annealing at 400 ^{o}C under ambient conditions (relative humidity ~90% in Shenzhen, China), as shown in Figure S3. The positive threshold voltage could be attributed to the electron trapping at the semiconductor channel or channel/dielectric interface. Besides, since the device is unpassivated and tested in ambient conditions with high humidity, which could also cause the device instabilities. Further optimization of the IGZO TFTs, especially with the introduction of passivation layer will improve the device stability. However, the 400 ^{o}C-annealed IGZO TFTs indeed showed much better performance and stability compared with the as-deposited counterpart.

Table S1. Cation fraction of IGZO thin films under various annealing temperatures by EDS.

Annealing temperature (°C)	In (at%)	Ga (at%)	Zn (at%)	In:Ga:Zn (at%)
As-deposited	12	6.84	35.55	0.34:0.19:1
200	13.07	6.94	35.8	0.37:0.19:1
300	11.64	6.81	34.6	0.34:0.20:1
40	13.31	6.60	37.24	0.36:0.18:1
500	12.84	6.96	36.06	0.36:0.19:1
600	13.35	6.32	36.39	0.37:0.17:1

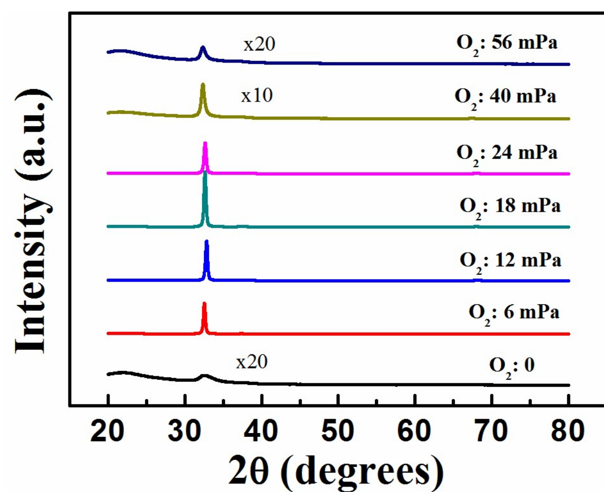

Figure S1. XRD patterns of IGZO thin films deposited with different with different oxygen partial pressures.

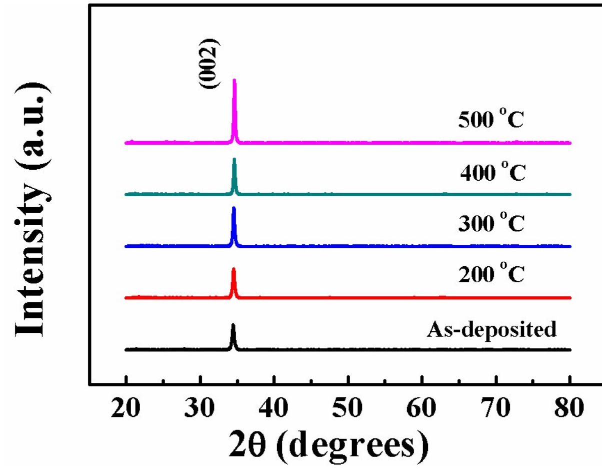

Figure S2. XRD patterns of ZnO thin films under different annealing temperatures fabricated using similar deposition conditions as that of IGZO films.

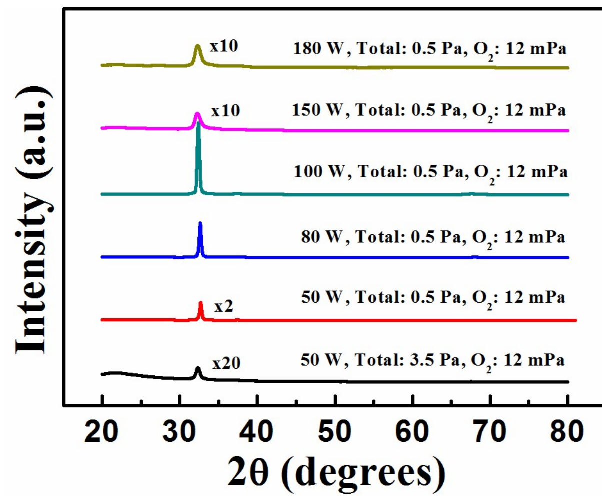

Figure S3. XRD patterns of IGZO thin films under different deposition powers and pressures.

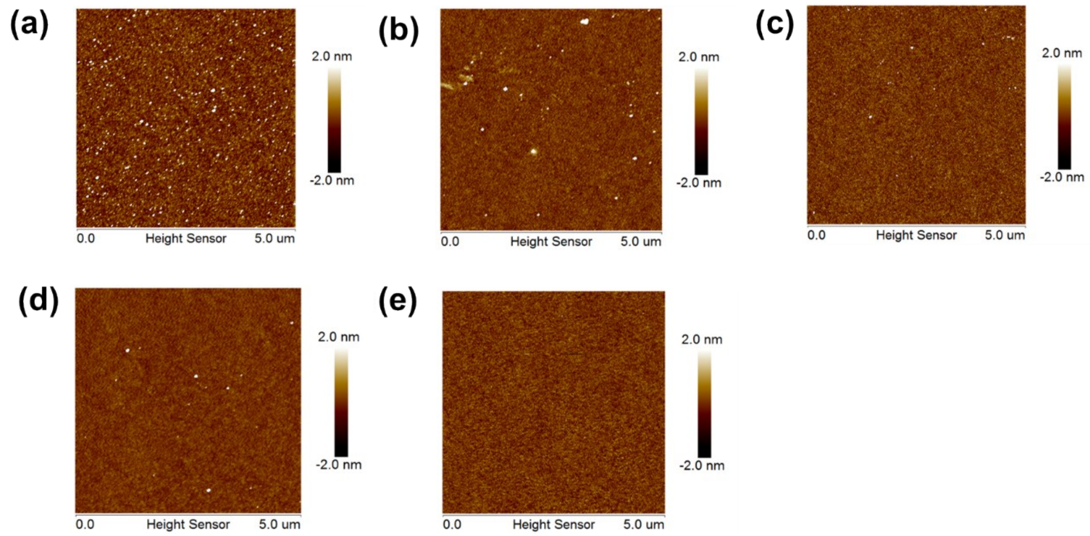

Figure S4. AFM images of IGZO thin films with different oxygen partial pressures of (a) 0 (rms: 0.45 nm), (b) 6 mPa (rms: 0.42 nm), (c) 12 mPa (rms: 0.37 nm), (d) 18 mPa (rms: 0.20 nm) and (e) 40 mPa (rms: 0.24 nm).

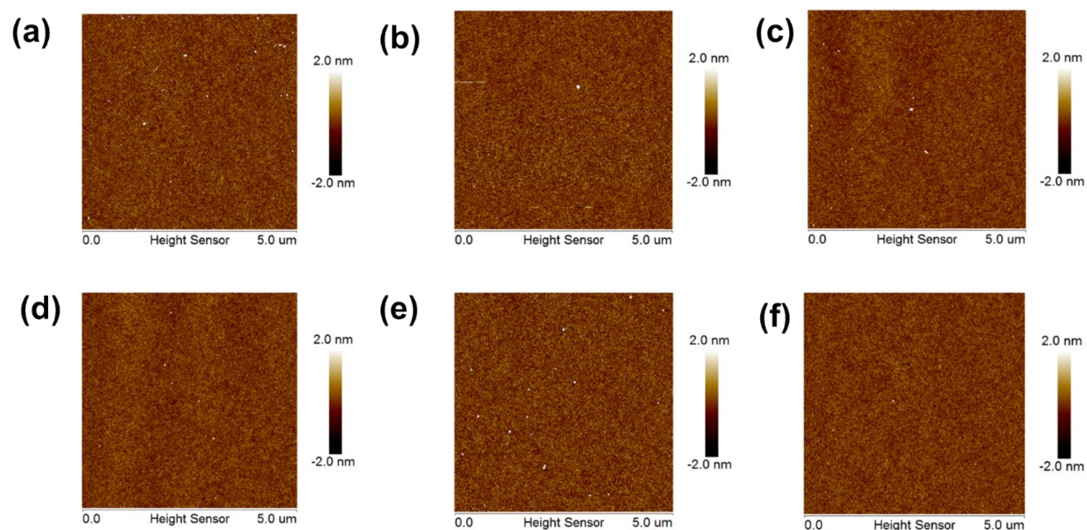

Figure S5. AFM images of IGZO thin films with different annealing temperatures of (a) non-annealed (rms: 0.37 nm), (b) 200 ^{o}C (rms: 0.32 nm), (c) 300 ^{o}C (rms: 0.25 nm), (d) 400 ^{o}C (rms: 0.28 nm), (e) 500 ^{o}C (rms: 0.37 nm) and (f) 600 ^{o}C (rms: 0.28 nm).

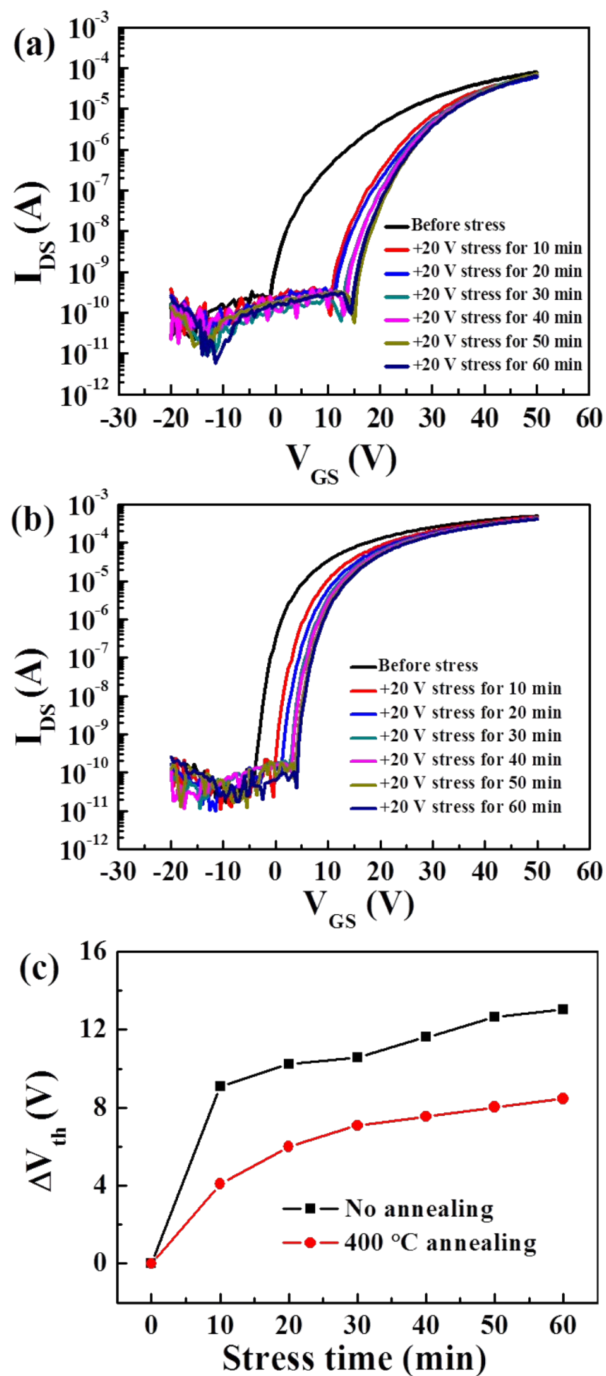

Figure S6. Transfer characteristics of (a) as-deposited and (b) 400 °C-annealed IGZO TFTs under a positive gate bias of 20 V. (c) Summary of threshold voltage shift of the two devices.