Ferroelectric Nanocomposite Networks with High Energy Storage Capacitance and Low Ferroelectric Loss by Designing Hierarchical Interface Architecture

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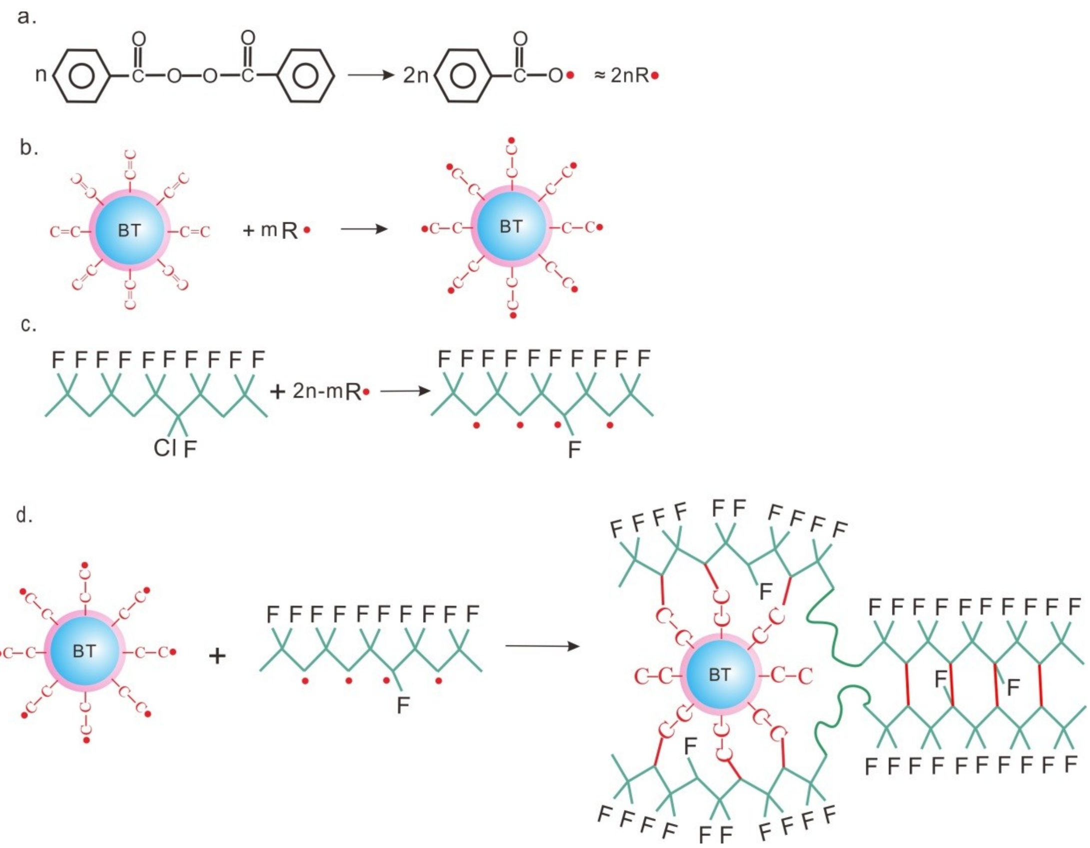

Figure S1. Schematic illustration of the mechanism of the cross-linking reactions in P(VDF-CTFE)/MPS@BT nanocomposite networks.

Table S1. Lattice constant and coherence length for the (200, 020) reflection of P(VDF-CTFE)/MPS@BT nanocomposites (B_0, B_5, B_{10}, and B_{15}) and nanocomposite networks ($B_{10}P_{10}$, and $B_{10}P_{15}$).

	***α*-phase**		***β*-phase**	
	***d*, Å (020)**	***L*, nm**	***D*, Å(100, 200)**	***L*, nm**
P(VDF-CTFE)	4.48	11.0	4.32	6.7
B_5	4.43	10.3	4.28	7.3
B_{10}	4.46	9.7	4.30	8.1
B_{15}	4.45	8.1	4.29	9.0
$B_{10}P_{10}$	4.43	7.3	4.31	6.2
$B_{10}P_{15}$	4.46	6.5	4.31	5.8

Table S2. Melting temperature (T) and the relative crystallinity of the P(VDF-CTFE)/MPS@BT nanocomposites and nanocomposite networks calculated from DSC curves.

Sample	T_m (°C)	Crystallinity (%)
P(VDF-CTFE)	173	23.6
B_5	171	25.2
B_{10}	172	25.4
B_{15}	171	26.1
$B_{10}P_{10}$	169	22.4
$B_{10}P_{15}$	168	21.7

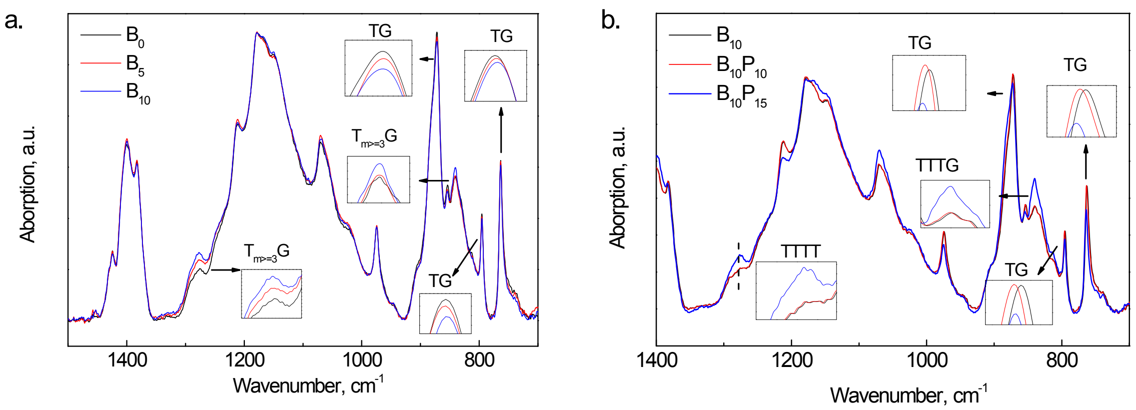

Figure S2. FTIR spectrum of (a) P(VDF-CTFE) and P(VDF-CTFE)/MPS@BT nanocomposites (B_5, and B_{10}).

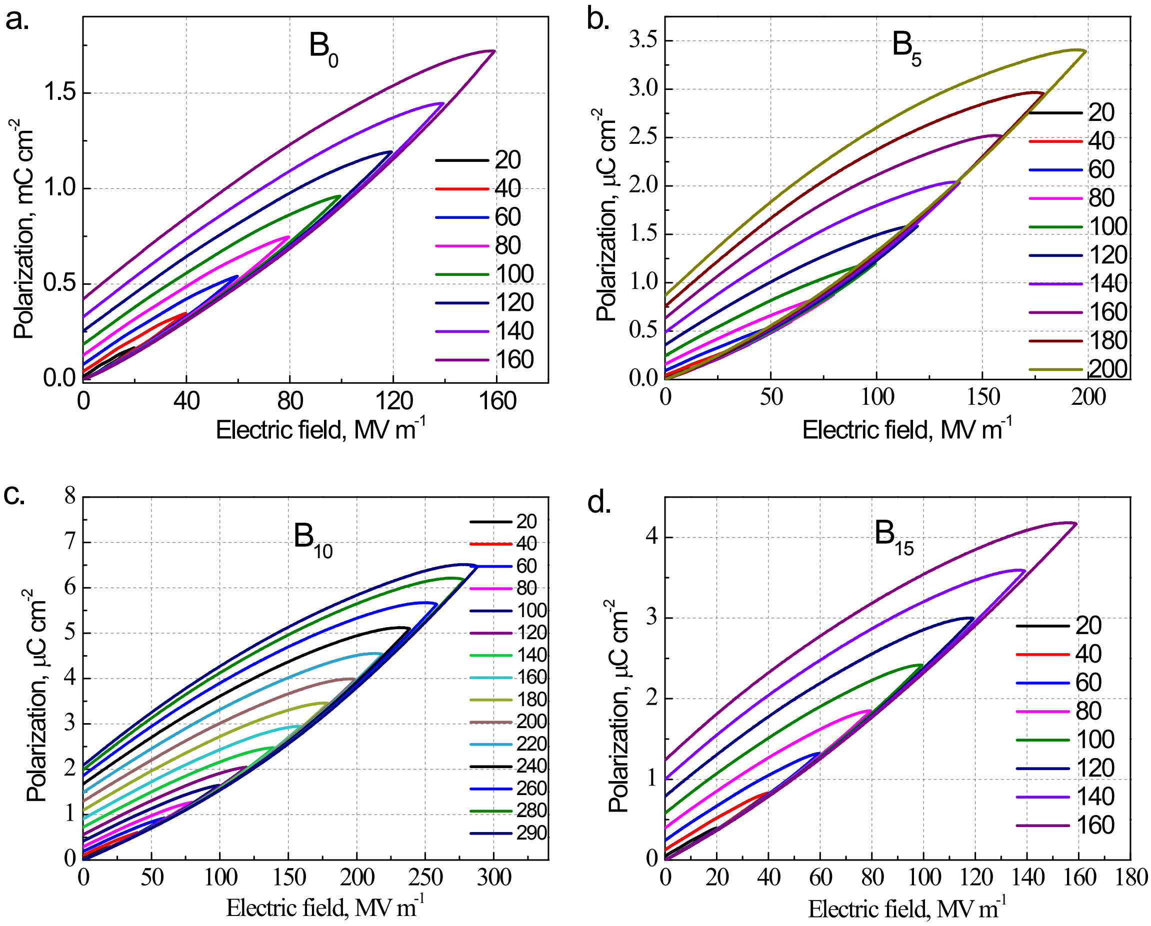

Figure S3. Unipolar D-E hysteresis loops for P(VDF-CTFE)/MPS@BT nanocomposites (a) B_0, (b) B_5, (c) B_{10}, and (d) B_{15}.

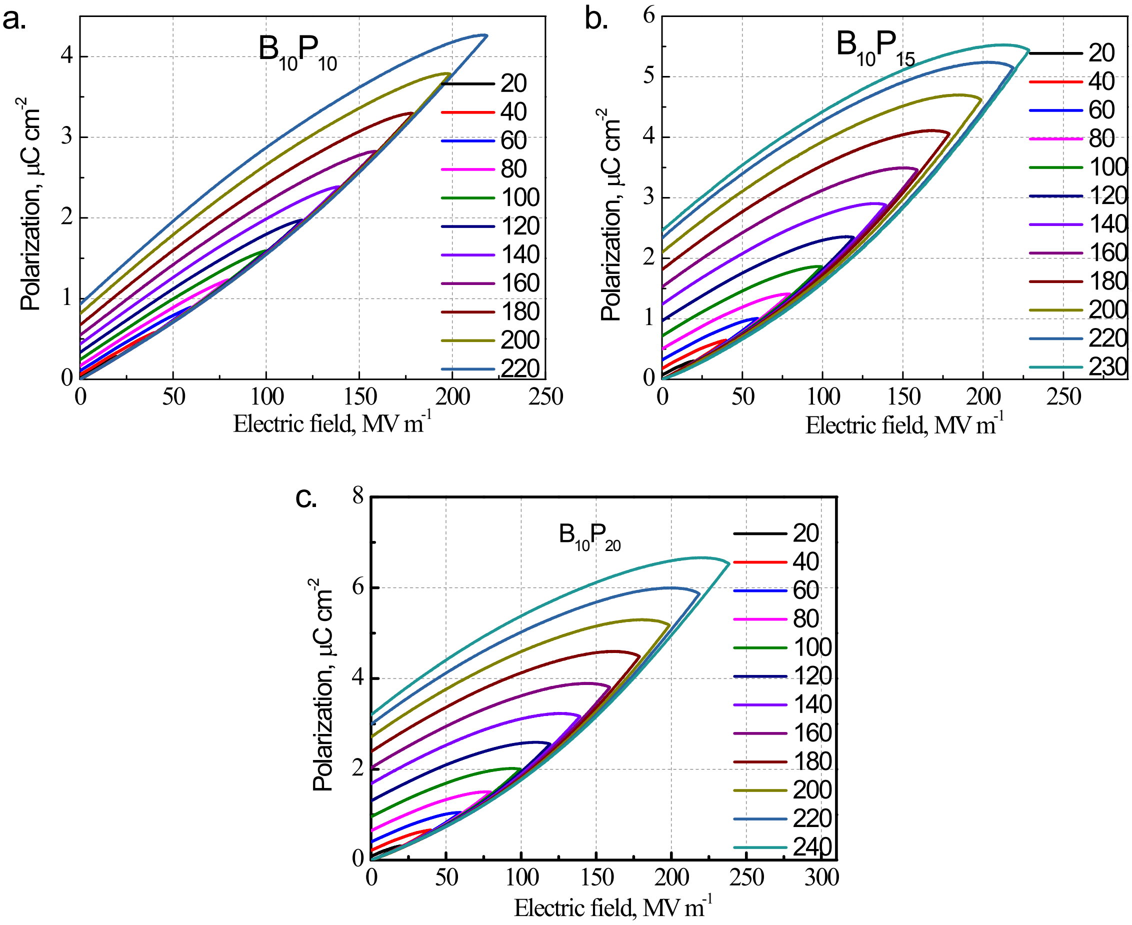

Figure S4. Unipolar D-E hysteresis loops for P(VDF-CTFE)/MPS@BT nanocomposite networks (a) $B_{10}P_{10}$, (b) $B_{10}P_{15}$, and (c) $B_{10}P_{20}$.