Electronic Supplementary Material (ESI) for Physical Chemistry Chemical Physics

Electronic Supplementary Information

Photoelectric probing for the interfacial trap density-of-states in ZnO nanowire field-effect transistors

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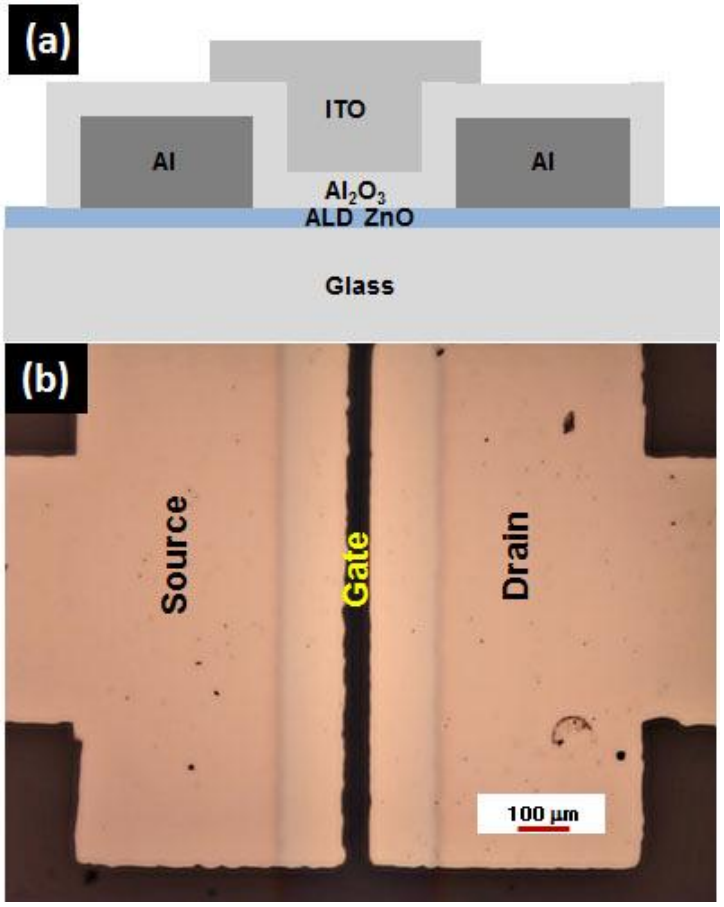

Figure S1. (a) Schematic cross-section and (b) Optical microscopic plan view images of transparent top-gate ZnO (20 nm) TFT with 30 nm ALD Al_2O_3 gate insulator fabricated on glass substrate

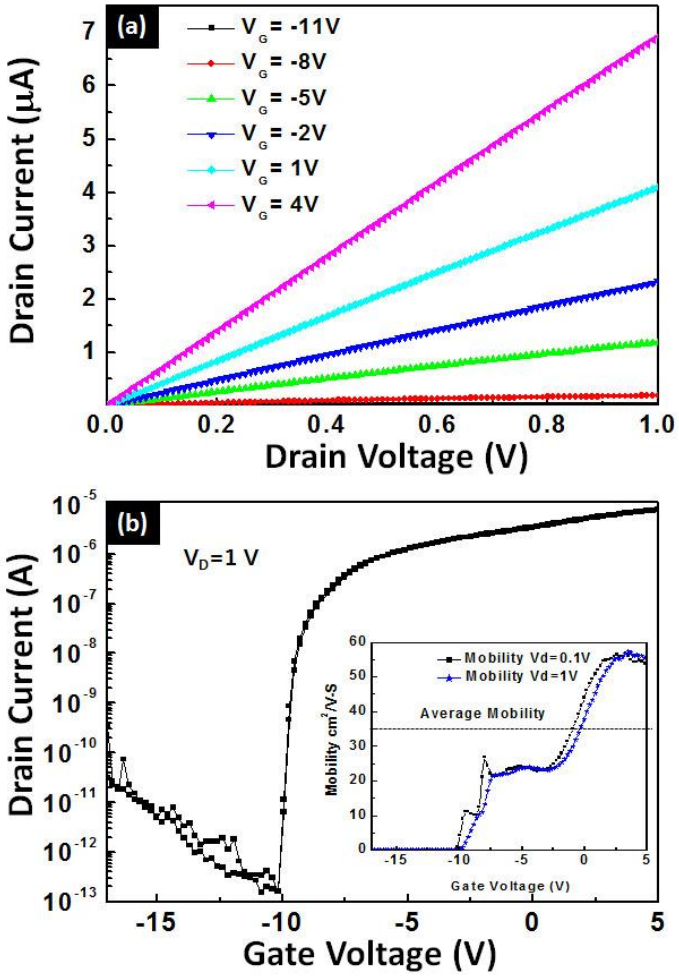

Figure S2. (a) I_D-V_D output curves of our top-gate ZnO NW FET with S and D composed of sputtered Ti/Au (50 nm/50 nm) for ohmic contact; the linear curves show that our S/D contacts using Ti/Au is ohmic. (b) Transfer curves obtained at V_D = 1 V exhibit that our device with ALD Al_2O_3 dielectric has no initial hysteresis, and also demonstrate that its linear mobility (μ) reaches to 57 $cm^2/V{\cdot}s$, as plotted with V_G, along with good S.S value of ~0.12 V/dec. More details on the μ estimation are given by the equations below,

$$\mu = \frac{g_m \times L^2}{C \times V_D} \qquad (1)$$

, where transconductance (g_m) and capacitance (C) are given by Eq. (2) and Eq. (3), respectively.

$$g_m = \frac{dI_D}{dV_G}, \quad (2)$$

$$C = \frac{2\pi\varepsilon_0\varepsilon_{Al_2O_3}L}{\ln(2t/r)} \text{ : (model of cylinder on an infinite metal plate)} \quad (3)$$

, where L (5 μm) is the channel length of the FETs, t (30 nm) is the thickness of the gate insulator layer, r (50 nm) is the wire radius, and $\varepsilon_{Al_2O_3}$ (~7.8) is the dielectric constant of the insulator. Based on above Eq. (1)~(3), a maximum value of the mobility is calculated to be ~57 $cm^2/V{\cdot}s$ under the V_D = 0.1 V/ 1 V conditions while the average mobility is ~40 $cm^2/V{\cdot}s$.

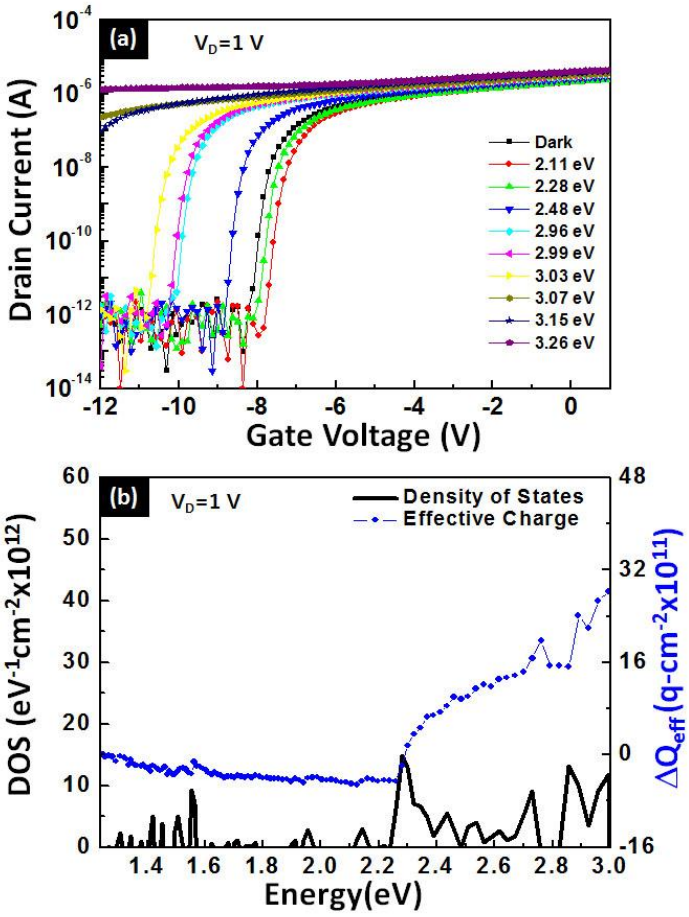

Fig. S3. Another set of ZnO NW FET with the same device structure was characterized for (a) the photo-induced transfer curves showing the V_{th} shift at a drain voltage V_D = 1 V, and for (b) the density of states (DOS) (black) and effective interface charge modulation (blue) spectra under photons of different energies. The main respective results of the transfer curve behavior and DOS location were almost the same as those in Figs. 4a and 4b, although interfacial trap DOS intensities were slightly weaker.

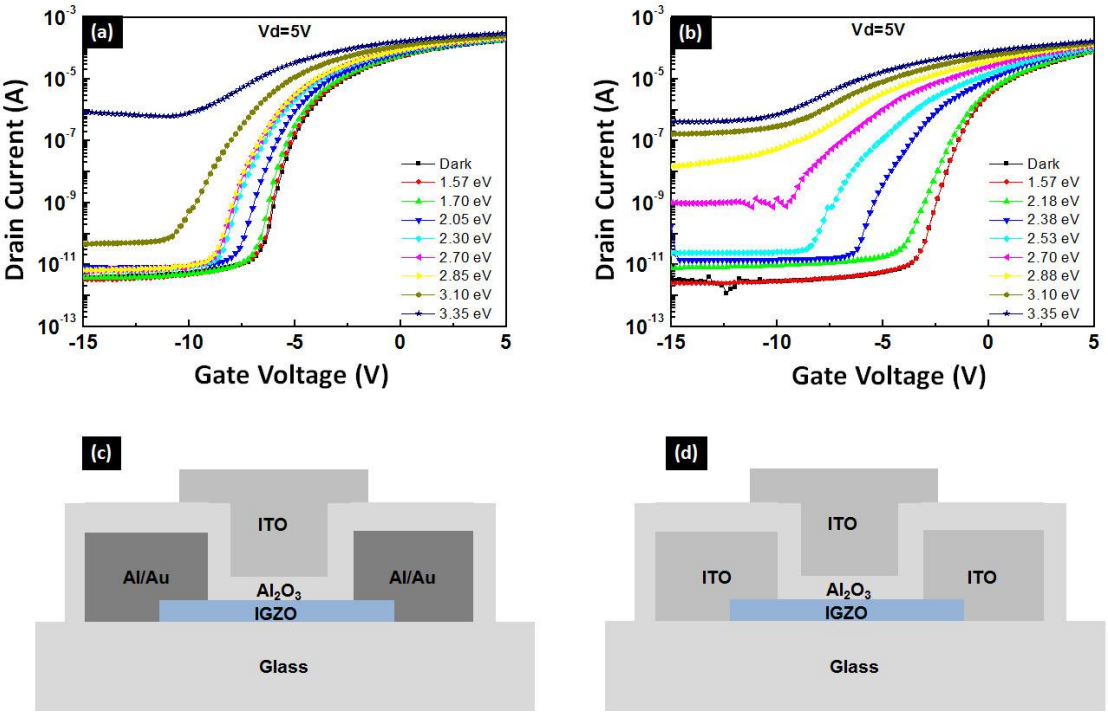

Fig. S4 Transfer curves of InGaZnO TFTs with opaque Au/Ti source/drain (a,c) and of fully transparent TFT with ITO source/drain (b,d) were achieved under visible and UV illuminations. In the case of fully transparent InGaZnO TFT with ITO source/drain, significant off-I_D increase was observed along with a large S.S. change even under visible photons while the other case with Au/Al source/drain showed only minimal increases of those values under visible before near UV photons (~3.06 eV). It is because the bulk region below the ITO drain is strongly influenced by visible photons and electric field (by 5 V). So, the case (a) can be used for the estimation of interfacial trap DOS whereas the case (b) is rather a mixture of bulk and interface traps. Since our ZnO NW FETs display more persistence in maintaining their S.S. shape and off-I_D level, we regard our trap DOS profile in visible photon energy regime as mainly from the traps near the NW/Al_2O_3 interface. In order to more theoretically explain above arguments, we attached the following remarks with two equations for V_{FB} and SS mechanism interpretations;

$$V_{FB} = \Phi_{MS} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx \qquad (1),$$

$$S.S. = \ln 10 \left(\frac{kT}{q} \right) \left[1 + \left(\sqrt{\frac{\varepsilon_{ch} N_{bt}}{kT}} + D_{it} \right) \frac{q^2}{C_{ox}} \right] \qquad (2)^*$$

, where kT = 0.026 eV at room temperature, ε_{ch} and C_{ox} are the respective dielectric constants of channel semiconductor and the electric capacitance of dielectrics, N_{bt} and D_{it} are respectively the near-interface-bulk trap density and the interface trap density-of-states (DOS) at the channel/dielectric interface trap as energy-independent average values; their units are cm^{-3} and cm^{-2} eV^{-1}, respectively. Q_{eff} of the equation (1) (see the main text) is related to the D_{it} and N_{bt} in Eq (2) as the charge density near the interface, and the second term in the large parenthesis of Eq (2) only exists for FETs operating in accumulation mode, extracted from $(\varepsilon_{ch}/L_D)/C_{ox}$ and a poisson's electrostatic equation to express the charging (filling) of near interface traps; it thus includes Debye length (~2 nm in general). This second term is usually ignored in Si-based MOSFET operating in inversion mode. The third term with D_{it} presents the charging of only interface traps, considered important for both inversion and accumulation mode transistors. The D_{it} defined in our main text for the PECCS measurements may thus include N_{bt} near the interface. Therefore, any significant change of S.S. and off-I_D in FETs indicates that other sources of trap-induced current are involved during the device operation. The bulk traps away from the interface would cause such S.S. and off-current increase.

* see J. Electrochem. Soc. 140, 3679-3683 (1993) and R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrated Circuits*, 3rd ed. (Wiley, New York, 2003), pp. 405-409, 397. for more details.

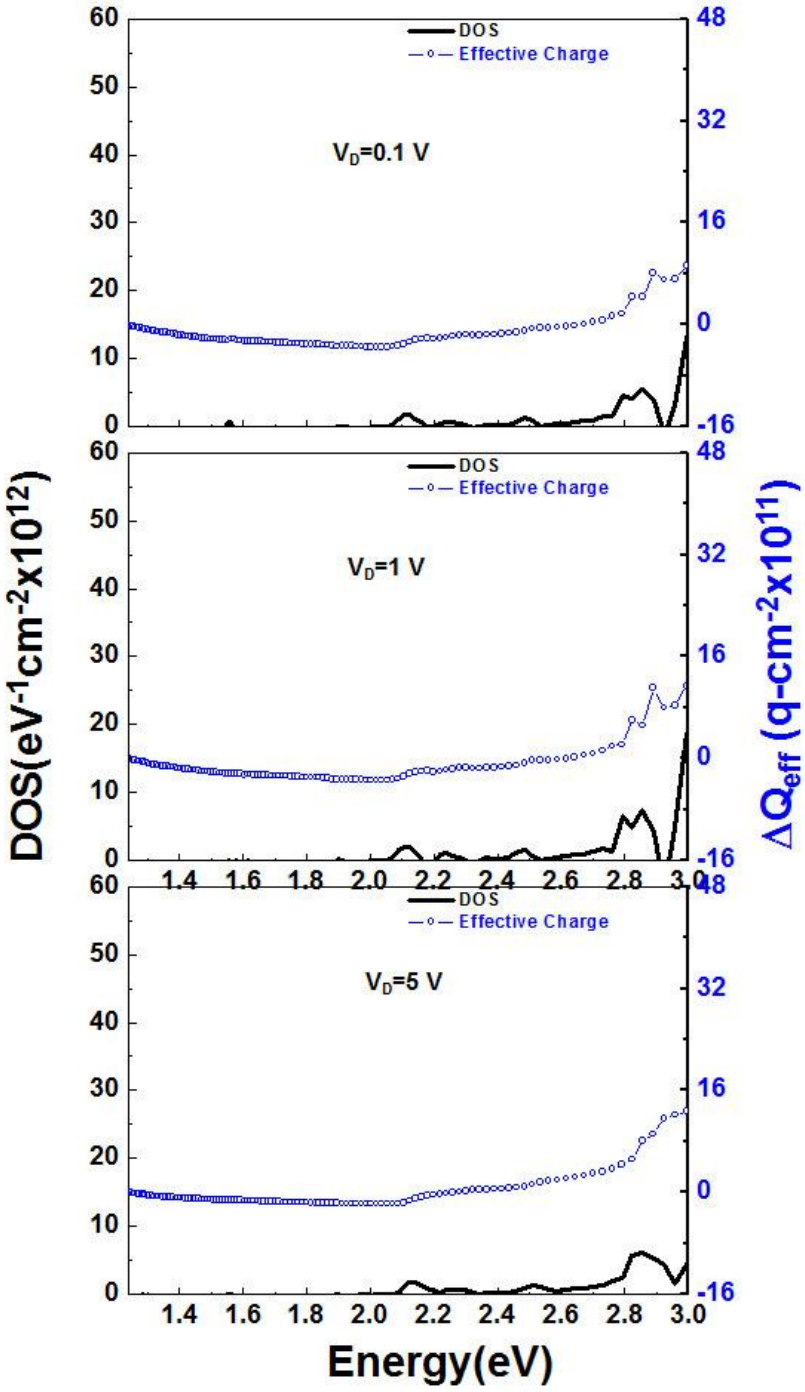

Figure S5. Density of states (DOS) profile of ALD ZnO TFT with low V_D's 0.1 V and 1 V show almost the same profile as that of the case with V_D = 5 V.