Electronic Supplementary Material (ESI) for Nanoscale Advances.

Dual-gated mono-bilayer graphene junction

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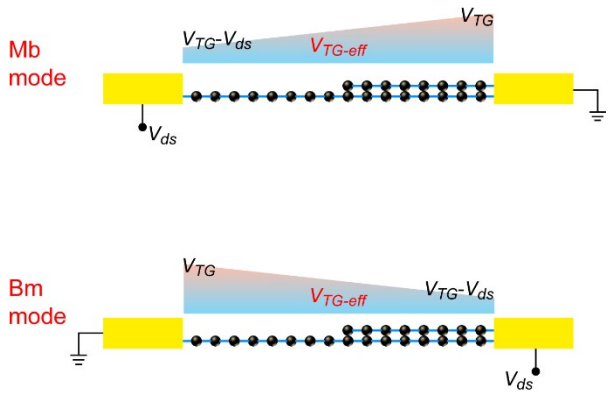

Fig. S1. Configuration of electrical measurement. When bilayer graphene is grounded and the bias voltage V_{ds} is applied on monolayer side, the measurement is defined as "Mb" mode (monolayer graphene has higher electric potential than bilayer graphene). The measurement is defined as "Bm" mode when monolayer graphene is grounded and the bias voltage is applied on bilayer side.

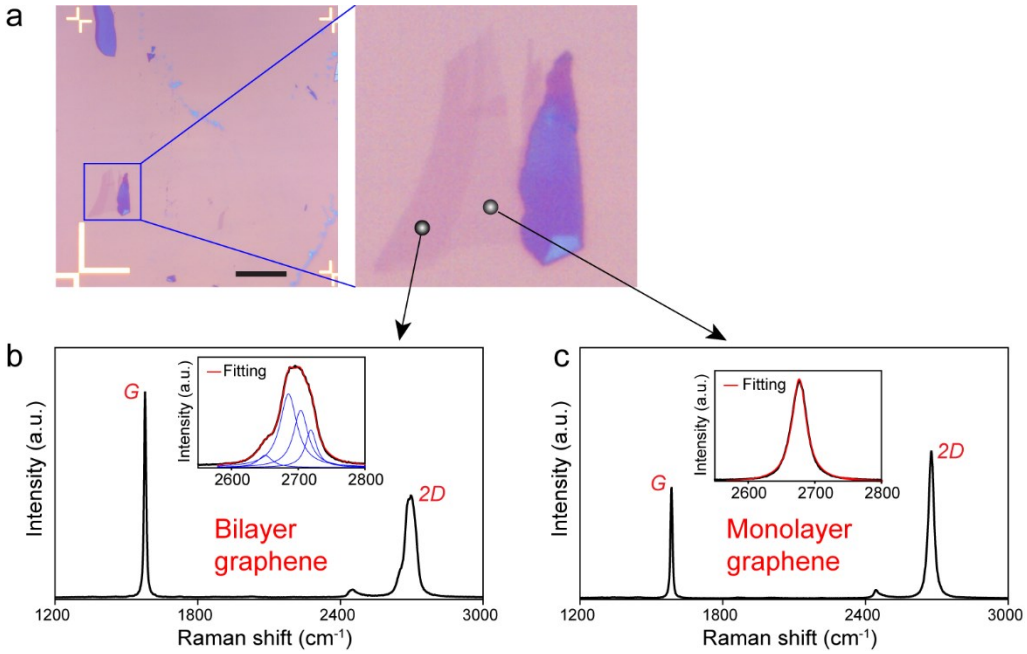

Fig. S2. Raman characterization of a typical graphene flake. (a) Optical microscope image of mechanically exfoliated graphene flakes on Si/SiO_2 wafer. Scale bar: 20 μm. (b, c) Raman spectrum collected at two regions of the flake, the insets are Lorentzian fitting of 2D peaks. The fitting results and 2D/G ratio identify mono- and bilayer graphene.

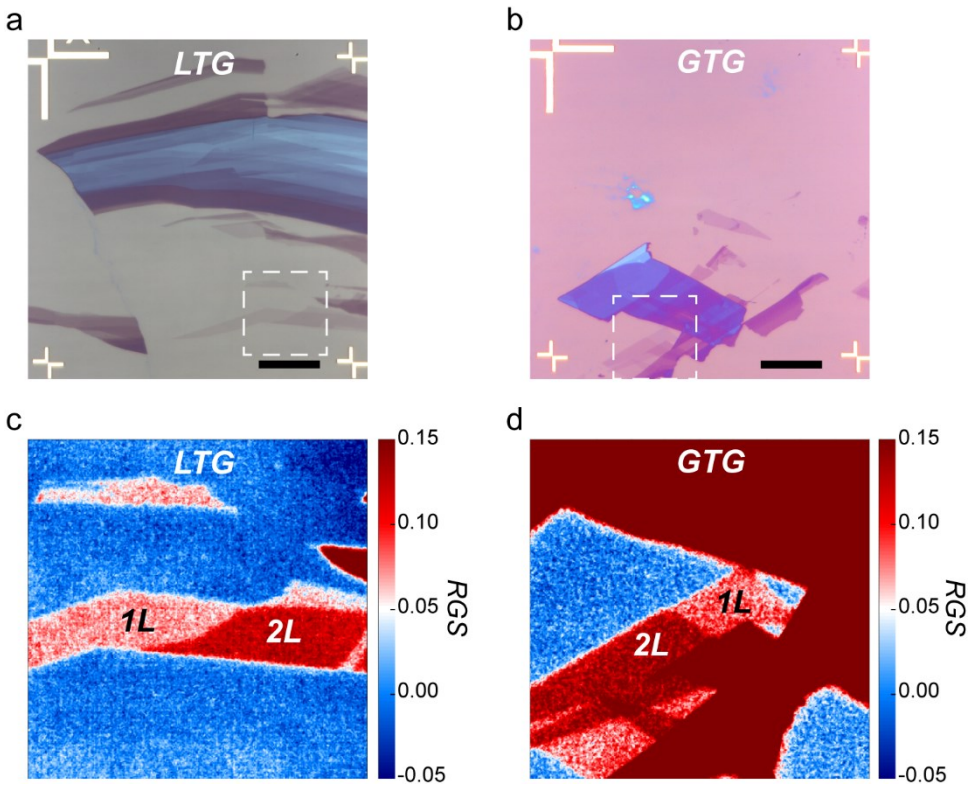

Fig. S3. *RGS* characterization of the graphene flakes used for devices fabrication. (a, b) Optical microscope image of the graphene flakes for LTG (a) and GTG (b) devices described in the context. Scale bar: 20 μm. (c, d) *RGS* mapping of the area marked with white dashed box in (a) and (b). The areas with *RGS* values of ~0.06 and ~0.12 are monolayer (1L) and bilayer (2L) graphene.

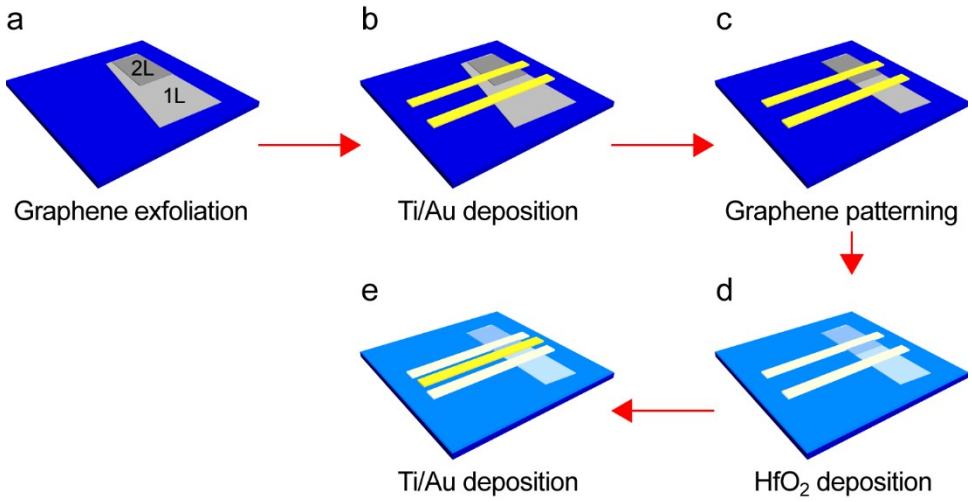

Fig. S4. Schematic of the fabrication process of graphene devices. (a) Graphene flakes are exfoliated and transferred to Si/SiO_2 wafers, and mono-bilayer (1L-2L) graphene junctions are identified by RGS mapping. (b) Source and drain electrodes of Ti/Au are patterned through electron beam lithography, electron beam evaporation and lift-off process. (c) The graphene channel is patterned by electron beam lithography and reactive ion etch. (d) HfO_2 film working as dielectric layer is deposited by atomic layer deposition. (e) Top gate electrode is deposited by the process same to source and drain electrodes.

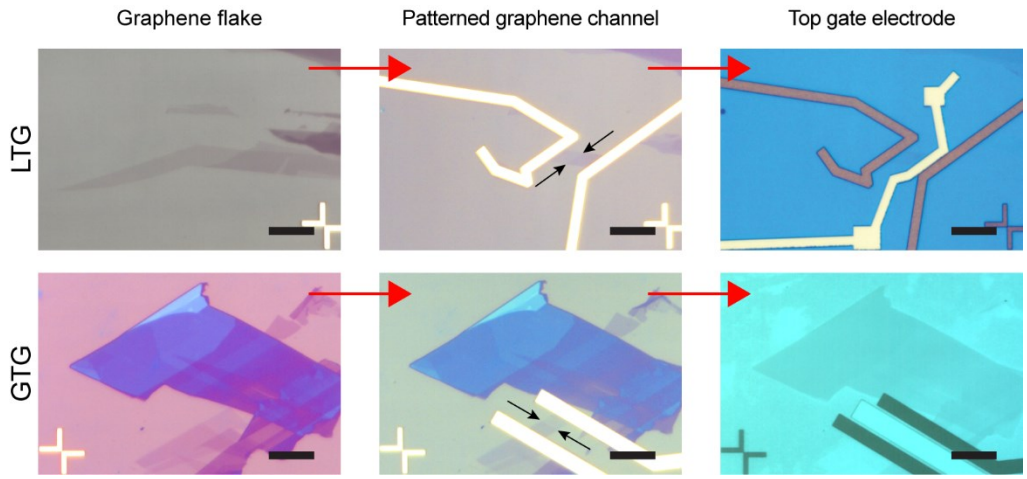

Fig. S5. Optical images of graphene devices fabrication process. The pairs of black arrows indicate the interfaces between mono- and bilayer graphene in the channels. Scale bar: 10 μm.

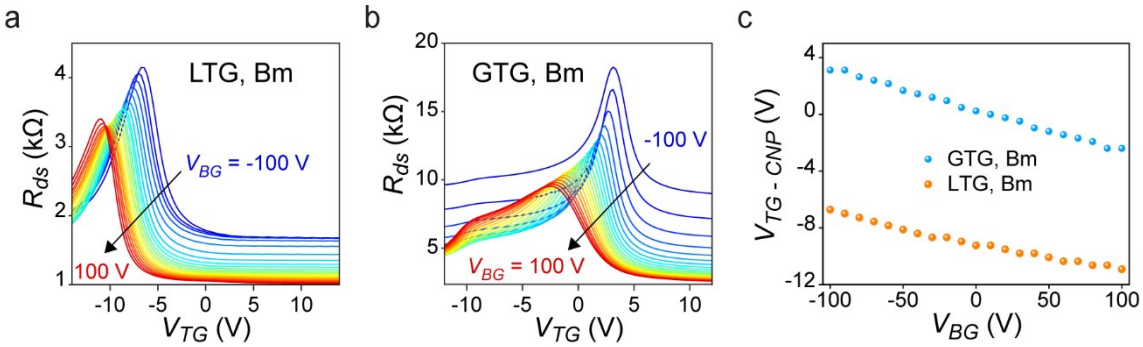

Fig. S6. Transfer curves measured in Bm mode. (a, b) Transfer curves of LTG and GTG devices measured in Bm mode. (c) V_{TG} at charge neutrality point ($V_{TG\text{-}CNP}$) of the transfer curves in (a) and (b).

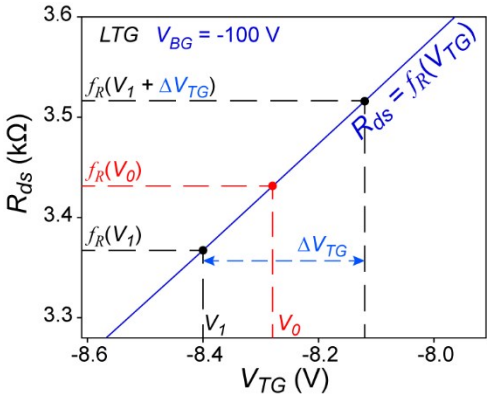

Fig. S7. Calculation of R_{ds} at arbitrary top gate V_0. The blue curve is a small part of the transfer curve defined as $R_{ds} = f_R(V_{TG})$, and the black circles represent practical measurement. Top gate voltages V_1 and $V_1 + \Delta V_{TG}$ are applied in practical transfer curve measurement, since ΔV_{TG} is quite small (0.28 V for LTG device measurement and 0.24 V for GTG device measurement), the transfer curve between V_1 and $V_1 + \Delta V_{TG}$ are assumed linear: $\frac{f_R(V_1 + \Delta V_{TG}) - f_R(V_1)}{\Delta V_{TG}} = \frac{f_R(V_0) - f_R(V_1)}{V_0 - V_1}$. Therefore, R_{ds} at top gate V_0 is calculated with this formula: $f_R(V_0) = \frac{f_R(V_1 + \Delta V_{TG}) - f_R(V_1)}{\Delta V_{TG}} \cdot (V_0 - V_1) + f_R(V_1)$.

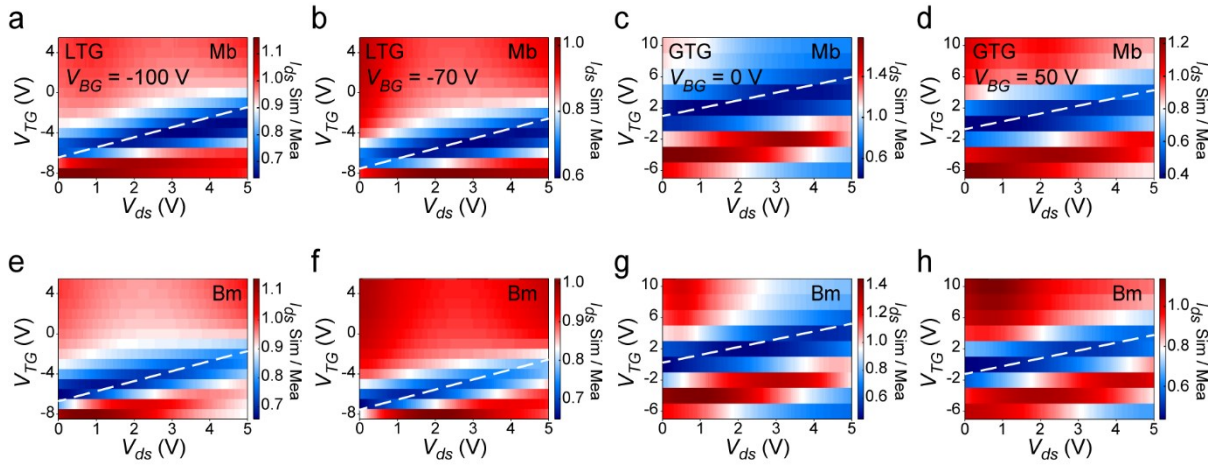

Fig. S8. I_{ds} Sim/Mea ratio. (a-d) Ratio of simulated *Ids* to the values measured in Mb mode at various V_{TG}. (e-h) The ratio of *Ids* in Bm mode corresponding to the conditions in (a-d). The white dashed lines indicate where V_{TG} - V_{ds} = $V_{TG\text{-}CNP}$. It's apparent that the simulation accuracy is well acceptable at (V_{TG}, V_{ds}) combinations far from the white lines, while much worse at (V_{TG}, V_{ds}) combinations near the white lines.