Supporting Information: Multi-scale analysis of radio-frequency performance of 2D-material based field-effect transistors

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I. Self-consistent numerical solver

The device electrostatics and transport are self-consistently solved so to obtain the potential, the Fermi level, and the carrier concentration at each position of the spatial grid, as well as the current through the semiconductor layer. A schematic view of the device is depicted in Figure S.1.

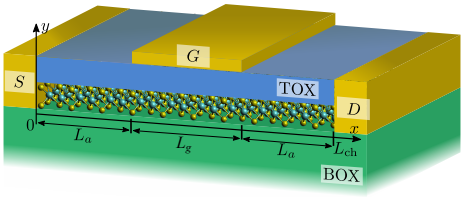

FIG. S.1: Schematic of the 2DM-based FET showing the device geometry, the coordinate reference system, as well as the lengths associated to the channel and access regions. The gate, drain and source terminals are labeled as G, D and S, respectively.

The inputs for these calculations are the semiconductor properties (density of states, mobility, doping) as well as the insulator ones (dielectric constant, trap energetic profiles), and the device bias conditions. In particular the two-dimensional Poisson equation is numerically treated in a cross-section of the device, assuming invariance along the width:

$$\nabla\left(\varepsilon(x,y)\nabla V(x,y)\right) = -\rho(x,y) \tag{S.1}$$

where ϵ is the dielectric constant, ρ is the charge density, comprising mobile carriers, fixed charges and traps, and V is the potential.

As for the transport, a drift-diffusion regime is considered along one dimension, assuming that the width of the 2D material sample is large enough, so not to experience any border effect. In the case of electrons the current density is given by:

$$J_{\mathrm{n}} = qn\mu_{\mathrm{n}}\nabla_x V + qD_{\mathrm{n}}\nabla_x n \tag{S.2}$$

where q is the net electron charge, D_{n} the diffusion coefficient, μ_{n} the electron mobility, n the carrier longitudinal density and J_{n} the current density. An equivalent expression is used for holes. The steady-state continuity equation is:

$$\nabla_x J = 0 \tag{S.3}$$

The impact of non-idealities is also included in the simulations. In particular, two spoiling effects are considered: interface traps and electric field dependent mobility. For the former, an arbitrary energetic profile can be defined to evaluate the surface charge density associated to a certain insulator interface:

$$Q_{\mathrm{it}} = -q \int_0^{\mathcal{E}_{\mathrm{C}}} D_{\mathrm{it,A}}\left(\mathcal{E}\right) f\left(\mathcal{E}\right) d\mathcal{E} + q \int_{\mathcal{E}_{\mathrm{V}}}^0 D_{\mathrm{it,D}}\left(\mathcal{E}\right) \left[1 - f\left(\mathcal{E}\right)\right] d\mathcal{E} \tag{S.4}$$

where Q_{it} is the surface density charge, $\mathcal{E}$ the energy referred to the intrinsic Fermi level ($E - E_{\mathrm{i}}$), $D_{\mathrm{it,A}}$ ($D_{\mathrm{it,D}}$) the density of acceptor (donor) traps, $f(E)$ the Fermi function, and $\mathcal{E}_{\mathrm{C}}$ ($\mathcal{E}_{\mathrm{V}}$) the conduction (valence) band edge. For the mobility degradation originated by the electric field, the following relation is employed[1]

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0}{v_{sat}} \left|\mathbf{E}_x\right|\right)^{\beta}\right]^{1/\beta}} \tag{S.5}$$

where μ_0 is the low field mobility, v_{sat} is the saturation velocity, β is the saturation coefficient and $\mathbf{E}_x$ electric field along the longitudinal coordinate. This expression is applied to both electron and hole mobilities.

II. Access and contact resistances

In the intrinsic device, the semiconductor layer can be split into three regions: (i) source access region, (ii) channel and (iii) drain access region. The resistance of each of these regions can be calculated as:

$$R_{i,\mathrm{acc}} = \int_{L_1}^{L_2} \frac{1}{q\left(\mu_{\mathrm{n}} n_{\mathrm{L}} + \mu_{\mathrm{p}} p_{\mathrm{L}}\right)} dl \tag{S.6}$$

where $L_1 = 0, L_{\mathrm{a}}$, and $L_{\mathrm{a}} + L_{\mathrm{g}}$; and $L_2 = L_{\mathrm{a}}, L_{\mathrm{a}} + L_{\mathrm{g}}$, and $2L_{\mathrm{a}} + L_{\mathrm{g}} = L_{\mathrm{ch}}$; are the integration limits for the source access, gate-controlled channel and drain access resistance calculation respectively (see Figure S.1 for a detailed representation). L_{a}, L_{ch}, L_{g}, stand for the access region, the channel and the gate lengths, respectively.

In addition to the intrinsic device, we also consider the extrinsic source and drain resistances (R_{s} and R_{d}) due to the metal-2DM contacts. At the numerical solver level, they are included in the structure as doped regions with fixed and limited conductivity placed at each side of the semiconductor layer.

III. Dynamic operation: terminal charges and intrinsic capacitance scheme

In order to compute the dynamic operation of a three-terminal device, the charge associated to each terminal is evaluated to later determine the intrinsic capacitances[2]. Thus, the charges

associated to the gate, drain and source terminals are calculated following the Ward-Dutton charge partition scheme, which ensures charge conservation[3]:

$$Q_{\mathrm{g}} = W \int_0^{L_{\mathrm{ch}}} -(p(x) - n(x))dx \tag{S.7}$$

$$Q_{\mathrm{d}} = W \int_0^{L_{\mathrm{ch}}} \frac{x}{L_{\mathrm{ch}}}(p(x) - n(x))dx \tag{S.8}$$

$$Q_{\mathrm{s}} = W \int_0^{L_{\mathrm{ch}}} \left(1 - \frac{x}{L_{\mathrm{ch}}}\right)(p(x) - n(x))dx \tag{S.9}$$

where g, d and s indicate that the charge is associated to gate, drain and source respectively. Then, we compute the intrinsic capacitances of a three-terminal device as:

$$C_{ij} = \begin{cases} \frac{\partial Q_i}{\partial V_j} & i = j \\ -\frac{\partial Q_i}{\partial V_j} & i \neq j \end{cases}, \quad i, j = g, d, s \tag{S.10}$$

IV. Small-signal approximation

When electronic devices operate in analog and radio-frequency applications, their terminals are biased with a DC voltage over which a time-varying signal is superimposed. If the amplitude of the time-varying signal is small enough, the resulting current and charge variations can be expressed in terms of it using linear relations. This way, a non-linear device can be treated as a linear circuit with conductance and capacitance elements connected forming a lumped network.

As depicted in Figure 2 of the manuscript, the model considers the capacitances C_{gd}, C_{dg}, C_{sd} and C_{gs}. The latter cannot be evaluated using Eq. (S.10) as in the simulations V_{s} is defined as the reference potential. To overcome this issue, we use the charge conservation condition on the gate charge[2].

$$\sum_j \frac{\partial Q_g}{\partial V_j} = 0 \Rightarrow C_{gs} = C_{gg} - C_{gd} \tag{S.11}$$

The resistances required by the small-signal model are obtained as exposed before in (S.6), except for R_{g} that is considered as an input parameter. Once the values of the discrete elements are calculated, the small-signal model can be used to evaluate the two main figures of merit for radio-frequency applications, the cut-off frequency f_{T}, and the maximum oscillation frequency f_{max}.

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