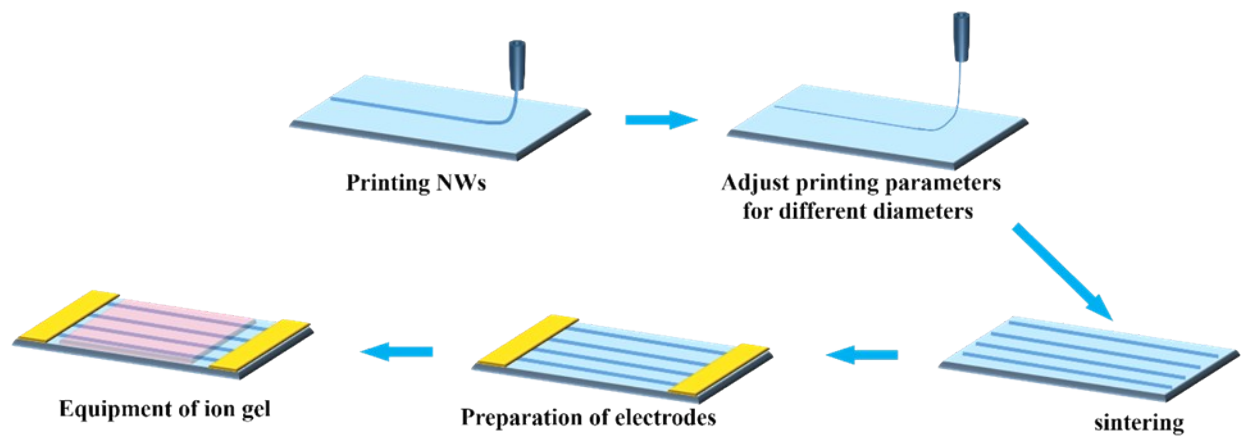


# Digitally-aligned ZnO nanowire array based synaptic transistors with intrinsically controlled plasticity for short-term computation and long-term memory

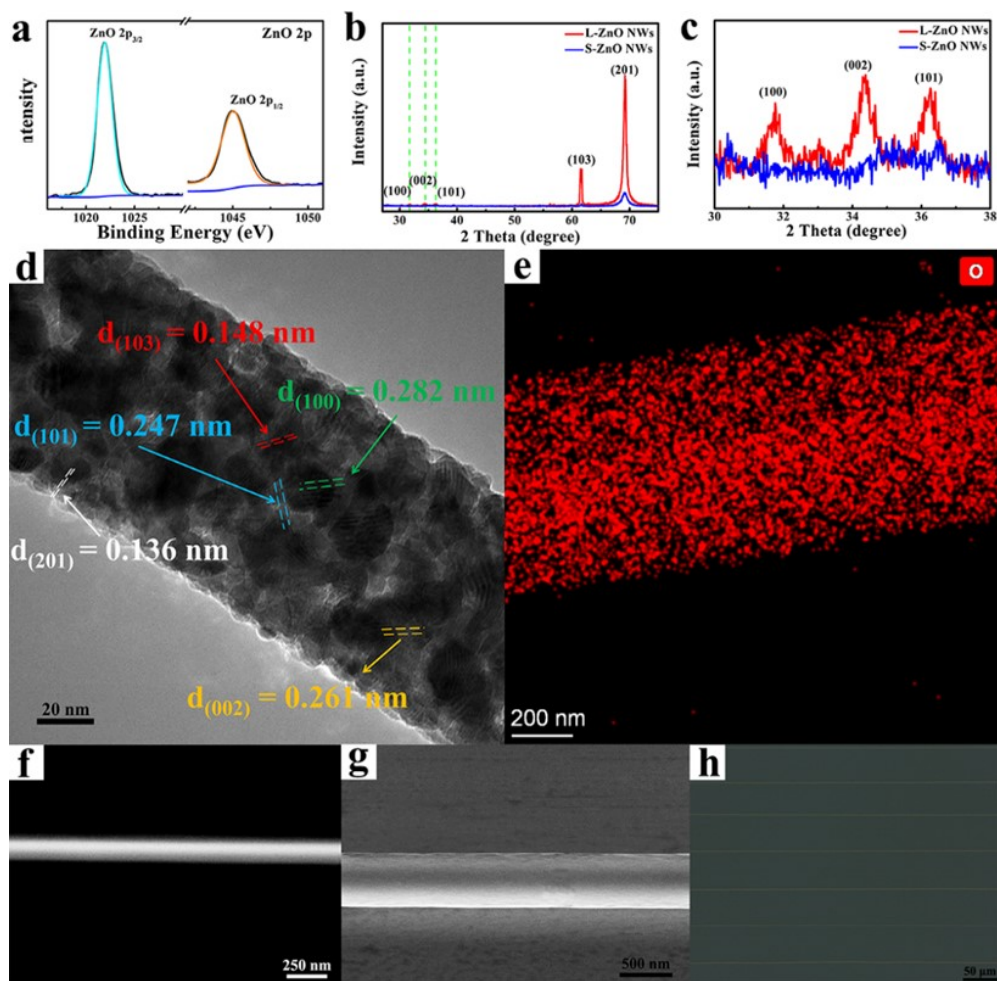
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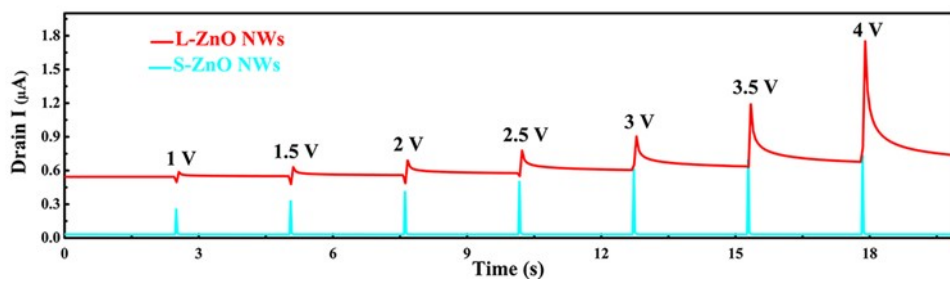
Institute of Optoelectronic Thin Film Devices and Technology, Key Laboratory of Optoelectronic Thin Film Devices and Technology of Tianjin, Engineering Research Center of Thin Film Photoelectronic Technology, Ministry of Education, National Institute of Advanced Materials, Nankai University, Tianjin 300350, China



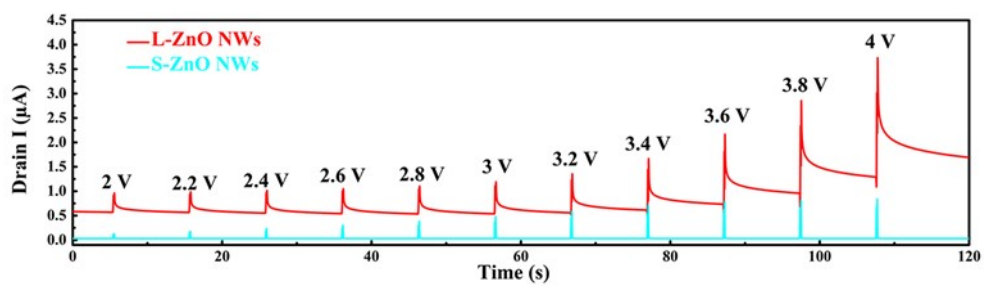
**Figure S1.** Schematic diagram of the preparation process of S-ZnO NWs and L-ZnO NWs.



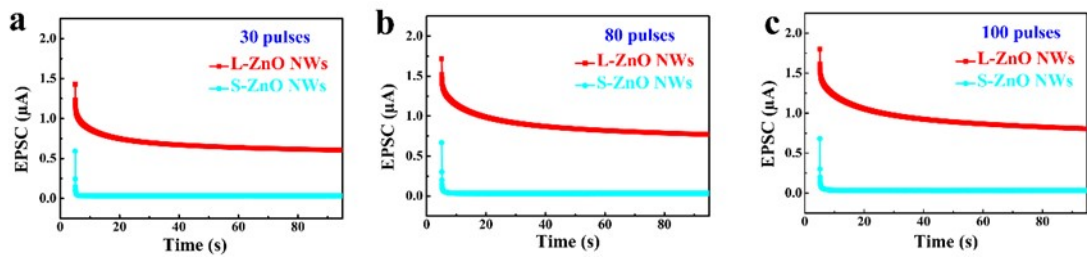
**Figure S2.** (a) High-resolution XPS spectra of Zn 2p in ZnO NWs. (b) XRD of S- and L-ZnO NWs. (c) Partial enlargement of XRD of S- and L-ZnO NWs. (d) High-resolution TEM image of S-ZnO NWs. (e) Elemental mapping of ZnO NWs for O. SEM images of diameter of (f) S-ZnO NWs and (g) L-ZnO NWs. (h) OM of ZnO NWs array.



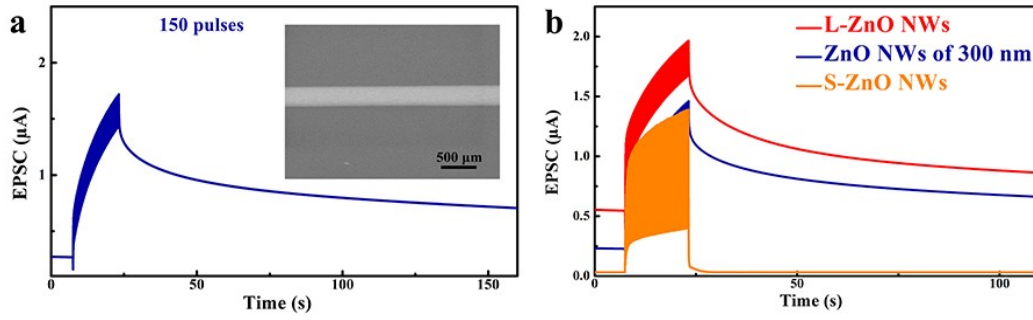
**Figure S3.** Contrast of SVDP between S-ZnO NWs and L-ZnO NWs.



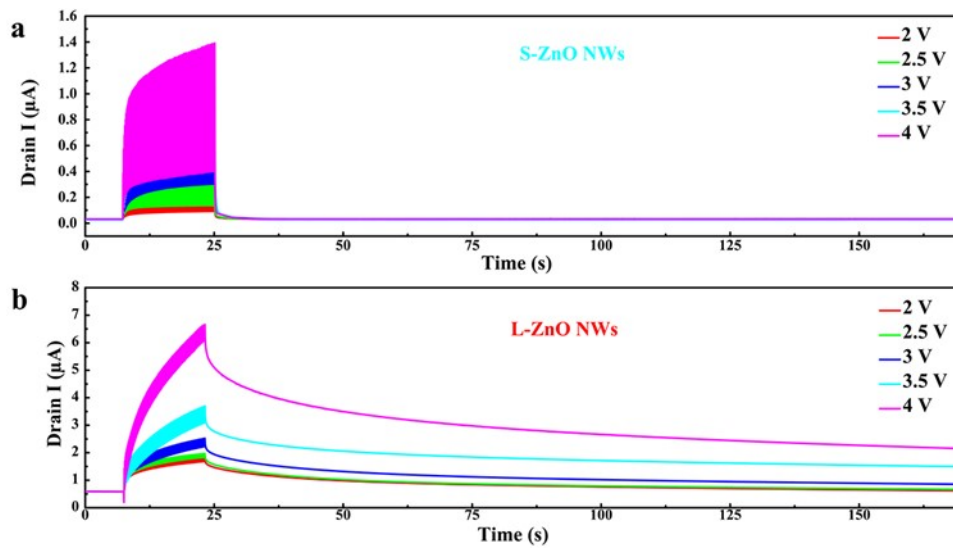
**Figure S4.** Contrast of PPF of different voltage between S-ZnO NWs and L-ZnO NWs.



**Figure S5.** The retention curve of synaptic weight of S-ZnO NWs and L-ZnO NWs with different numbers: (a) 30, (b) 80 and (c) 150.



**Figure S6.** (a) The LTP of ZnO-NW STs of 300 nm. (b) Postsynaptic responses of S-ZnO-NW STs, ZnO-NW STs of 300 nm and L-ZnO-NW STs after 150 presynaptic inputs (3 V).



**Figure S7.** Contrast of LTP between (a) S-ZnO NWs and (b) L-ZnO NWs with 150 gate pulses under different voltages (2 V, 2.5 V, 3 V, 3.5 V and 4 V).