Electronic Supplementary Material (ESI) for Materials Chemistry Frontiers.

Supporting information

A novel 3D porous electrode of polyaniline and PEDOT:PSS coated SiNWs for low-cost and high-performance supercapacitors

Xiaojuan Shen,*[a] Xuan Zhang,[a] Tongfei Wang,[a] Songjun Li,*[a] Zhaoqiang Li*[b]

[a] *Research School of Polymeric Materials, School of Materials Science & Engineering, Jiangsu University, Zhenjiang, Jiangsu Province, 212013, China.*
[b] *Department of Chemical Engineering, University of Waterloo, Waterloo, ON N2L 3G1, Canada.*

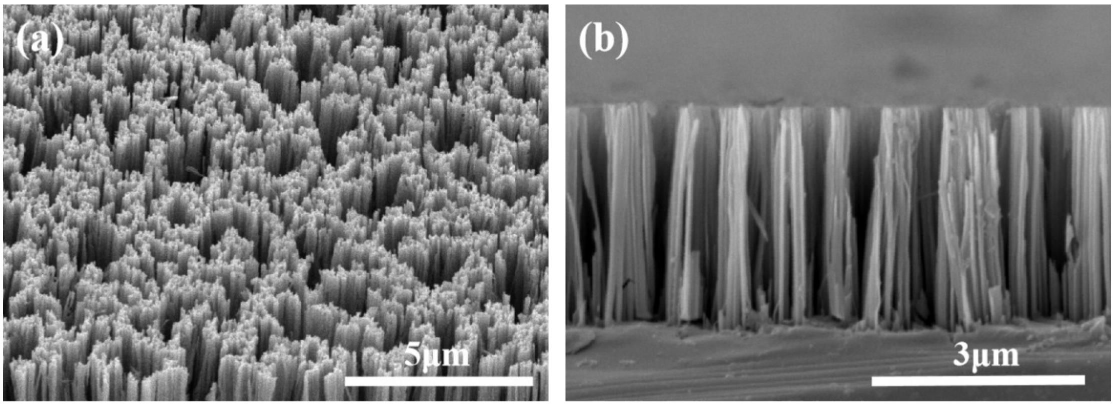

Fig. S1 SEM image of SiNWs etched by MACE method for 60 min on EG Si wafer from (a) 45 title and (b) cross-section.

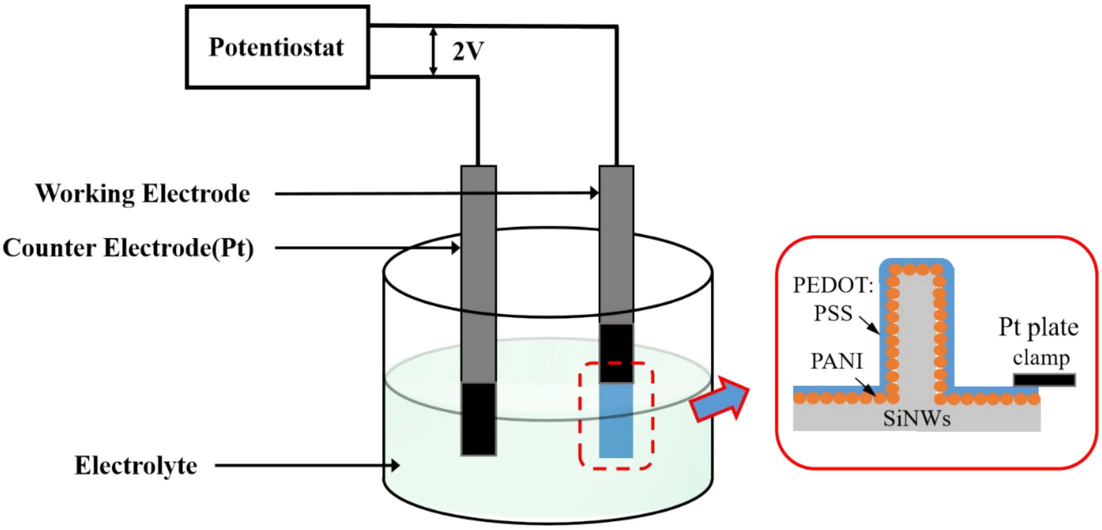

Fig. S2 Schematic of the electropolymerization system. The SiAN substrate coated with the PEDOT:PSS layer is used as the working electrode. Pt plate clamp connects with the surface where PANI and PEDOT:PSS decorate on the SiNWs substrate.

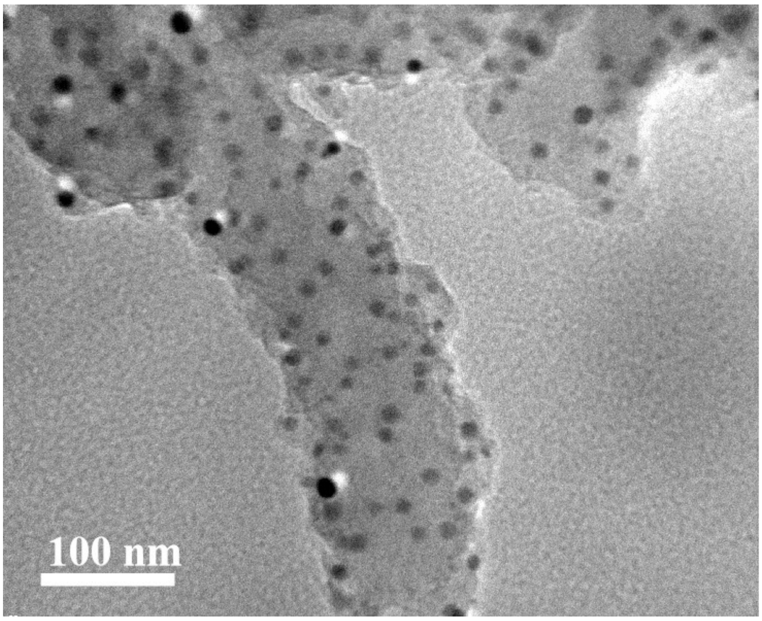

Fig. S3 TEM image of PANF.

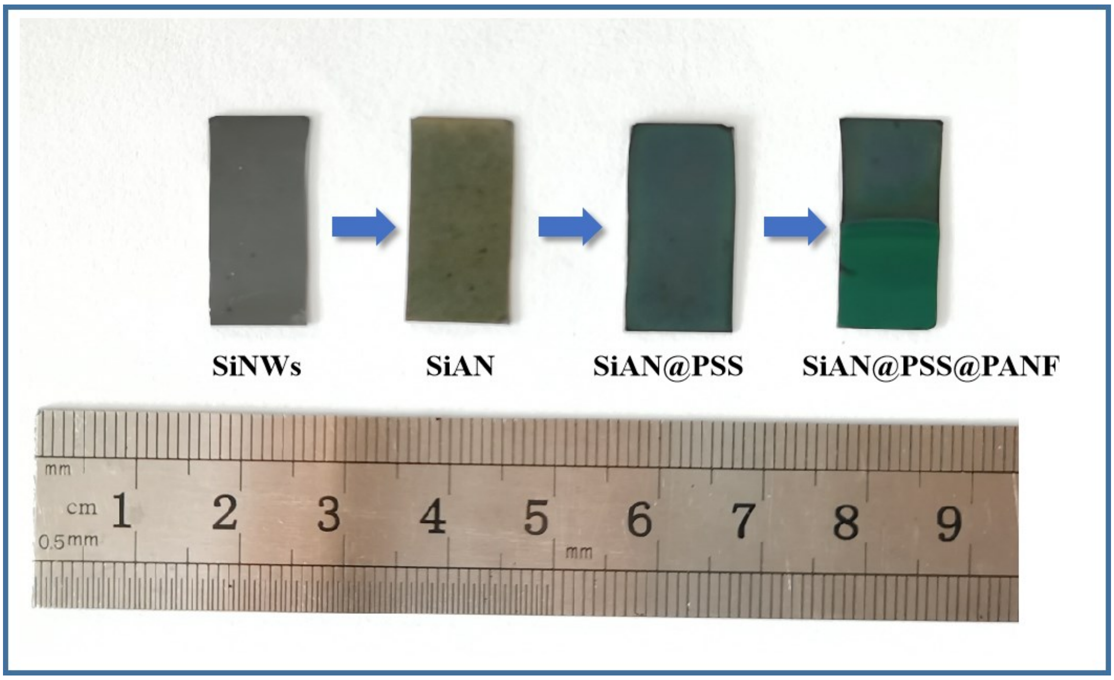

Fig. S4 Photographs of the different fabricated Si substrates. The deposition time of PANF is 5 min.

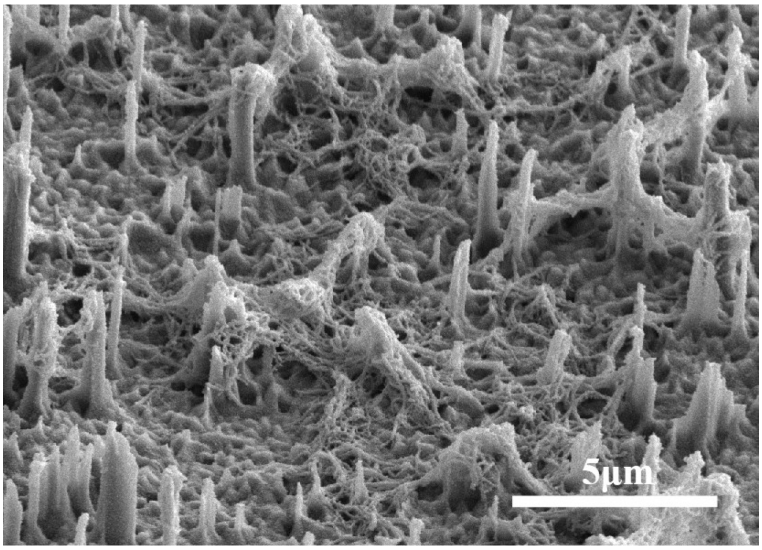

Fig. S5 SEM image of polyaniline electrodeposited on the naked SiNWs substrate using the Ag as the rear electrode with the electrodeposition time of 10 min.

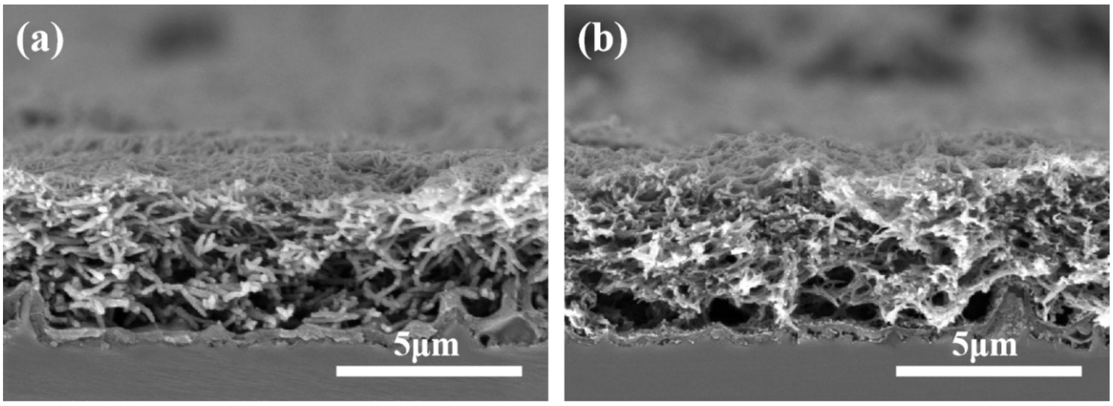

Fig. S6 Cross-section SEM images of PANF synthesized on the SiAN@PSS substrates incorporated (a) without and (b) with graphene.

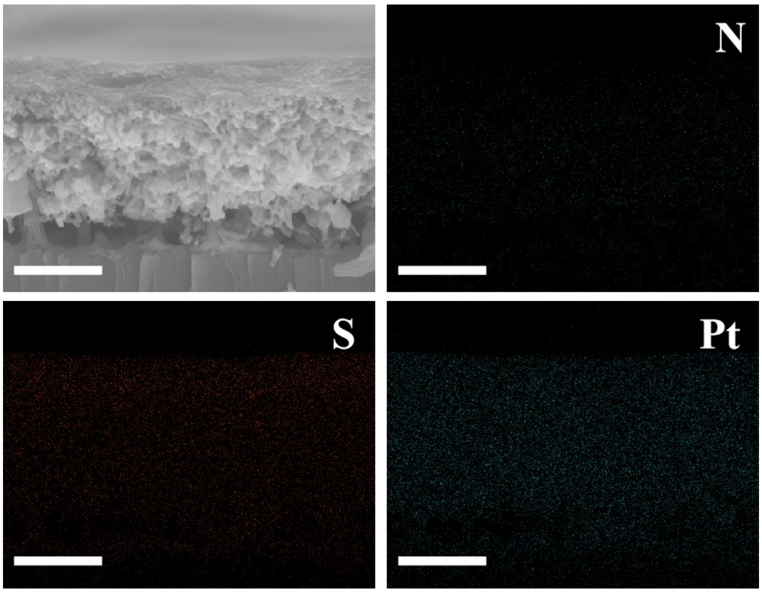

Fig. S7 SiAN@PSS@GP coated with H_2PtCl_6 doped PEDOT:PSS layer and the corresponding cross-section element mappings of N, S and Pt. The electrodeposition time of GP is 8 min. The scale bar is 5 μm.

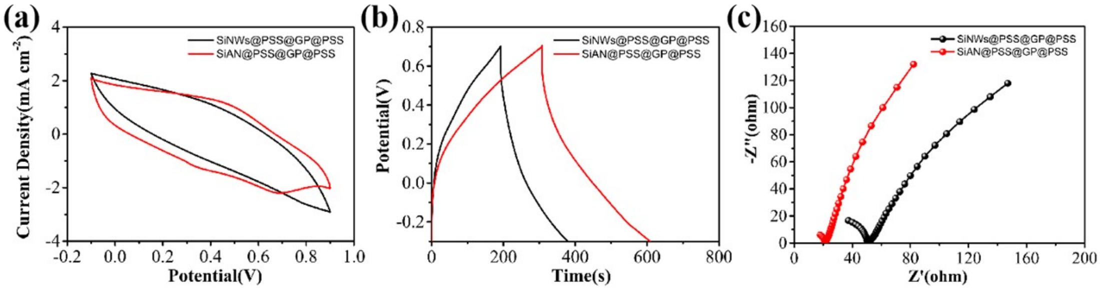

Fig. S8 (a) CV curves measurement at 10 mV s^{-1}, (b) GCD measurement at the current density of 1mA cm^{-2} and (c) Nyquist plots of the electrodes fabricated with PANI (SiAN@PSS@GP@PSS) and without PANI (SiNWs@PSS@GP@PSS) between the PEDOT:PSS and SiNWs. The electrodeposition time is 8 min.

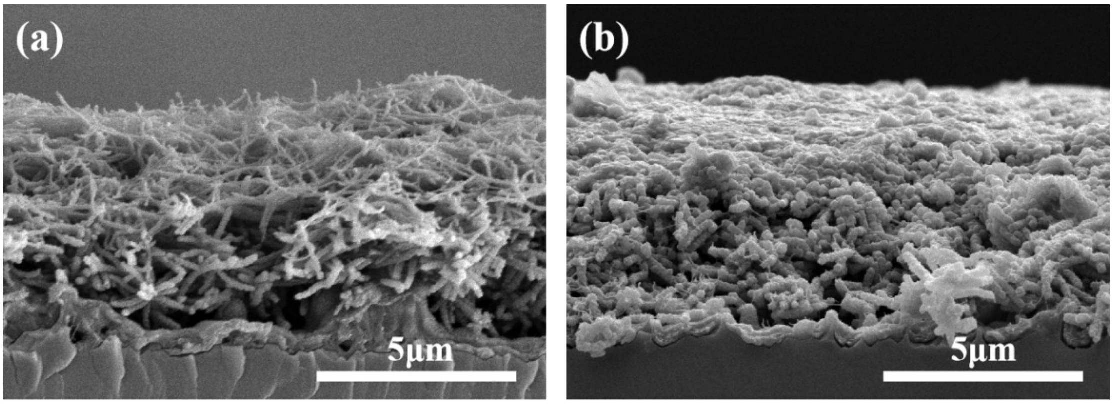

Fig. S9 The cross-section SEM images of PANF synthesized on (a) SiAN@PSS substrate and (b) SiNWs@PSS substrate.

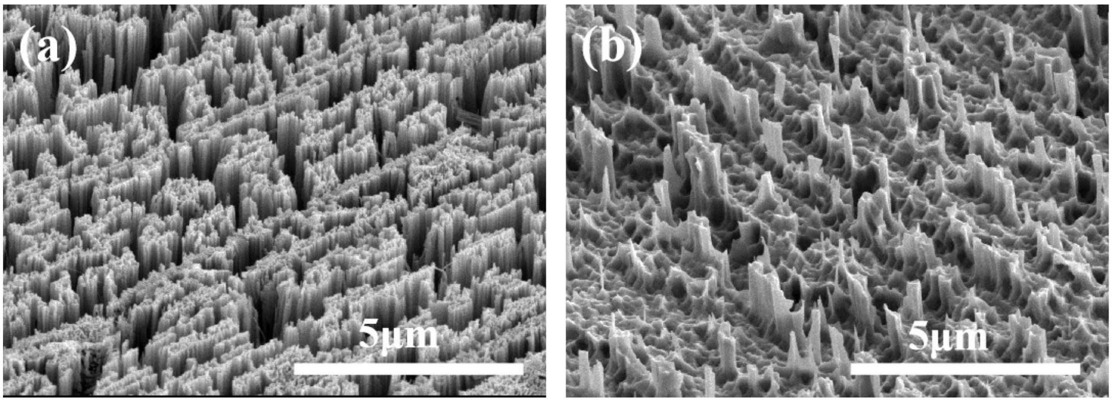

Fig. S10 SEM images of (a) pristine SiNWs synthesized from SG Si wafer with MACE method for 30 min, (b) SiNWs treated by TMAH solution for 40 min.

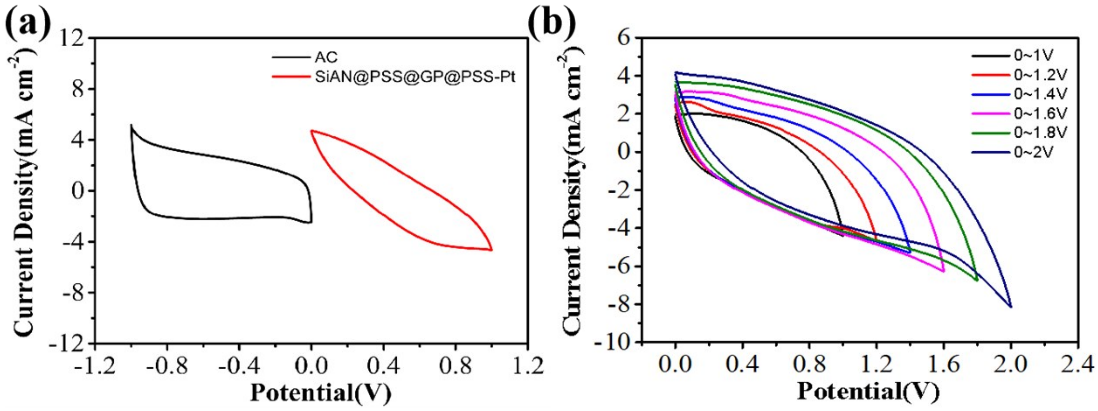

Fig. S11 (a) CV curves obtained for AC and SiAN@PSS@GP@PSS-Pt electrodes at the scan rate of 10 mV s^{-1} and (b) the corresponding CV curves of the ASC in aqueous electrolyte for different potential windows at a scan rate of 20 mV s^{-1}.

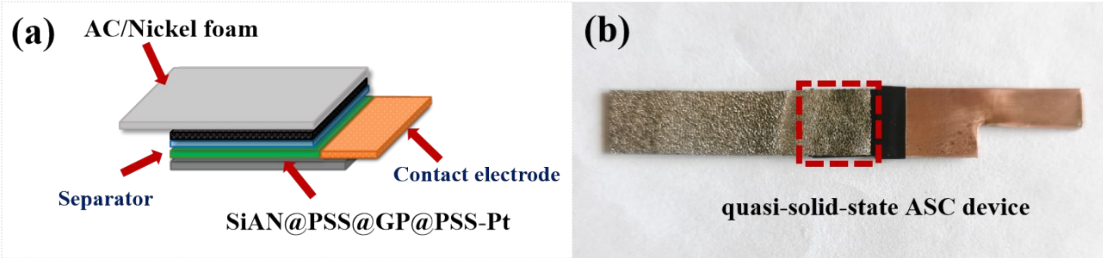

Fig. S12 (a) A schematic illustration of the fabricated quasi-solid-state ASC device and (b) an optical image of the device.

Table S1 Capacitance comparison of SiAN@PSS@GP@PSS-Pt electrode with the previously reported on-chip supercapacitor electrodes using 3D Si nanostructure.

Type	Electrode material	Si growth	Capacitance ($mF\ cm^{-2}$)	Test Condition	Device configuration	Electrolyte	Refs
1	SiNWs	CVD	0.046	50mV s^{-1},0.7V	2-electrode	IL/PC[(a)]	1
	SiNWs	CVD	0.013	100mV s^{-1},1.5V	2-electrode	IL	2
	SiNTrs	CVD	0.35	1mA cm^{-2},4 V	2-electrode	IL	3
	Oxidized-SiNWs	Etching	0.404	50mV s^{-1},1.5V	3-electrode	IL	4
2	SiNWs/PEDOT	CVD	9	0.1mA cm^{-2},1.5V	2-electrode	IL	5
	PEDOT@SiNWs	Etching	115	0.5mA cm^{-2},1V	3-electrode	IL	6
			39.2	0.25mA cm^{-2},1V	2-electrode		
	SiNTrs/PPy	CVD	14	1mA cm^{-2},1.5V	2-electrode	IL	7
	SiNWs/RuOx	Etching	19	5mV s^{-1},1V	3-electrode	Na_2SO_4	8
			6.5	2mV s^{-1},1V	2-electrode	PVA/H_2SO_4	
	SiNWs/MnO_2	CVD	13	0.4mA cm^{-2},2.2V	3-electrode	$LiClO_4$-IL	9
	In_2O_3/mesoporous Si	CVD	1.36	10mV s^{-1},1.2V	3-electrode	Na_2SO_4	10
	C@SiNWs	Etching	25.64	0.1mA cm^{-2},0.7V	3-electrode	Na_2S0_4	11
	Diamond/SiNWs	CVD	1.9	0.1mA cm^{-2},4V	2-electrode	IL	12
	rGO-SiNWs	HWCVP	0.24	10μA cm^{-2}, 1.3V	3-electrode	IL	13
	C/PSiNWs	Etching	190	1mA cm^{-2}, 0.8V	3-electrode	IL	14
3	Si@Ti@TiN	Etching	43.8	1mA cm^{-2},0.8V	2-electrode	H_2SO_4	15
	PEDOT/D@ SiNWs	CVD	9.5	0.1mA cm^{-2},2.5V	2-electrode	IL	16
	SiNWs/PEDOT@ PPy	Etching	106	0.5mA cm^{-2},1.5V	3-electrode	IL	17
			46.5	0.5mA cm^{-2},1.5V	2-electrode		
	Al_2O_3/PEDOT:PSS /SiNWs	CVD	8.4	20mV s^{-1},1.2V	3-electrode	Na_2SO_4	18

SiNWs/C/MnOx	Etching	381	12.5mA cm^{-2},2.95V	3-electrode	IL	19
SiNWs/NC@NiO	Etching	110	1mA cm^{-2}, 0.4V	3-electrode	KOH	20
Si-TNR/TiN/MnO_2	Etching	125 39.7	0.2mA cm^{-2},3.6 V 0.25mA cm^{-2},0.8V	3-electrode 2-electrode	Na_2SO_4 Na_2SO_4	21
SiNWs/C/NCO	Etching	1650 560	3mA cm^{-2},0.45V 1mA cm^{-2},0.8V	3-electrode 2-electrode	KOH KOH	22
PANI/GNW/SiNWs	Etching	185	10mV s^{-1},1V	3-electrode	H_2SO_4	23
SiAN@PSS@GP@PSS-Pt	Etching	790.89 (EG) 718.85 (SG)	1mA cm^{-2},1V	3-electrode	Na_2SO_4	This work

1: Pristine Si, 2: Binary composite, 3: Ternary composite.

(a)IL: ionic liquid, PC: Polycarbonate.

Table S2 Comparison of energy density and power density of SiAN@PSS@GP@PSS-Pt//AC with the previous reported Si-based devices.

System	Electrolyte	E ($mWh\ cm^{-2}$)	P ($mW\ cm^{-2}$)	Refs
Graphene/Si	$PYR_{13}TFSI$	0.004	4	24
PEDOT/PPy/SiNWs	$PYR_{13}TFSI$	0.0146	0.315	17
In_2O_3/mesoporous Si	1M Na_2SO_4	0.00059	0.03	10
Diamond/SiNWs	PMPyrrBTA	0.00013	0.15	25
Diamond/SiNWs	40%PMPyrrTFSI/PC	0.023	0.94	26
PPy/SiNTrs	$PYR_{13}TFSI$	0.004	0.8	7
Al_2O_3/PEDOT:PSS/SiNWs	0.5 M Na_2SO_4	0.0023	4.1	18
Ru/SiNWs	0.5 M H_2SO_4/PVA	0.035	0.5	27
RuO_2/SiNWs	H_2SO_4/PVA	0.0004	0.03	8
C@SiNWs	1 M Na_2SO_4	0.04	0.00175	11
MnOx/C/PSiNW	0.1M EMIM-TFSI	0.555	0.48	19
PEDOT/D/SiNWs	$N_{1114}TFSI$	0.007	1.3	16
GNW/RuOx/Si	H_3PO_4/PVA	0.0151	2.49	28
PEDOT coated SiNWs	$N_{1114}TFSI$	0.0092	0.11	6
Graphene/PANI/SiNWs	1M H_2SO_4	0.0117	0.42	29
SiAN@PSS@GP@PSS-Pt	1M Na_2SO_4	0.194	0.850	This work
//AC	PVDF-HFP/IL	0.063	0.801	

References

1 F. Thissandier, A. Le Comte, O. Crosnier, P. Gentile, G. Bidan, E. Hadji, T. Brousse and S. Sadki, Highly doped silicon nanowires based electrodes for micro-electrochemical capacitor applications, *Electrochem. Commun.*, 2012, **25**, 109-111.

2 A. Soam, N. Arya, A. Singh and R. Dusane, Fabrication of silicon nanowires based on-chip micro-supercapacitor, *Chem. Phys. Lett.*, 2017, **678**, 46-50.

3 D. Gaboriau, D. Aradilla, M. Brachet, J. Le Bideau, T. Brousse, G. Bidan, P. Gentile and S. Sadki, Silicon nanowires and nanotrees: elaboration and optimization of new 3D architectures for high performance on-chip supercapacitors, *RSC Adv.*, 2016, **6**, 81017-81027.

4 L. Qiao, A. Shougee, T. Albrecht and K. Fobelets, Oxide-coated silicon nanowire array capacitor electrodes in room temperature ionic liquid, *Electrochim. Acta*, 2016, **210**, 32-37.

5 D. Aradilla, G. Bidan, P. Gentile, P. Weathers, F. Thissandier, V. Ruiz, P. Gómez-Romero, T. J. S. Schubert, H. Sahin and S. Sadki, Novel hybrid micro-supercapacitor based on conducting polymer coated silicon nanowires for electrochemical energy storage, *RSC Adv.*, 2014, **4**, 26462-26467.

6 X. Shen, C. Liu, X. Zhang, J. Li, J. Zhao and S. Li, High capacitive PEDOT-coated SiNWs electrode for micro-supercapacitors with facile preparation, *J. Inorg. Organomet. Polym.*, 2020, **30**, 3722-3734.

7 D. Aradilla, D. Gaboriau, G. Bidan, P. Gentile, M. Boniface, D. Dubal, P. Gómez-Romero, J. Wimberg, T. J. S. Schubert and S. Sadki, Innovative 3-D nanoforest heterostructure made of polypyrrole coated silicon nanotrees for new high performance hybrid micro-supercapacitor, *J. Mater. Chem. A*, 2015, **3**, 13978-13985.

8 W. Zheng, Q. Cheng, D. Wang and C. V. Thompson, High-performance solid-state on-chip supercapacitors based on Si nanowires coated with ruthenium oxide via atomic layer deposition, *J. Power Sources*, 2017, **341**, 1-10.

9 D. P. Dubal, D. Aradilla, G. Bidan, P. Gentile, T. J. Schubert, J. Wimberg, S. Sadki and P. Gomez-Romero, 3D hierarchical assembly of ultrathin MnO_2 nanoflakes on silicon nanowires for high performance micro-supercapacitors in Li- doped ionic liquid, *Sci. Rep.*, 2015, **5**, 9771.

10 B. Zhu, X. Wu, W. J. Liu, H. L. Lu, D. W. Zhang, Z. Fan and S. J. Ding, High-performance on-chip supercapacitors based on mesoporous silicon coated with ultrathin atomic layer-deposited In_2O_3 films, *ACS Appl. Mater. Interfaces*, 2019, **11**, 747-752.

11 R. R. Devarapalli, S. Szunerits, Y. Coffinier, M. V. Shelke and R. Boukherroub, Glucose-derived porous carbon-coated silicon nanowires as efficient electrodes for aqueous micro-supercapacitors, *ACS Appl. Mater. Interfaces*, 2016, **8**, 4298-4302.

12 D. Aradilla, F. Gao, G. Lewes-Malandrakis, W. Müller-Sebert, D. Gaboriau, P. Gentile, B. Iliev, T. Schubert, S. Sadki, G. Bidan and C. E. Nebel, A step forward into hierarchically nanostructured materials for high performance micro-supercapacitors: Diamond-coated SiNW electrodes in protic ionic liquid electrolyte, *Electrochem. Commun.*, 2016, **63**, 34-38.

13 A. Soam, P. Kavle, A. Kumbhar and R. O. Dusane, Performance enhancement of micro-supercapacitor by coating of graphene on silicon nanowires at room temperature, *Current Applied Physics*, 2017, **17**, 314-320.

14 J. P. Alper, S. Wang, F. Rossi, G. Salviati, N. Yiu, C. Carraro and R. Maboudian, Selective ultrathin carbon sheath on porous silicon nanowires: materials for extremely high energy density planar micro-supercapacitors, *Nano Lett.*, 2014, **14**, 1843-1847.

15 B. Wei, H. Liang, Z. Qi, D. Zhang, H. Shen, W. Hu and Z. Wang, Construction of 3D Si@Ti@TiN thin film arrays for aqueous symmetric supercapacitors, *Chem. Commun.*, 2019, **55**, 1402-1405.

16 D. Aradilla, F. Gao, G. Lewes-Malandrakis, W. Muller-Sebert, P. Gentile, M. Boniface, D. Aldakov, B. Iliev, T. J. Schubert, C. E. Nebel and G. Bidan, Designing 3D multihierarchical heteronanostructures for high-performance on-chip hybrid supercapacitors: poly(3,4-(ethylenedioxy)thiophene)-coated

Diamond/silicon nanowire electrodes in an aprotic ionic liquid, *ACS Appl. Mater. Interfaces*, 2016, **8**, 18069-18077.

17 Q. Zhou, Y. Zhou, M. Bao and X. Ni, Modified silicon nanowires@polypyrrole core-shell nanostructures by poly(3,4-ethylenedioxythiophene) for high performance on-chip micro-supercapacitors, *Appl. Surf. Sci.*, 2019, **487**, 236-243.

18 A. Valero, A. Mery, D. Gaboriau, P. Gentile and S. Sadki, One step deposition of PEDOT–PSS on ALD protected silicon nanowires: Toward ultrarobust aqueous microsupercapacitors, *ACS Appl. Energy Mater.*, 2018, **2**, 436-447.

19 S. Ortaboy, J. P. Alper, F. Rossi, G. Bertoni, G. Salviati, C. Carraro and R. Maboudian, MnOx-decorated carbonized porous silicon nanowire electrodes for high performance supercapacitors, *Energ. Environ. Sci.*, 2017, **10**, 1505-1516.

20 Q. Zhou, M. Bao and X. Ni, A novel surface modification of silicon nanowires by polydopamine to prepare SiNWs/NC@NiO electrode for high-performance supercapacitor, *Surf. Coat. Technol.*, 2020, DOI: 10.1016/j.surfcoat.2020.126660.

21 P. Lu, E. Halvorsen, P. Ohlckers, L. Müller, S. Leopold, M. Hoffmann, K. Grigoras, J. Ahopelto, M. Prunnila and X. Chen, Ternary composite Si/TiN/MnO_2 taper nanorod array for on-chip supercapacitor, *Electrochim. Acta*, 2017, **248**, 397-408.

22 N. R. Chodankar, I. V. Bagal, S.-W. Ryu and D.-H. Kim, Hybrid material passivation approach to stabilize the silicon nanowires in aqueous electrolyte for high-energy efficient supercapacitor, *Chem. Eng. J.*, 2019, **362**, 609-618.

23 J. Li, N. Van Toan, Z. Wang and T. Ono, Metal-assisted-chemical-etching of silicon nanowires for templating 3D graphene growth towards energy storage in microsystems, *J. Micromech. Microeng.*, 2019, **29**.

24 D. Aradilla, M. Delaunay, S. Sadki, J.-M. Gérard and G. Bidan, Vertically aligned graphene nanosheets on silicon using an ionic liquid electrolyte: towards high performance on-chip micro-supercapacitors, *J. Mater. Chem. A*, 2015, **3**, 19254-19262.

25 G. S. Gund, D. P. Dubal, D. Aradilla, D. Gaboriau, P. Gentile, T. J. S. Schubert, W. Mueller-Sebert, G. Bidan, J. Wimberg, S. Sadki and P. G. Romeroa, Diamond-

coated silicon nanowires for enhanced micro-supercapacitor with ionic liquids, *International Conference on Industrial Instrumentation and Control (ICIC)*, 2015, **978**, 4799-7165.

26 F. Gao, G. Lewes-Malandrakis, M. T. Wolfer, W. Müller-Sebert, P. Gentile, D. Aradilla, T. Schubert and C. E. Nebel, Diamond-coated silicon wires for supercapacitor applications in ionic liquids, *Diamond Relat. Mater.*, 2015, **51**, 1-6.

27 Y. Bencheikh, M. Harnois, R. Jijie, A. Addad, P. Roussel, S. Szunerits, T. Hadjersi, S. El Hak Abaidia and R. Boukherroub, High performance silicon nanowires/ruthenium nanoparticles micro-supercapacitors, *Electrochim. Acta*, 2019, **311**, 150-159.

28 J. Li, M. Zhu, Z. An, Z. Wang, M. Toda and T. Ono, Constructing in-chip micro-supercapacitors of 3D graphene nanowall/ruthenium oxides electrode through silicon-based microfabrication technique, *J. Power Sources*, 2018, **401**, 204-212.

29 N. Van Toan, T. T. Kim Tuoi, J. Li, N. Inomata and T. Ono, Liquid and solid states on-chip micro-supercapacitors using silicon nanowire-graphene nanowall-pani electrode based on microfabrication technology, *Mater. Res. Bull.*, 2020, **131**.