SUPPLEMENTARY MATERIALS FOR

Benzohexacene guide in accurate determination of field effect carrier mobilities in long acenes.

E. Bedel Pereira^a, J. Bassaler^a, H. Laval^a, J. Holec^b, R. Monflier^a, F. Mesnilgrente^a, L. Salvagnac^a, E. Daran^a, B. Duployer^d, C. Tenailleau^d, A. Gourdon^b, A. Jancarik^{b, c} and I. Séguy^{*a}

^a LAAS-CNRS, Université de Toulouse, UPS, 31031 Toulouse, France

^b CEMES-CNRS, 29 Rue J. Marvig, 31055 Toulouse (France)

^c CRPP, UMR CNRS 5031, Université de Bordeaux, 33600 Pessac, France.

^d CIRIMAT, Université de Toulouse, CNRS, Université Toulouse 3 - Paul Sabatier, 118 Route de Narbonne, 31062 Toulouse cedex 9 - France

E-mail: iseguy@laas.fr



0 nm

Figure S1. AFM tapping mode $5x5 \ \mu m^2$ images of 50 nm tetracene film grown on SiO₂/OTS substrates at a deposition flux of ca. 0.4 Å.s⁻¹.



Figure S2. X-ray diffraction patterns of 20 nm (red), 50 nm (blue) and 90 nm (black) thick benzohexacene films deposited on SiO₂/OTS at nominal deposition flux of 0.4 Å.s^{-1} .



Figure S3. X-ray diffraction patterns of 50 nm thick benzohexacene films deposited on SiO₂/OTS at nominal deposition flux of 0.2 Å.s⁻¹ (red), 0.4 Å.s⁻¹ (blue), 2 Å.s⁻¹ (black).

The room-temperature output characteristics of transistors prepared with 75 nm-thick tetracene film on OTS treated (called OTS) and untreated SiO₂ substrates (called no OTS) were first measured. The I_{DS} vs V_{DS} characteristics obtained on OTS-grafted devices are displayed in Figure S4. The source – drain distance, L, is 50 μ m and the channel width, W, is 1000 μ m. The OTFT operated at source-drain voltage, V_{DS}, up to - 50 V. A sharp increase of the source–drain current, IDS, at negative values of the gate voltage, V_{GS}, indicates hole accumulation (p-type) mode. A linear regime at low V_{DS} (V_{DS} < - 10 V) and a saturation regime at high V_{DS} (V_{DS} > - 10 V) are clearly observed.



Figure S4. Output characteristics of the OTS-pretreated tetracene based transistor with channel size W/L = $1000 \mu m/50 \mu m$.

Linear (μ_{lin}) and saturation (μ_{sat}) field effect mobilities are calculated based on the following equations. In linear regime ($V_{DS} < V_{GS} - V_{th}$), the drain current I_{DS} is expressed as follows:

$$\mu_{lin} = g_m \frac{L}{W} \frac{1}{C_{SiO_2} \cdot V_{DS}} \quad \text{with } g_m = \frac{\partial I_{SD}}{\partial V_{GS}} \qquad (Eq. S1)$$

where W and L are the channel width and length respectively, C_{SiO2} is the oxide capacitance per unit area, V_{th} the threshold voltage and μ_{lin} the field effect mobility extracted via a linear fitting of the transconductance g_m .

For the saturation regime ($V_{DS} > V_{GS} - V_{th}$), the field effect mobility, μ_{sat} , is then extracted by linear fitting of the square root of I_{DS} :



 $\mu_{sat} = \frac{2L}{W} \frac{1}{C_{SiO_2}} \left(\frac{\partial \sqrt{|I_{SD}|}}{\partial V_{GS}} \right)^2 \tag{Eq. S2}$

Figure S5. Semilogarithmic transfer curves (left y-axis) and plot of square root (right y-axis) versus gate voltage for $V_{DS} = -10$ V (a) and $V_{DS} = -50$ V (b) of OTS-grafted tetracene based OTFT with channel size W/L = 1000 μ m/50 μ m.

Figures S5(a) and (b) show transfer characteristics, for $V_{DS} = -10$ V (linear regime) and $V_{DS} = -50$ V (saturation regime) of OTS-grafted tetracene transistor. The measured devices presenting a very slight hysteresis, we consider the forward curve to extract the parameters of interest. The threshold voltage, V_{th} , is obtained using the extrapolation in the linear region method at $V_{DS} = -10$ V (Fig. 7(a)). From these measurements, we found a V_{th} of -16 V, an I_{On}/I_{Off} ratio of 2.5.10⁶.

The field effect mobility, calculated at linear and saturation regimes, are 0.12 cm².V⁻¹.s⁻ ¹ and 0.16 cm².V⁻¹.s⁻¹ respectively, comparable to those published for similar bottom contact tetracene OTFT. For transistors with untreated dielectric surface, we only achieved the characterization of the 30 µm channel length device (not shown here). We observe a drastic decrease in mobility values, close to 1.5.10⁻³ cm².V⁻¹.s⁻¹, suggesting the importance of the role played by the SiO₂ surface preparation in tetracene OTFTs with very low evaporation rate in agreement with previous published results. Since in transistors, charge transport takes place in a very thin layer adjacent to the dielectricsemiconductor interface, the hole mobility is both governed by the polymorphic structure of the thin film and the SCO dielectric surface coverage. For this polycrystalline material, molecular orientation in the first monolayers (ML) could have a huge impact on electronic coupling leading to higher μ_{FE} for thin film phase than for bulk phase. In our samples, TFP seems to be the major phase in the first MLs, indicating that μ_{FE} limitation arises here from poor film connection in lateral transport pathways due to lack in OSC coverage (see AFM image). Such μ_{FE} decrease with tetracene effective conductive area has already been related in literature. In view of those obtained field effect mobilities, at the state of the art, we consider that our measurement method with tetracene benchmark devices is fully operational for the examination of the new n-acene presented in the paper.



Figure S6. Transfer characteristics for V_{DS} = -10 V of the no OTS benzohexacene based transistor with (black) and without channel probes (red) with channel size W/L = 300 μm / 200 μm