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## **Supporting Information**

## Suppression of Short Channel Effects in Ferroelectric Si Junctionless Transistors with Sub-10 nm Gate Length Defined by Helium Ion Beam Lithography

Teng-Jan Chang<sup>1</sup>, Ting-Yun Wang<sup>1</sup>, Chin-I Wang<sup>1</sup>, Zheng-da Huang<sup>1</sup>, Yu-Sen Jiang<sup>1</sup>, Chun-Yi Chou<sup>1</sup>,

Wei-Chung Kao<sup>1</sup>, and Miin-Jang Chen<sup>1\*</sup>

<sup>1</sup>Department of Materials Science and Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. \*E-mail: mjchen@ntu.edu.tw



**Figure S1** The time domain waveform in the PUND measurement of the MFM capacitor. The kinks in the first and third pulses of the measured voltage waveform suggests the voltage amplification induced by the FE switching in the HZO layer.



Figure S2 The GIXRD patterns of the HZO layer on  $n^+$  Si and tungsten (W).



**Figure S3** The  $I_D$ - $V_D$  curves of the (a) FE JLT and (b) PE JLT with  $L_G = 5 \mu m$ .



Figure S4 The  $I_D$ - $V_D$  curves of the (a) FE JLT and (b) PE JLT with  $L_G = -8$  nm.



**Figure S5** The dependence of the SS distribution of the FE JLTs on the gate length  $(L_G)$  for the (a) forward and (b) reverse sweeps.



Figure S6 The SS versus  $I_D$  diagram of different devices of the FE JLTs with  $L_G = -8$  nm at  $V_D = 50$  mV.



Figure S7 The SS versus  $I_D$  diagram of different devices of FE JLTs with  $L_G = -5\mu m$  at  $V_D = 50$  mV.

The statistics of the SS in the forward and reverse sweeps of all the measured FE JLTs operated at  $V_D =$  50 mV are summarized in Figure S5. It can be seen that the SS of the forward and reverse sweeps increases with the shrinkage of the gate length, as expected from short channel effects. For the forward-sweep FE JLTs, the average SS values are ~175, 140 and 100 mV/dec, respectively, for  $L_G = ~8$  nm, 100 nm, and 5 µm. The average SS values drop to ~121, 78, and 52 mV/dec for  $L_G = ~8$  nm, 100 nm, and 5 µm in the reverse sweep of the FE JLTs due to the FE polarization switching in the subthreshold region. The examples of the SS versus  $I_D$  diagrams of the FE JLTs with  $L_G = ~8$  nm and 5 µm, respectively, are plotted in Figure S6 and S7. The reproducible measurement data demonstrate that the FE polarization switching during the reverse sweep is beneficial to the suppression of SS.