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Side-liquid-gated electrochemical Transistors and their Neuromorphic Applications

Supplementary Information

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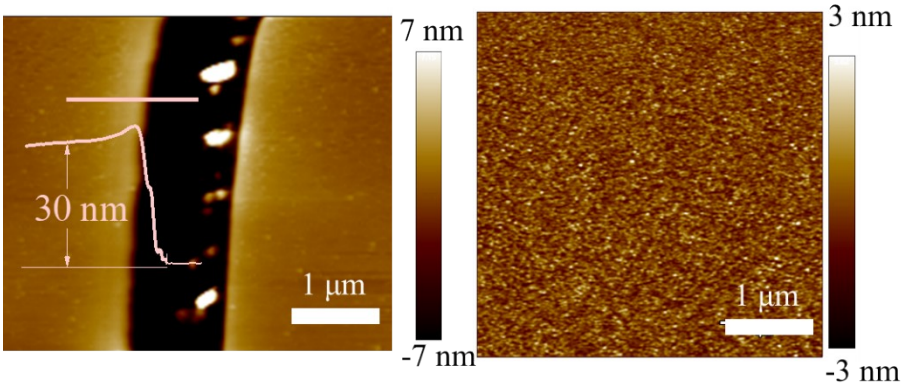

Fig. S1. AFM image of Er_2O_3 and In_2O_3 a Surface morphology and corresponding height profile of Er_2O_3. **b** Surface morphology of In_2O_3.

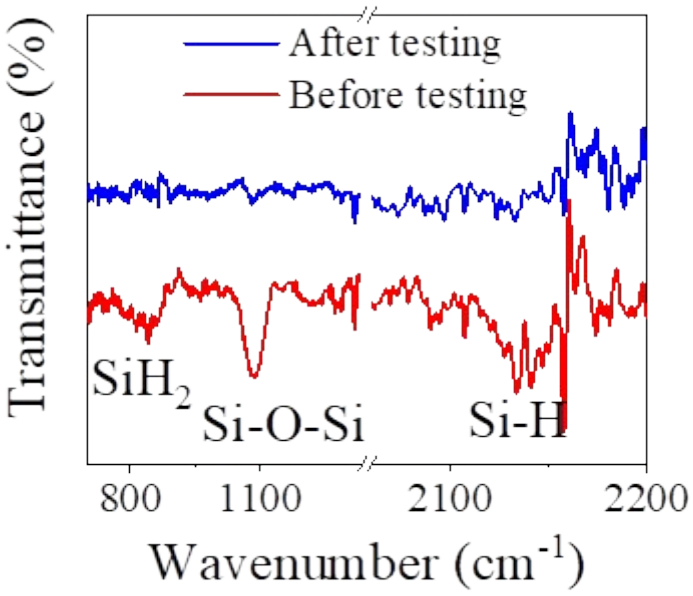

Fig. S2. IR spectra (KBr) for the SiO_2/Si substrate before and after PEO gating.

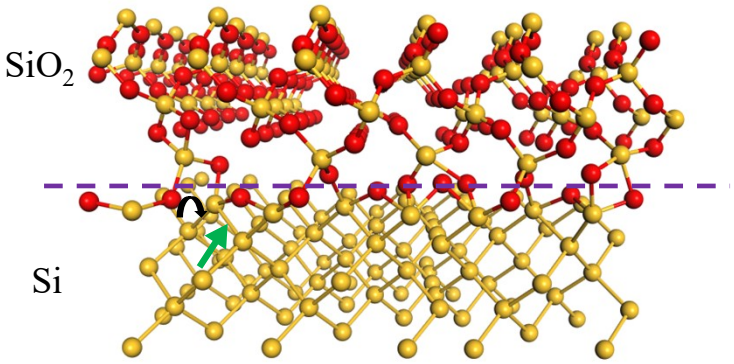

Fig. S3. The Si/SiO_2 interface Model. The position of the interface is shown by the dashed line. The black arrow shows the most probable migration path for a proton in the Si/SiO2 interface. Interface with suboxide bond (the Si–Si bond at the SiO_2 side) of the interface is indicated by the green arrow. The red and yellow spheres are O and Si atoms, respectively.

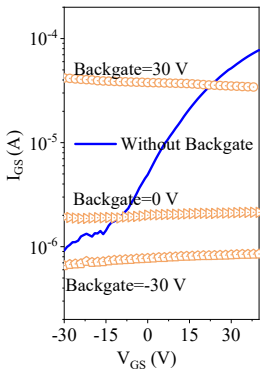

Fig. S4. The transfer characteristic curves of In_2O_3/SiO_2 TFT under different backgate voltage. The blue solid line represents the transfer characteristic curves of In_2O_3/SiO_2 TFT without backgate. The hollow pentagon, triangle, and hexagon represents the transfer curves of In_2O_3/SiO_2 TFT under fixed backgate voltage of 30 V, 0V, and -30V, respectively.

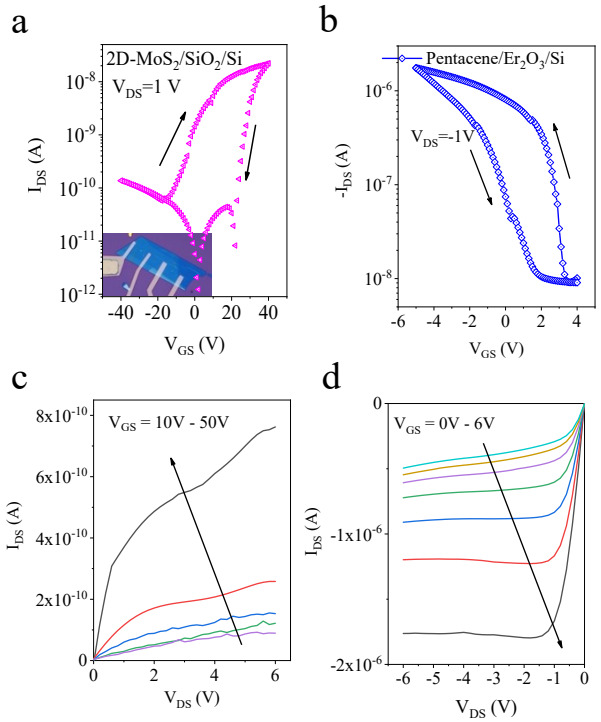

Fig. S5. Electrical characteristic of the MoS_2/SiO_2 FET and Pentacene/Er_2O_3 TFT. a, b Transfer characteristic curves of MoS_2/SiO_2 FET **(a)** and Pentacene/Er_2O_3 TFT **(b)**. **c, d** Output curves of MoS_2/SiO_2 FET **(c)** and Pentacene/Er_2O_3 TFT **(d).**

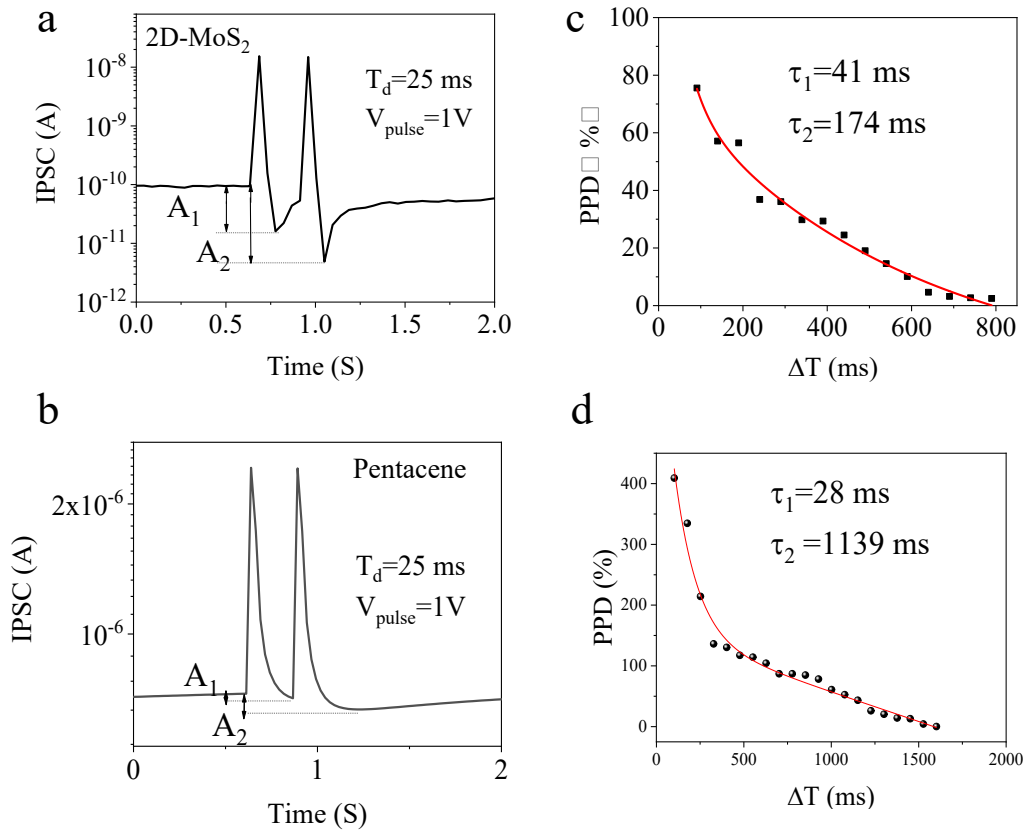

Fig. S6. The synaptic plasticity behavior of the PEO:$LiClO_4$-gate MoS_2/SiO_2 and Pentacene/Er_2O_3 synaptic transistors. a, b IPSC of the PEO:$LiClO_4$-gate MoS_2/SiO_2 (**a**) and Pentacene/Er_2O_3 (**b**) synaptic transistor triggered by a pair of displacement pulses. **b, d** Corresponding PPD index over various spike time intervals.

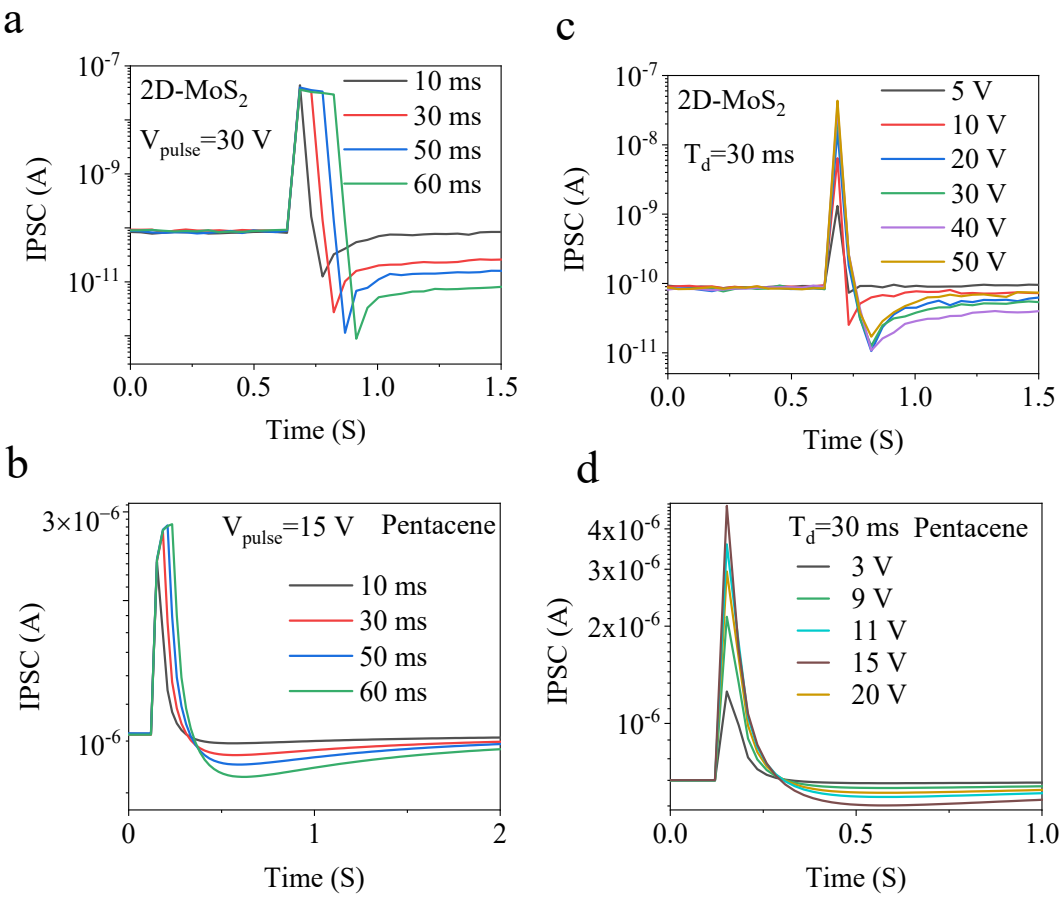

Fig. S7. The transition from STP to LTP of PEO:$LiClO_4$ gated 2D-MoS_2/SiO_2 FET and pentacene/Er_2O_3 TFT. a, b IPSCs of 2D-MoS_2/SiO_2 FET **(a)** and pentacene/Er_2O_3 TFT **(b)** triggered by side-gate pulses with different duration time. **c, d** IPSCs 2D-MoS_2/SiO_2 FET **(c)** and pentacene/Er_2O_3 TFT **(d)** triggered by side-gate pulses with different voltages.

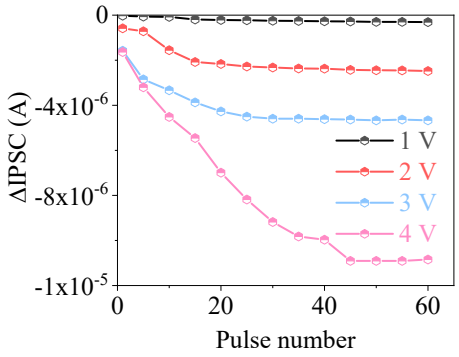

Fig. S8.The ΔIPSC of $PEO:LiClO_4$ gated In_2O_3/Er_2O_3 TFT under side-gate pulse ranging from 1 V to 4 V.