

The Supplemental Material for “One dimensional MOSFETs for sub-5 nm high performance applications: a case of Sb₂Se₃ nanowires”

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Table s1. The doping concentration and the maximum currents

Doping type	Doping concentration (/m)	Maximum currents ($\mu\text{A}/\mu\text{m}$)
	6×10^7	85.03
P-type	3×10^8	100.33
	6×10^8	111.59
N-type	1×10^7	148.86

Table s2. Criteria of the sub-5 nm Lg GAA Sb₂Se₃ FETs' ballistic efficeicny versus the 2028 needs of the ITRS 2013 for the HP and LP applications. The doping concentration is $N_n=3\times 10^7 \text{ m}^{-1}$.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{off} ($\mu\text{A}/\mu\text{m}$)	I_{on} ($\mu\text{A}/\mu\text{m}$)	I_{on}/I_{off}	C_t (fF/ μm)	τ (ps)	PDP (fJ/ μm)
HP	5	0	197.7	0.1	2.627	2.63×10^1	-	-	-
		1	150.2	0.1	734.25	7.34×10^3	-	-	-
		2	122.4	0.1	3599.588	3.60×10^4	0.25	0.13	0.31
		3	103.4	0.1	3123.159	3.12×10^4	0.20	0.12	0.25
	3	0	389.2	0.1	-	-	-	-	-
		1	257.4	0.1	-	-	-	-	-
		2	186.1	0.1	83.05	8.30×10^2	-	-	-
		3	150.1	0.1	1002.096	1.00×10^4	0.15	0.28	0.18
	1	1	845.2	0.1	-	-	-	-	-
		2	423.5	0.1	-	-	-	-	-
		3	255.0	0.1	-	-	-	-	-
	LP	5	0	197.7	5×10^{-5}	-	-	-	-
1			150.2	5×10^{-5}	-	-	-	-	-
2			122.4	5×10^{-5}	-	-	-	-	-
3			103.4	5×10^{-5}	8.359	1.67×10^5	-	-	-
3		0	389.2	5×10^{-5}	-	-	-	-	-
		1	257.4	5×10^{-5}	-	-	-	-	-
		2	186.1	5×10^{-5}	-	-	-	-	-
		3	150.1	5×10^{-5}	-	-	-	-	-
1		1	845.2	5×10^{-5}	-	-	-	-	-
		2	423.5	5×10^{-5}	-	-	-	-	-
		3	255.0	5×10^{-5}	-	-	-	-	-
ITRS									
HP	5.1	-	-	0.1	900	9.00×10^3	0.6	0.423	0.24
ITRS									
LP 2028	5.9	-	-	5×10^{-5}	295	5.90×10^6	0.69	1.493	0.28

L_g : the gate length. L_{UL} : the underlap length. SS : the subthreshold swing. I_{off} : the off-state current. I_{on} : the on-state current. C_g : the gate capacitance. τ : the delay time. PDP: the power dissipation.

Table s3. Criteria of the sub-5 nm Lg GAA Sb₂Se₃ FETs' ballistic efficiency versus the 2028 needs of the ITRS 2013 for the HP and LP applications. The doping concentration is $N_n=6\times 10^7 \text{ m}^{-1}$.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{off} ($\mu\text{A}/\mu\text{m}$)	I_{on} ($\mu\text{A}/\mu\text{m}$)	I_{on}/I_{off}	C_t (fF/ μm)	τ (ps)	PDP (fJ/ μm)
HP	5	0	248.9	0.1	-	-	-	-	-
		1	173.9	0.1	115.175	1.15×10^3	-	-	-
		2	124.1	0.1	2792.187	2.79×10^4	0.32	0.22	0.39
		3	94.5	0.1	2883.088	2.88×10^4	0.25	0.17	0.31
	3	0	505.3	0.1	-	-	-	-	-
		1	284.2	0.1	-	-	-	-	-
		2	176.0	0.1	3.29	3.29×10^1	-	-	-
		3	153.5	0.1	402.588	1.03×10^3	-	-	-
	1	1	704.8	0.1	-	-	-	-	-
		2	520.2	0.1	-	-	-	-	-
		3	342.0	0.1	-	-	-	-	-
	LP	5	0	248.9	5×10^{-5}	-	-	-	-
1			173.9	5×10^{-5}	-	-	-	-	-
2			124.1	5×10^{-5}	-	-	-	-	-
3			94.5	5×10^{-5}	8.103	1.62×10^5	-	-	-
3		0	505.3	5×10^{-5}	-	-	-	-	-
		1	284.2	5×10^{-5}	-	-	-	-	-
		2	176.0	5×10^{-5}	-	-	-	-	-
		3	153.5	5×10^{-5}	-	-	-	-	-
1		1	704.8	5×10^{-5}	-	-	-	-	-
		2	520.2	5×10^{-5}	-	-	-	-	-
		3	342.0	5×10^{-5}	-	-	-	-	-
ITRS									
HP	5.1	-	-	0.1	900	9.00×10^3	0.6	0.423	0.24
2028									
ITRS									
LP 2028	5.9	-	-	5×10^{-5}	295	5.90×10^6	0.69	1.493	0.28

L_g : the gate length. L_{UL} : the underlap length. SS : the subthreshold swing. I_{off} : the off-state current. I_{on} : the on-state current. C_g : the gate capacitance. τ : the delay time. PDP: the power dissipation.