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Electronic Supplementary Information

Self-array of one-dimensional GaN nanorods using the electric field on dielectrophoresis for photonic emitters of display pixel

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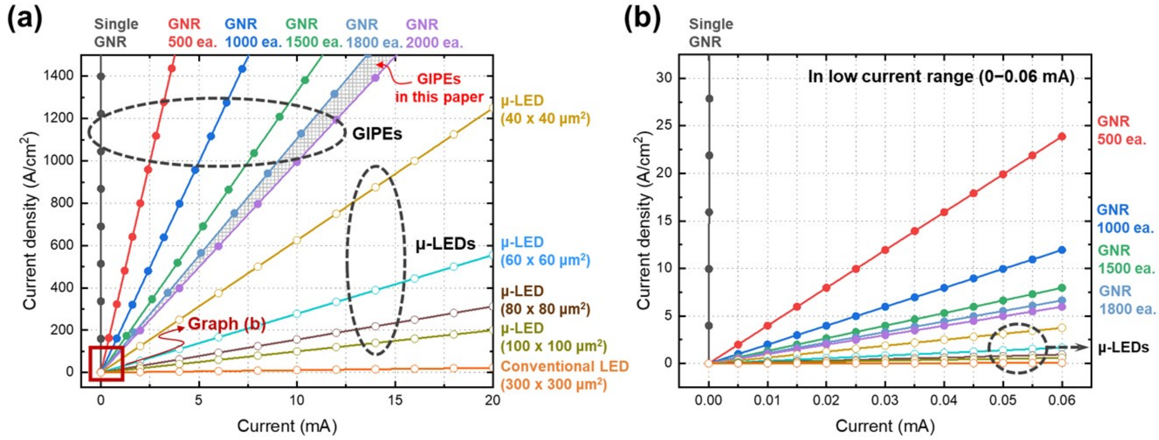

Fig. S1 (a) Current vs. current density plot of conventional LED, μ-LEDs of various sizes, single GNR PE, and the GIPEs composed of 500, 1000, 1500, and 2000 ea. of GNRs. (b) Current vs. current density plot in the range of 0−0.06 mA.

In Fig. S1a, the current densities of the GIPEs and the μ-LEDs were calculated from the current values. The GIPEs with less than 2000 ea. of GNRs have higher current densities at the same current value than those of the μ-LEDs of 40 x 40 μm^2, 60 x 60 μm^2, 80 x 80 μm^2, 100 x 100 μm^2, and conventional LED of 300 x 300 μm^2. Furthermore, the current densities of the GIPEs increase more significantly than those of the μ-LEDs as the current value increases. Therefore, the external quantum efficiency droop of GIPEs appears to be more pronounced than that of the μ-LEDs. Fig. S1b shows that single GNR and GIPEs have higher current density compared to μ-LED even in the low current range.

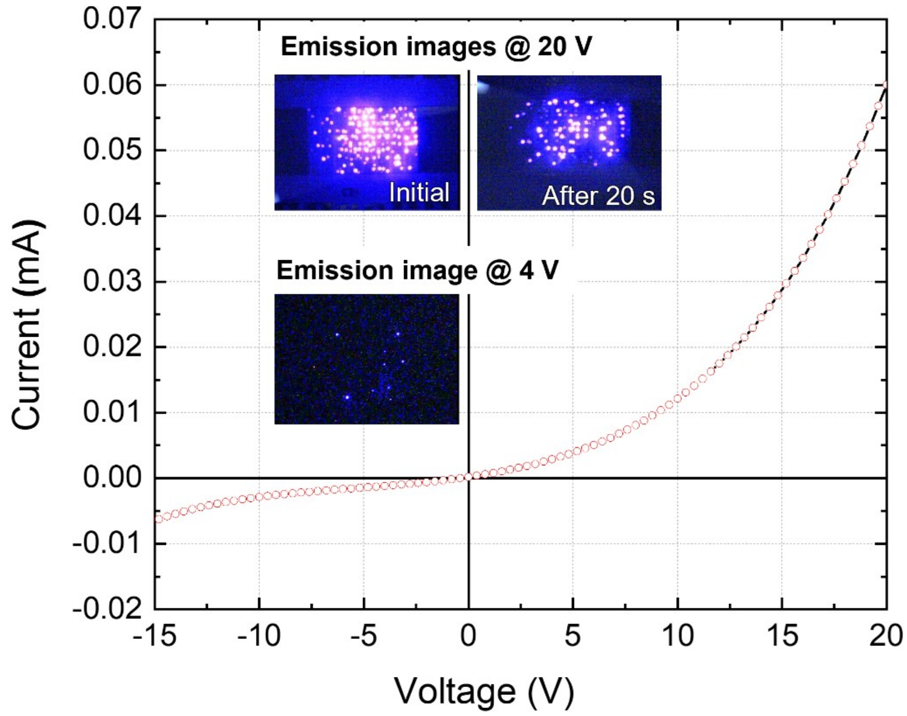

Fig. S2 Current vs. voltage curve of a GIPEs composed of horizontally self-arrayed GNRs on IDEs. (Inset) Emission images of GIPEs at 4 V and 20 V.

In Fig. S2, the GPIE had a high forward operating voltage with a maximum of 20 V at 0.06 mA because of the high current density of GNRs and the high contact resistance between the electrodes and GNRs. (Inset) The emission image of the GIPEs at a low voltage of 4 V and a high voltage of 20 V. For GIPEs operated at 20 V, the emission intensity decreased after 10–20 s compared to immediately after driving.

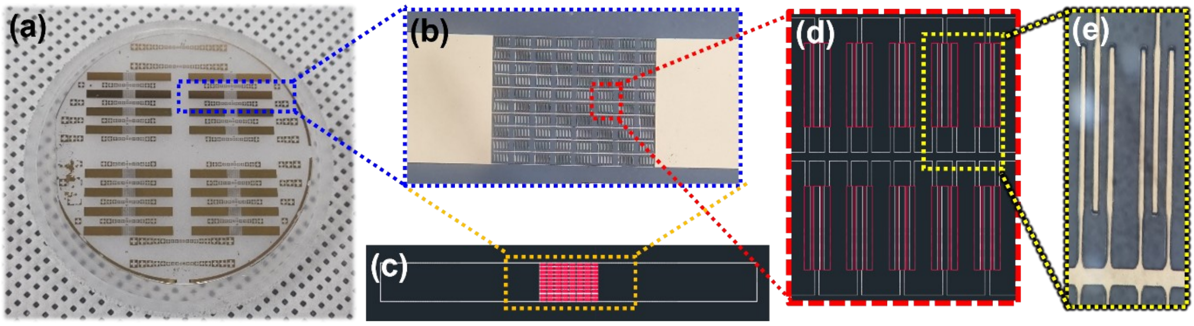

Fig. S3 (a) The image of fabricated GIPEs on the sapphire substrate. (b) The optical microscope image of a GIPE consist of IDE units of 400 ea. The CAD drawing images of (c) a single GIPE and (d) IDE units in the GIPE. (e) The OM image of IDE units of 2 ea.

Fig. S3a–e show the fabricated GIPE chips and designs. The IDE unit is composed of three finger electrodes (Fig. S3e). One GIPE has IDE units of 400 ea (Fig. S3b and c). The chip size of the GIPE is 1.7 x 16.5 mm^2, and area of the IDEs, excluding the contact pads, is 1.7 x 2.5 mm^2.

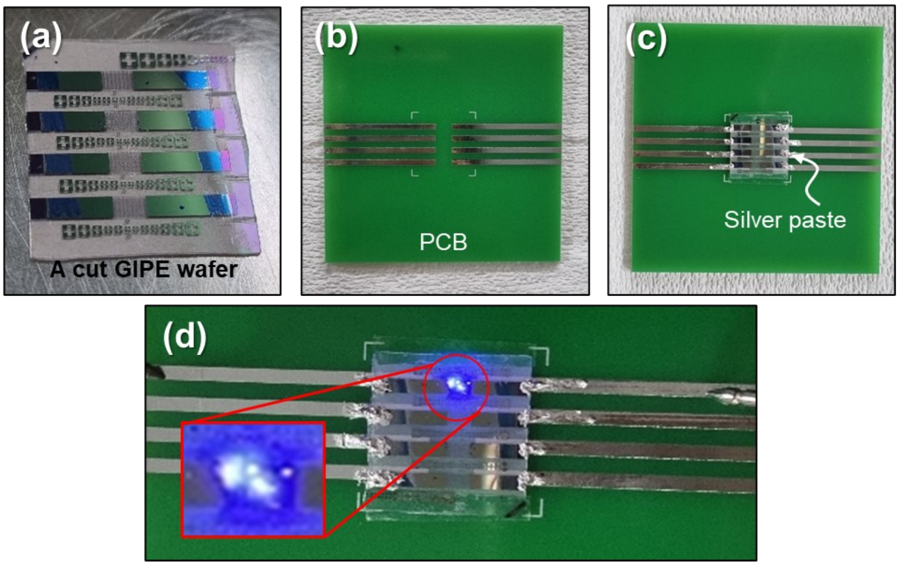

Fig. S4 The image of **(a)** a cut wafer in which GNRs are arrayed on the IDEs, **(b)** a printed circuit board (PCB) substrate, **(c)** a wafer mounted on PCB through silver paste, and **(d)** radiation of the GIPE.

Fig. S4 shows the packaged GIPE and its emission image. A cut GIPE wafer which contains horizontally arrayed GNRs on IDEs was placed on PCB. The wafer was connected to the PCB using silver pastes, as shown in Fig. S4c. Fig. S4d shows the light emission of a GIPE chip under current injection by a power supply.

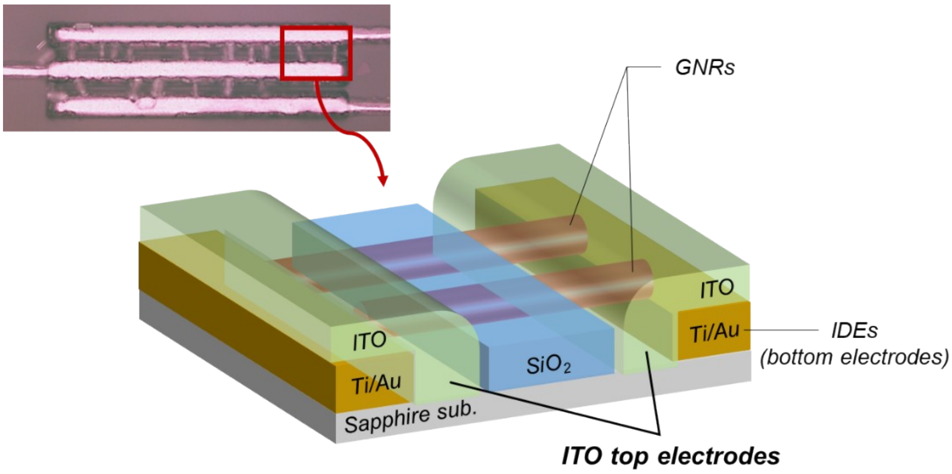

Fig. S5 The schematic image of additional top electrodes, which buried the ends of the GNRs as a sandwich structure.

The GIPEs fabricated in this paper have bottom electrodes for array GNRs and current injection to GNRs. However, for the current injection, additional electrodes are necessary due to the high contact resistance. Fig. S5 shows the schematic image of ITO top electrodes, which deposit on the ends of the GNRs and bottom electrodes after GNRs self-array process. The top electrodes are fabricated to cover both ends of the GNRs, which do not have *n*-electrodes, so that the current injection efficiency can be improved.

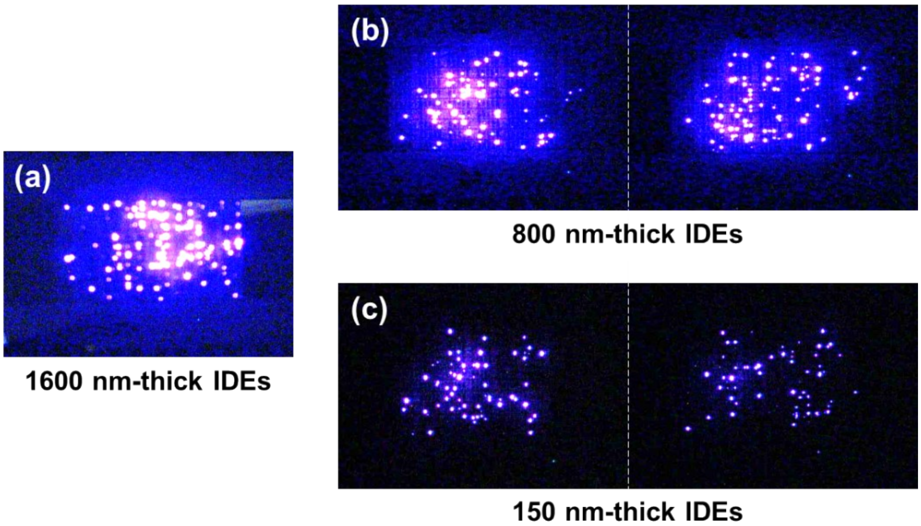

Fig. S6 The EL emission images at 15 V of (a) a GIPE chip with 1600 nm-thick IDEs, (b) GIPE chips with 800 nm-thick IDEs, and (c) GIPE chips with 150 nm-thick IDEs.

Fig. S6 shows the EL emissions depending on the electrode thickness. The GIPE chip with 1600 nm-thick IDEs is dominated by well-arrayed GNRs, and the GIPE chip with 800 nm-thick IDEs is dominated by semi-arrayed GNRs. The GIPE chip with 150 nm-thick IDEs has the lowest GNR density and many non-arrayed GNRs. It was confirmed that the EL intensity also increased with the increasing GNRs array density as the electrode thickness increased.

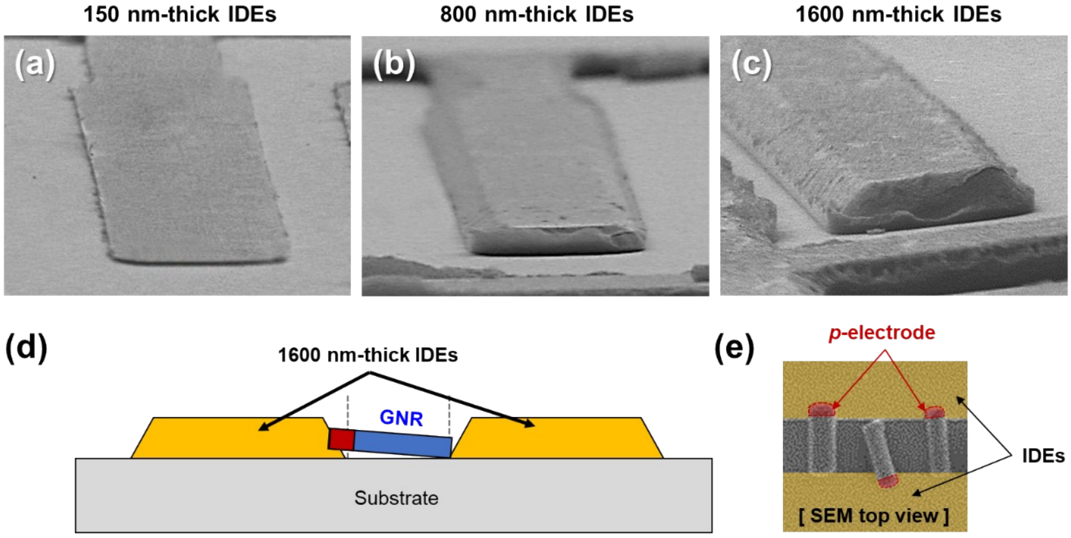

Fig. S7 The FE-SEM tilted images of (a) 150 nm-thick IDE, (b) 800 nm-thick IDE, and (c) 1600 nm-thick IDE. (d) The schematic image and (e) FE-SEM top view image of a GNR's position between 1600 nm-thick electrodes.

Fig. S7 shows the FE-SEM tilted images of different types of electrodes. In the case of 150 nm-thick IDEs, the sidewall of the electrodes was at right angles. However, in the cases of 800 and 1600 nm-thick IDEs, the sidewall of the electrodes was upward-tapered shapes. In the FE-SEM top-view images in Fig. 5a''−c'', especially 1600 nm-thick IDEs in Fig. 5c'', GNRs appear to be placed onto the electrodes because of the tapered shape of the electrodes. As shown in Fig. S7d, the GNRs placed between the electrodes were dominant. Fig. S7e shows the FE-SEM top view image of self-arrayed GNRs on the 1600 nm-thick IDEs. The *p*-electrodes of GNRs are placed on the sidewall of the IDE.

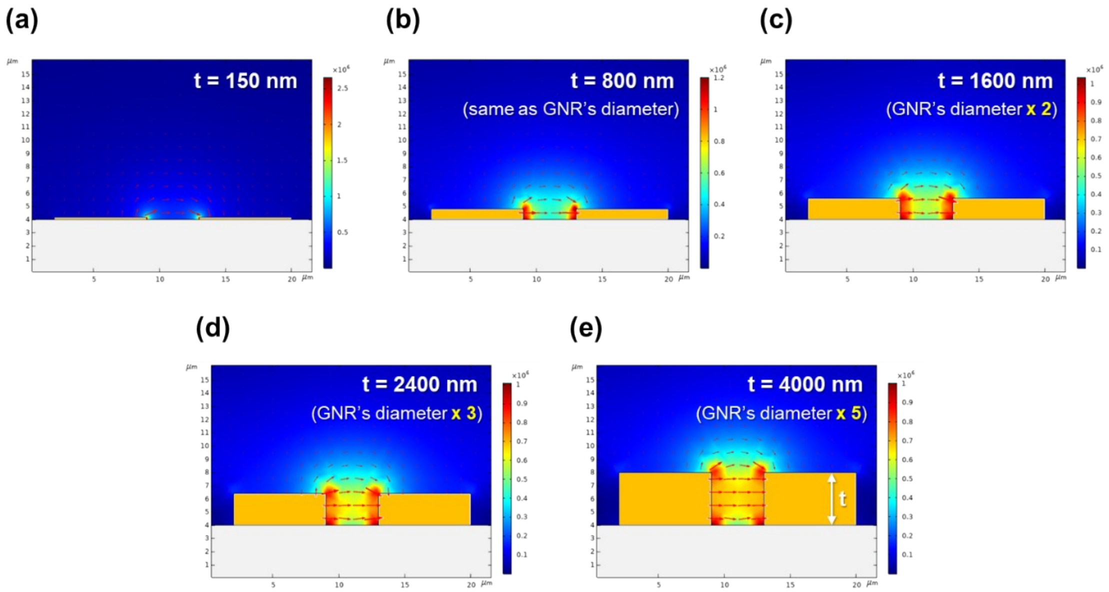

Fig. S8 The E-field simulation result of (a) 150 nm-thick electrodes, (b) 800 nm-thick electrodes, (c) 1600 nm-thick electrodes, (d) 2400 nm-thick electrodes, and (e) 4000 nm-thick electrodes using COMSOL Multiphysics software.

The E-field simulation depending on the electrode thickness was conducted by the AC/DC module of COMSOL Multiphysics software. The width of electrodes and the gap between electrodes were set as 7 μm and 4 μm, respectively. As the electrode thickness increased, E-field intensity per unit area decreased slightly but the effective E-field area became wider. However, it was confirmed that the E-field intensity between the electrodes decreased significantly at 4000 nm-thick electrodes, where the electrode thickness was five times the GNR diameter. Therefore, there is a possibility of a limit to the GNRs self-array, because the DEP force per unit area decreases when the thickness of the electrode is greatly increased.

Table S1 The comparison table of the studies on the photonic emitters using horizontally arrayed GNRs.

	Diameter of GNRs (nm)	Number of arrayed GNRs (ea.)	Chip size (mm^2)	Process conditions		The peak EQE
				Top electrode	Sidewall passivation	
Ref. 1	≤ 500	Non-reported	7 x 6	O	X	**Non-reported**
Ref. 2	530	360–540	Non-reported	O	O	**20.2 %**
Ref. 3	500	Non-reported	7 x 6	X	X	**Non-reported**
This work	800	1800–2000	1.7 x 2.5	X	O	**2.6 %**

[Reference]

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3 Y. J. Eo, G. Y. Yoo, H. Kang, Y. K. Lee, C. S. Kim, J. H. Oh, K. N. Lee, W. Kim and Y. R. Do, *ACS Appl. Mater. Interfaces*, 2017, **9**, 37912.

Table S1 shows the comparison of studies related to the PEs using horizontally arrayed GNRs. The optical properties of the devices are affected by several parameters, such as the number of arrayed GNRs, chip size, electrode structure, and so on. Therefore, the EQE results of the device fabricated in this study could not be directly compared with other literature.