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Supporting Information

Enhancing the Electrical Performance of InAs Nanowire Field-Effect Transistors through Improving Surface and Interface Properties by Coating Thermal-Oxidized Y_2O_3

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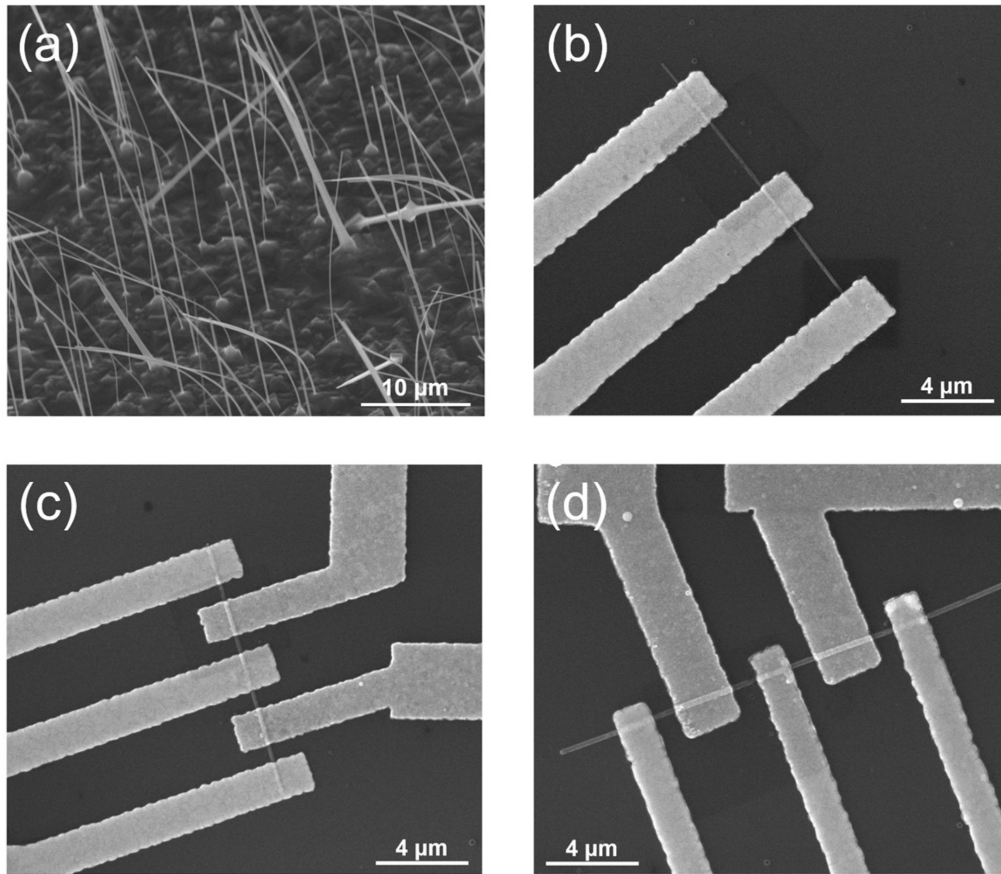

Figure S1. Scanning electron microscopy (SEM) images of InAs nanowires (NWs). (a) InAs NW array on the substrate. (b), (c), (d) Three pairs of InAs NW FETs, each based on the same individual InAs NW.

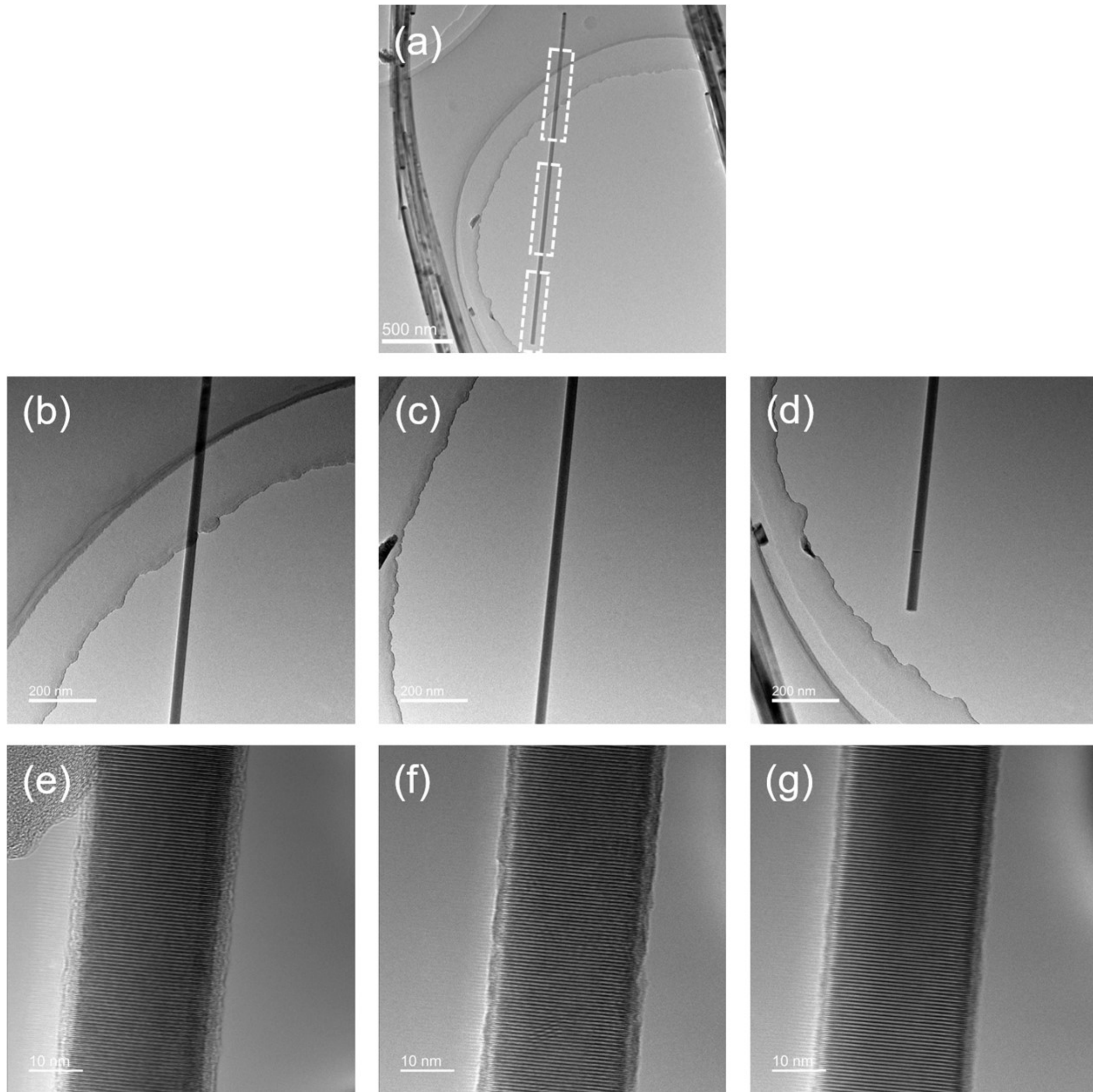

Figure S2. Transmission electron microscopy (TEM) images of a typical InAs NW. (a) Low-magnification TEM image of the InAs NW. (b)-(d) TEM images of different sections of this NW, outlined by the three dashed squares from top to bottom in (a), respectively. (e)-(g) High-resolution TEM images of the three sections in (b)-(d), respectively.

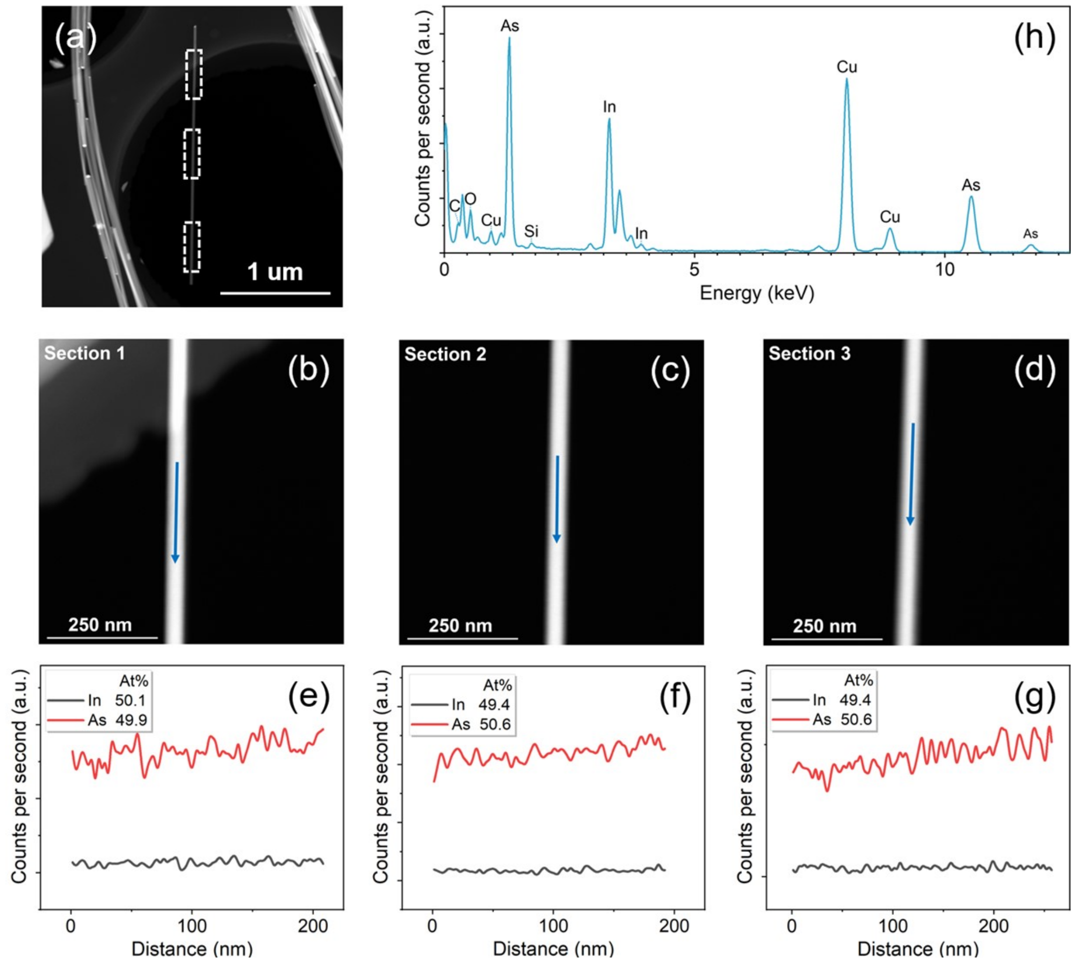

Figure S3. Scanning transmission electron microscopy (STEM) images and energy dispersive X-ray spectroscopy (EDS) analysis results of a typical InAs NW. This NW is the same one as shown in Figure S2. (a) Low-magnification STEM image of the NW. (b)-(d) STEM images of different sections of this NW, outlined by the three dashed squares in (a) from top to bottom, respectively. (e)-(g) EDS line scan results along the arrow direction in (b)-(d), respectively, showing the In/As ratio is uniform. (h) EDS spectrum of the InAs NW section in (c). The result shows that there are In and As, and O in the oxide layer besides Cu from the grid, C from the holy carbon film and small amount of Si from the detector.

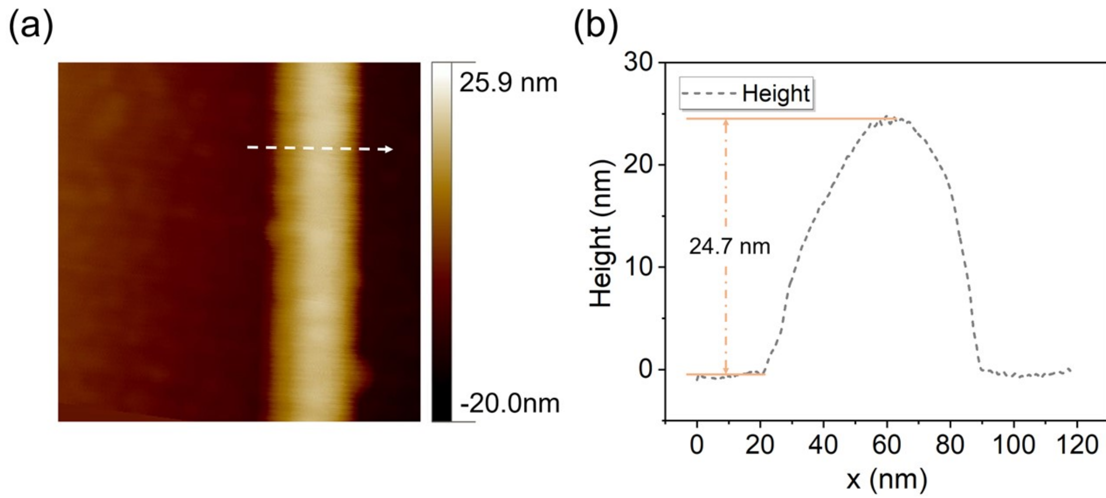

Figure S4. Atomic force microscopy (AFM) image of the NW in a baseline BGFET. The line profile in (b) is along the white dashed line in (a) showing the diameter of the NW is 24.7 nm.

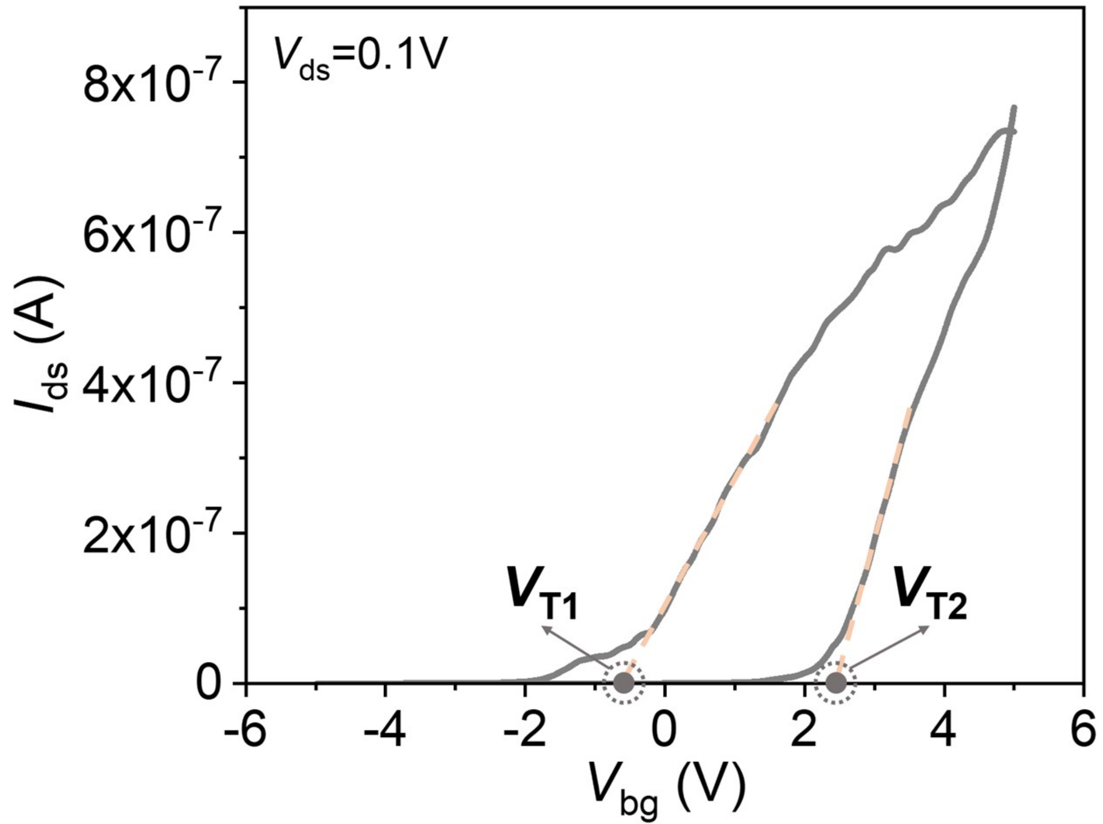

Figure S5. Method of defining the hysteresis of FET. The continuous line is the measured transfer curve in line scale. The dashed lines show the extension of the linear part of both the forward and backward transfer curves to intersect with the horizontal axis. The hysteresis of the FET can be defined by the difference of the two intersection points, V_{T1} and V_{T2}.

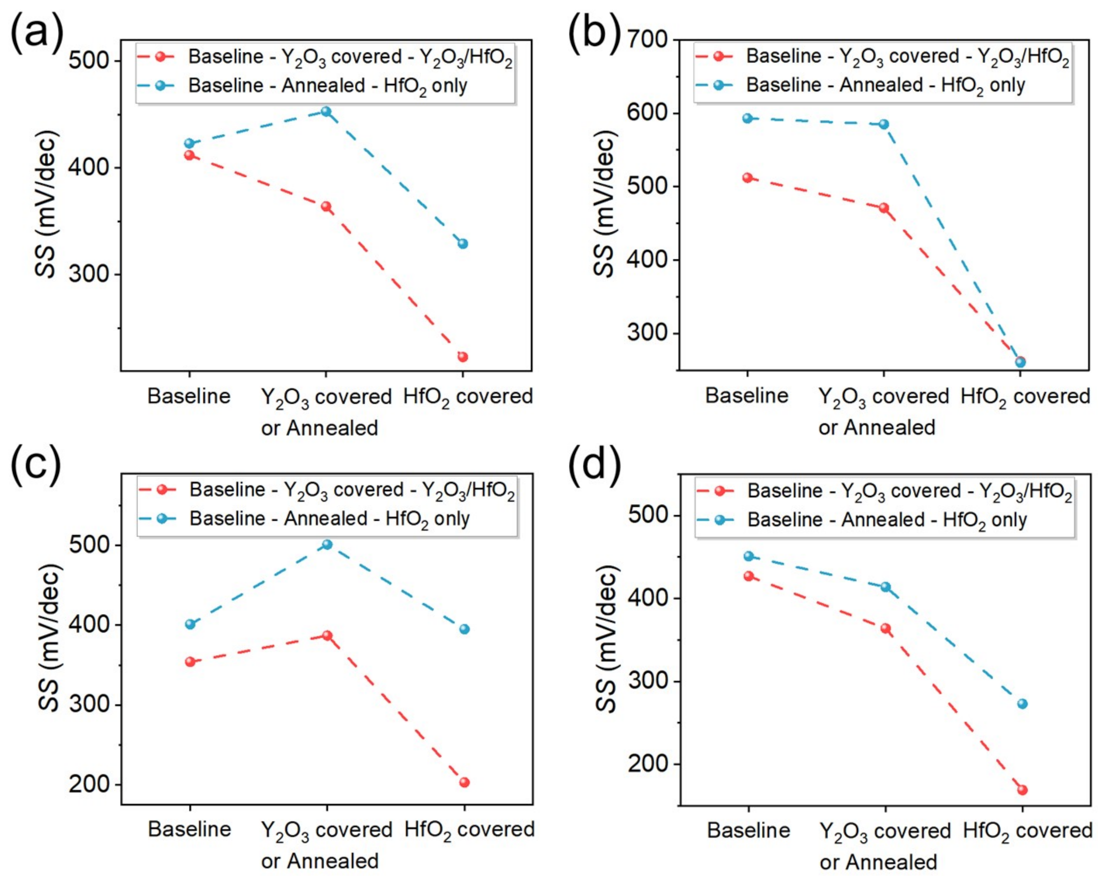

Figure S6. *SS* of other four pairs of BGFETs.

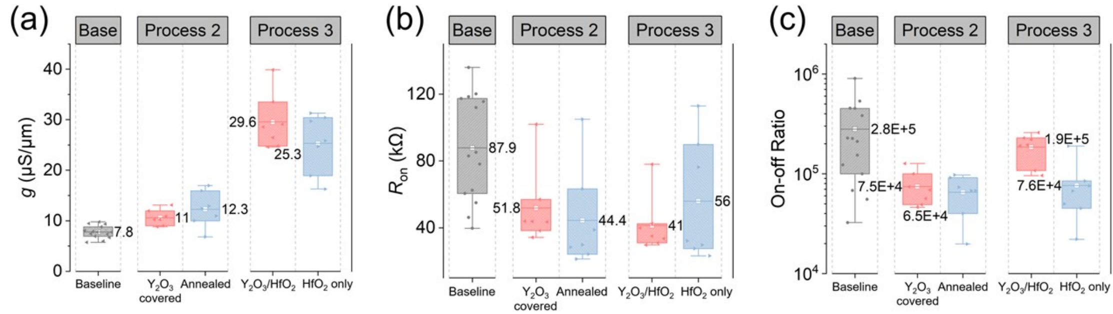

Figure S7. Statistic data of other electrical properties of paired BGFETs. (a) Transconductance, *g*. (b) On-state resistance, R_{on}. (c) On-off ratio.

As shown in Fig. S7(a), the transconductance of the device increased by the thermal annealing process is further improved after HfO_2 coating. The transconductance of the Y_2O_3/HfO_2-covered BGFETs is larger than that of the HfO_2-covered BGFETs. Fig. S7(b) shows the comparison of R_{on}. Due to different diameters of the NWs, there is a large spread in the value of R_{on} of baseline BGFETS, whereas the dispersion of R_{on} for Y_2O_3-covered BGFETs and annealed BGFETs decreases after annealing. After HfO_2 coating, R_{on} of Y_2O_3/HfO_2-covered devices decreases further, while the average value and dispersion of R_{on} of the HfO_2-covered BGFETs increase. Fig S7(c) shows the on-off ratio of the BGFETs. The diameters of the NWs used here are in the range of 18-33 nm, and the baseline BGFETs have an on-off ratio of more than five orders of magnitude, with a maximum of 9.03×10^5. The thermal annealing process reduces the dispersion of the on-off ratio, but increases I_{off} slightly, leading to a lower on-off ratio (but still greater than 10^4). After HfO_2 coverage, the electrostatic environment of the channel is improved, thus the average on-off ratio of Y_2O_3/HfO_2-covered devices is significantly increased to 1.9×10^5.

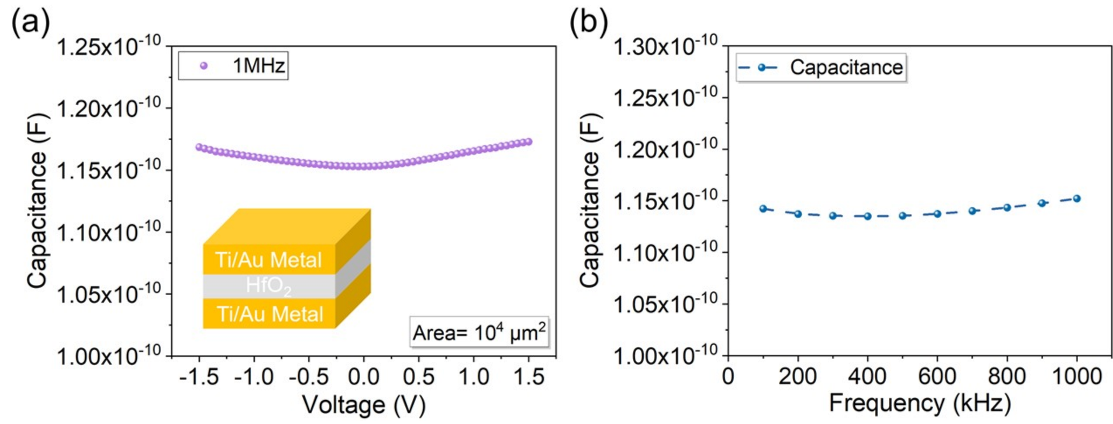

Figure S8. Capacitance test of the Ti/Au-HfO_2-Ti/Au capacitor. (a) Capacitance-voltage (*C-V*) curve. (b) Capacitance-frequency (*C-F*) curve.

$$C_{HfO_2} = A \cdot \frac{\varepsilon_0 \varepsilon_{rHfO_2}}{t_{ox_{HfO_2}}} \#(1)$$

where $\varepsilon_0 = 8.85 \times 10^{12}\ F/m$, t_{ox}=5 nm. "A" represents the capacitor area (equals to 10^4 μm^2). ε_{rHfO_2} is calculated to be 13.1 by the equation above. As shown in Fig. S8(b), the capacitance value is basically unchanged from 100 kHz to 1 MHz.

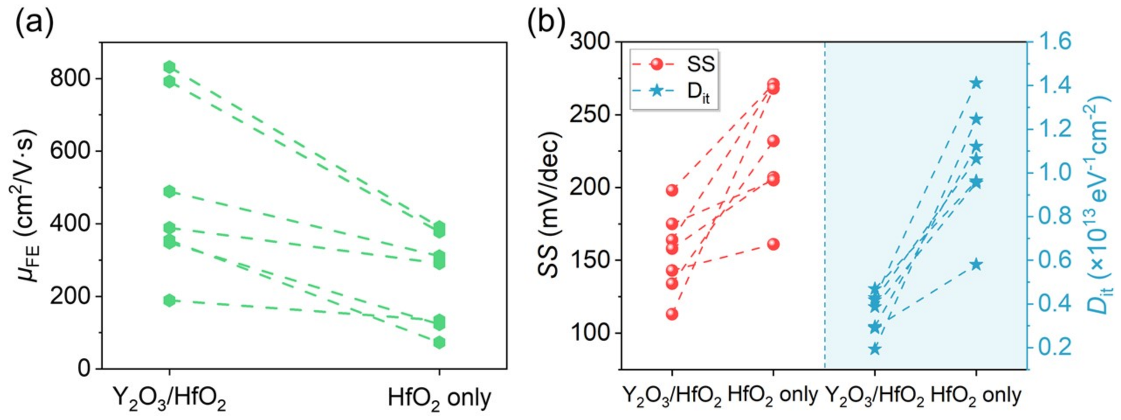

Figure S9. Comparison of (a) μ_{FE}, (b) SS and D_{it} of seven pairs of TGFETs.

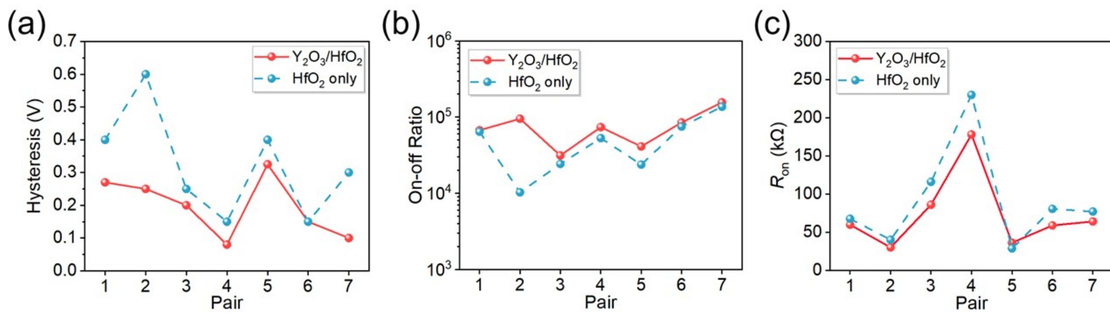

Figure S10. Comparison of electrical properties of pairs of Y_2O_3/HfO_2-covered and HfO_2-covered TGFETs. (a) Hysteresis, (b) On-off ratio, and (c) R_{on}.