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Stacked On-Chip Supercapacitors for Extreme Environments

Abhijit Baburaj[1], Hemtej Gullapalli[1,2], Anand B. Puthirath[1]*, Devashish Salpekar[1], Jarin Joyner[1], Suppanat Kosolwattana[1], Robert Vajtai, Babu Ganguli[1]*, Pulickel M. Ajayan[1]*

[1]Department of Materials Science and NanoEngineering, Rice University, 6100 Main St, Houston, TX 77005, USA
[2]Analog Garage, Analog Devices Inc. Boston, MA, USA

*E-mail: ajayan@rice.edu, babu.ganguli@rice.edu, anandputhirath@rice.edu

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S1: On-Chip Supercapacitor Cell Components and Micrograph of 3-layer structure

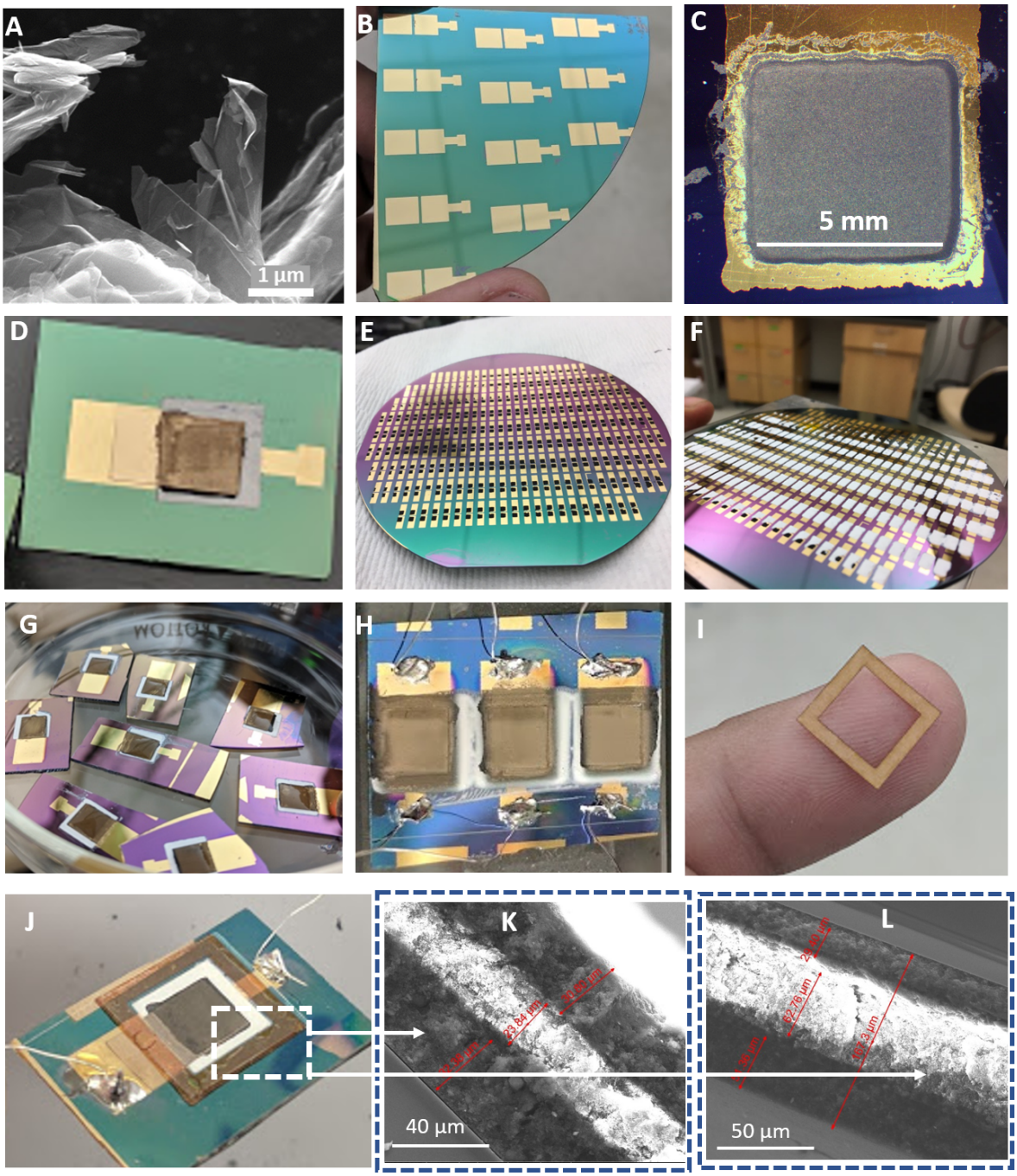


Figure S1: Different steps of fabrication process for on-chip supercapacitors (a) SEM micrograph of Nano24. The SEM image show nano graphitic flakes (b) Batch coating of Ti/Au current collector on Si/SiO2 wafer. The silicon wafer is coated with multiple current collectors and multiple devices can be coated at the same time on the Silicon wafer and cut into single devices and integrated with the micro electronic devices (c) Optical image of electrode coated on the current collector (d) Image of separator with 2nd electrode and gold coating on top (e) Batch coating of first layer of electrode. For scalability pruposes devices can be coated in a large batch using a doctor blade. The slurries for the electrodes and seperator can be spread onto the kapton template masks and homogeneously coated with the doctor blade (f) Batch coating of separator (g) Multiple devices cut after batch coating on the silicon wafer (b) Multiple stacked on-chip supercapacitors with all the layers coated and with wired connections

soldered on to the gold current collectors (i) Kapton tape cut using a laser printer. The Kapton, along with a micro-glass plate, was used to seal the device (j) Packaged on-chip supercapacitor (k) and (l) Cross-section electron micrograph of the electrodes and quasi solid-state electrolyte configurations

S2: CV data at different scan rates at -20^{0}C , RT and 60^{0}C

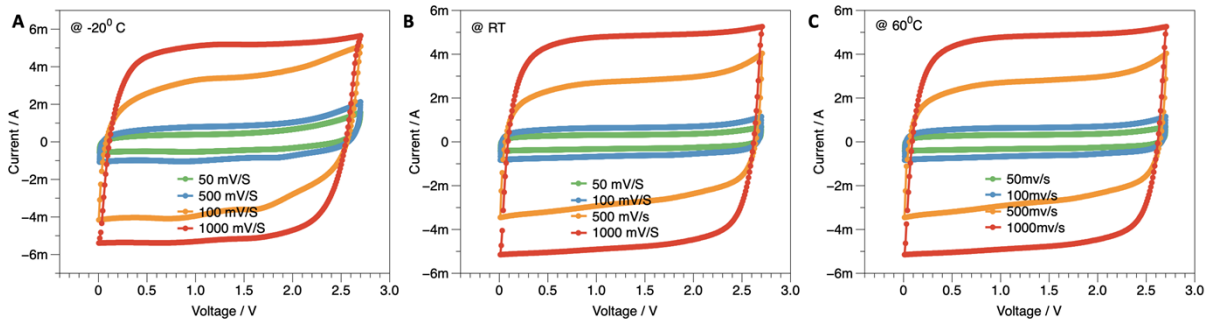


Figure S2: The cyclic voltammogram (CV) of on chip supercapacitors at different scan rates and temperatures (a) CV at -20 ^{0}C shows device capacitance of 4.8 mF, 4.6 mF, 3 mF and 2.62 mF respectiviely for 50 mV/S, 100 mV/s, 500 mV/s and 1000 mV/s (b) at room temperature, 8.85 mF, 8.3 mF, 5.75 mF and 4. 75 mF (c) at 60 ^{0}C, 10.1 mF, 9.1 mF, 8.1 mF and 5.68 mF respectively.

Table S1: The capacity variation at different voltage sweeps and various temperature ranges

Temp	Scan rate (mv/s)	Capacity (mF)
-20^{o}C	50	4.8
	100	4.6
	500	3
	1000	2.62
0^{o}C	50	8
	100	6.14
	500	4
	1000	3.02
25^{o}C (RT)	50	8.85
	100	8.3
	500	5.75
	1000	4.53
40^{0}C	50	9.6
	100	8.8
	500	8.02
	1000	5.18
60^{o}C	50	10.1
	100	9.1
	500	8.1
	1000	5.68

S3: CV data for 3 different dvices at -20^{0}C , RT and 60^{0}C

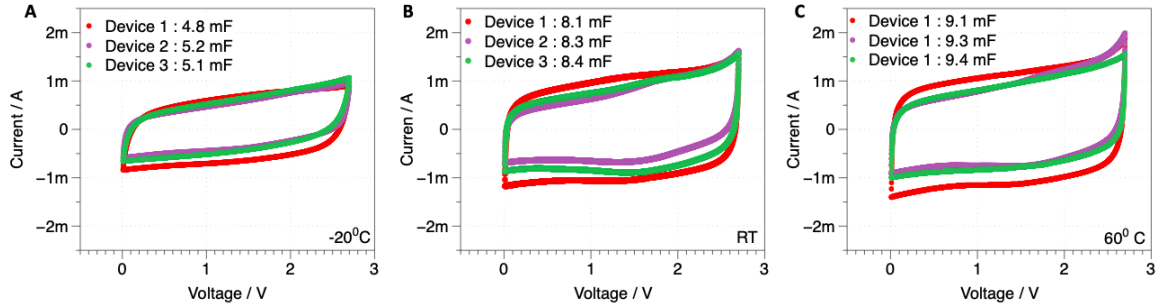


Figure S3: Comparison of electrochemical performances of three different on-chip supercapacitors at different temperature ranges (a) CV at -20 ^{0}C shows device capacitance of 4.8, 5.2 and 5.3 mF (b) The CV at room temperature with a capacitance of 8.1, 8.3 and 8.4 mF (c) CV at 60 ^{0}C with a capacitance of 9.1, 9.3 and 9.4 mF. It is worthy to note that for all three devices the capacitance values were around the same at the different temperatures.

S4: The chronoamperometric charge-discharge curves at various temperatures (-20^{0}C , RT and 60^{0}C) and for different charge-discharge currents.

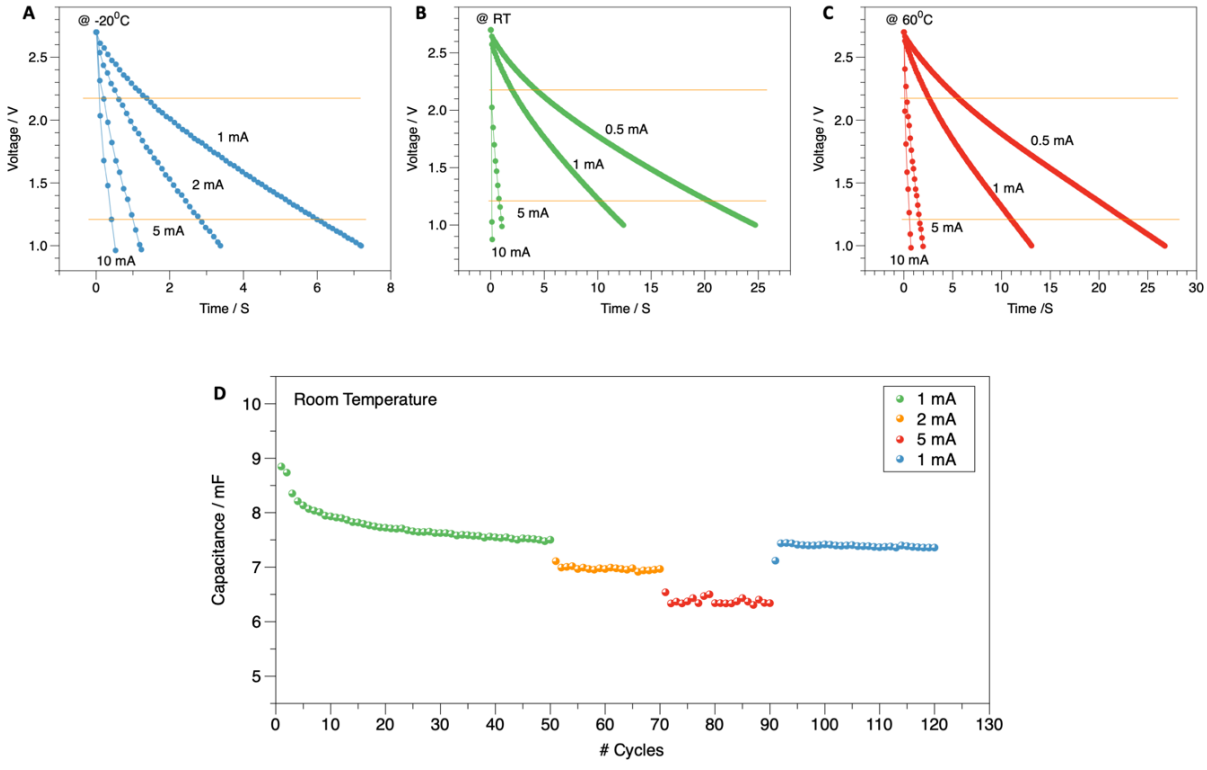


Figure S4: Comparison of the charge discharge curves of onchip super capacitor at different current rate at different tempearures (a) Dicharge curves at -20^{o}C for 1 mA, 2 mA, 5 mA and 10 mA (b) Dicharge curves at 25 ^{o}C for 1 mA, 2 mA, 5 mA and 10 mA (c) Dicharge curves at 60^{o}C for 1 mA, 2 mA, 5 mA and 10 mA and (d) the capacitance variation against the different dicharge currents over several cyles at room temperature. The voltage window that is aceessible throughout the different discharge rates are also labelled with orange lines in the dicharge curve characteristics.

S5: Galvanostatic charge-discharge measurements and charge-discharge curves of on-chip supercapacitor devices with voltage up to 2.7 V at RT.

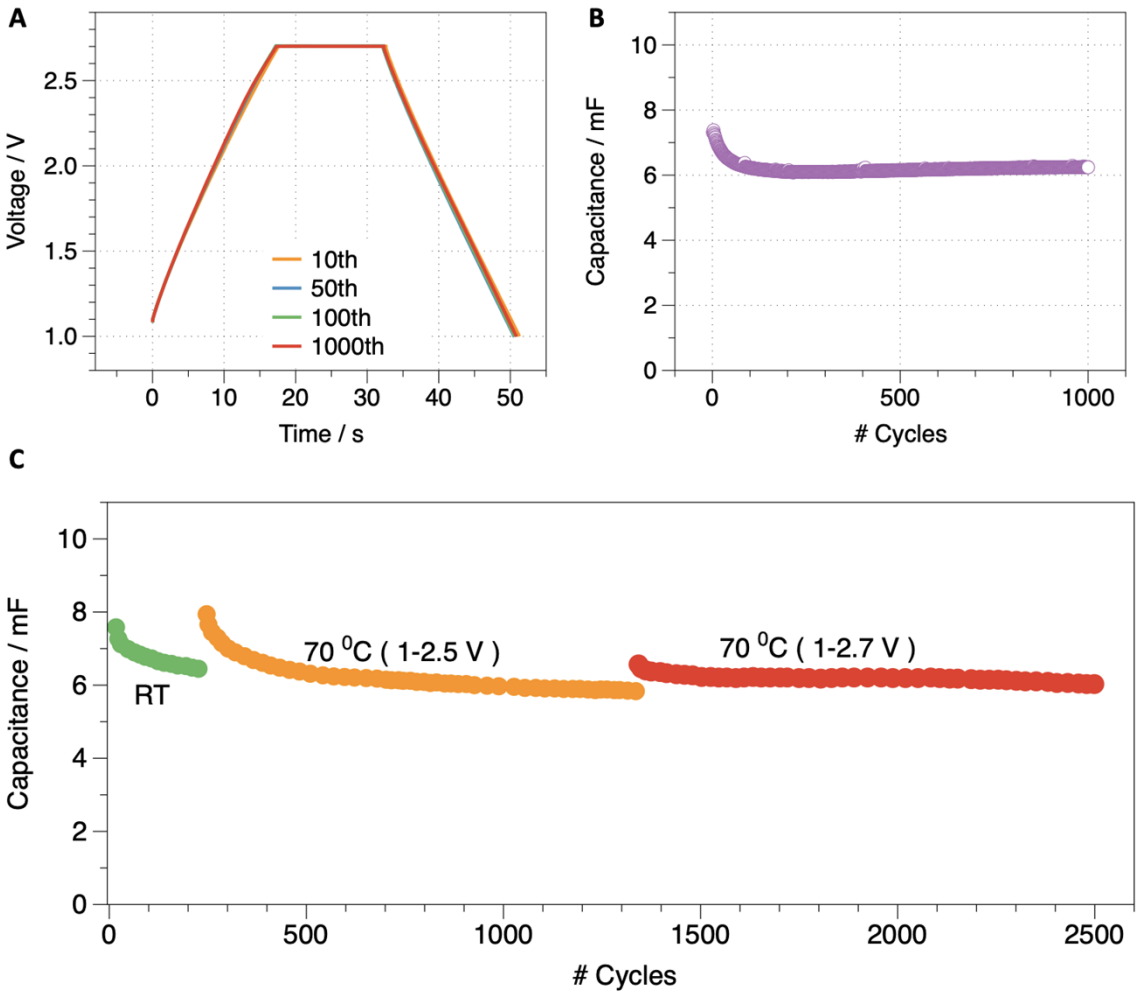
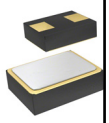


Figure S5: Charge-discharge, temperature reliability and leakage studies (a) chronoamperometric (0.5 mA, 1-2.7V) charge-discharge curves 10th, 50th, 100th and 1000th cycles (b) The cycling stability test results for 1K cycles. A drop in the capacitance observed during the initial cycles is due to the quasi-reversible chemical side reactions. (c) The charge-discharge capacity at room temperature, and 70^{0}C (1-2.5V) and 70^{0}C (1-2.7V) for over 1000 cycles. The devices showed stability even with an increase in temperature and voltage.

S6: Table (S2) of comparison of existing supercapacitor devices and their dimensions, capacitance and ESR values.

Image	Company	Size	Rated Cap	Rated ESR	Observed Capacitance @100mv/s	Observed ESR (EIS)
	CapXX GA109	20x18x1	170 mF	40 mΩ	235 mF	50 mΩ
	Maxwell BCAP0001 P270 T01	8x13.5mm (DxH)	1F	700 mΩ	2.2 F	300 mΩ
	Elna America DSK-3R3H224U-HL	6.8x 3 mm (DxH)	220 mF	200 Ω	50 mF	37.6 Ω
	Elna America DSK-3R3H703T414-HLL	4.8x1.71mm (DxH)	70 mF	100 Ω	27.05 mF	30.57 Ω
	Seiko XH311HG-IV07E	3.8x1.1mm (DxH)	20 mF	300 Ω	8.43 mF	200 Ω
	Seiko CPH3225A	3.2x2.5 x0.9mm (LxBxH)	11mF	160Ω	10.19 mF	175 Ω
	Rice On-Chip	11mm x 7.5mm x 0.1mm (+pack) Active: 7mm X 7mm			17mF and improving	6 Ω