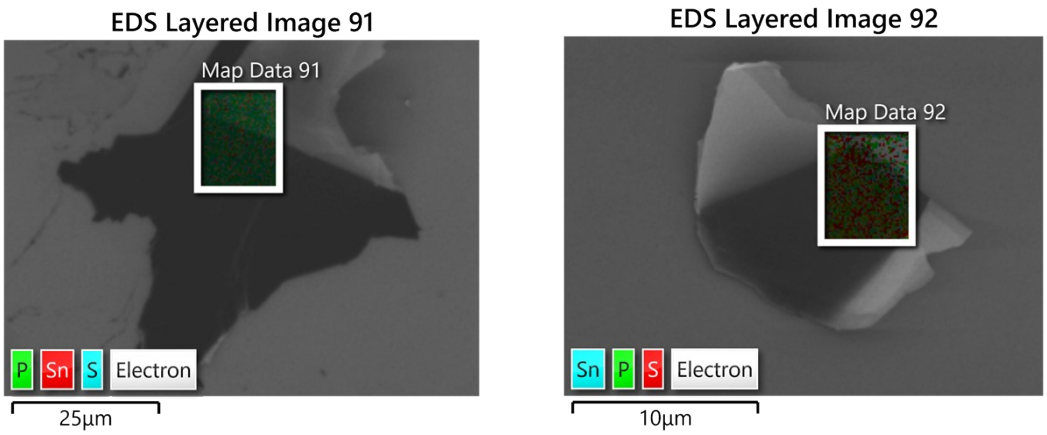
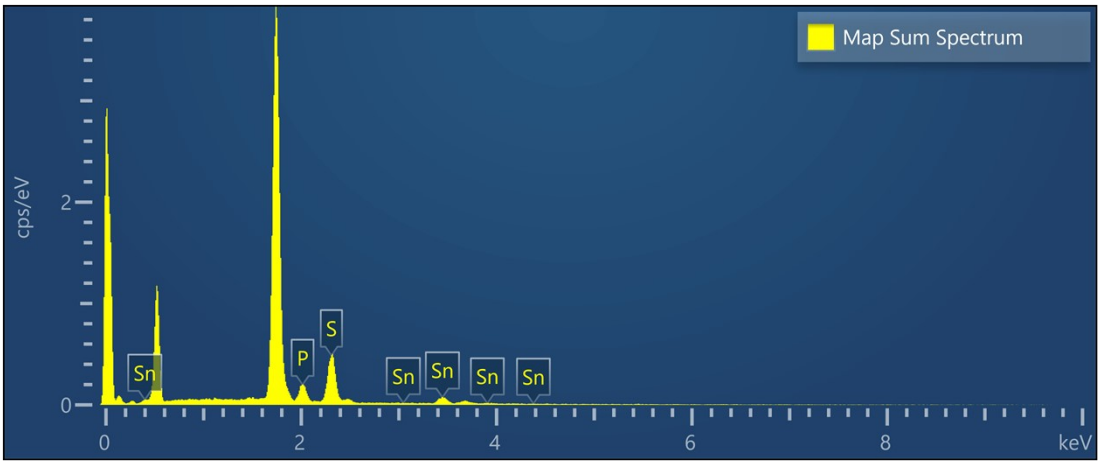
Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.





Element	Line Type	Apparent Concentration	k Ratio	Wt%	Atomic %
P	K series	10.41	0.05822	16.54	23.49
S	K series	18.36	0.15819	45.52	62.45
Sn	L series	9.93	0.09927	37.94	14.06
Total:				100.00	100.00
Element	Line Type	Apparent Concentration	k Ratio	Wt%	Atomic %
P	K series	8.64	0.04831	23.98	32.10
S	K series	9.86	0.08492	43.82	56.65
Sn	L series	4.75	0.04750	32.21	11.25
Total:				100.00	100.00

fig S1. Detailed EDS results of SnP_2S_6 samples.

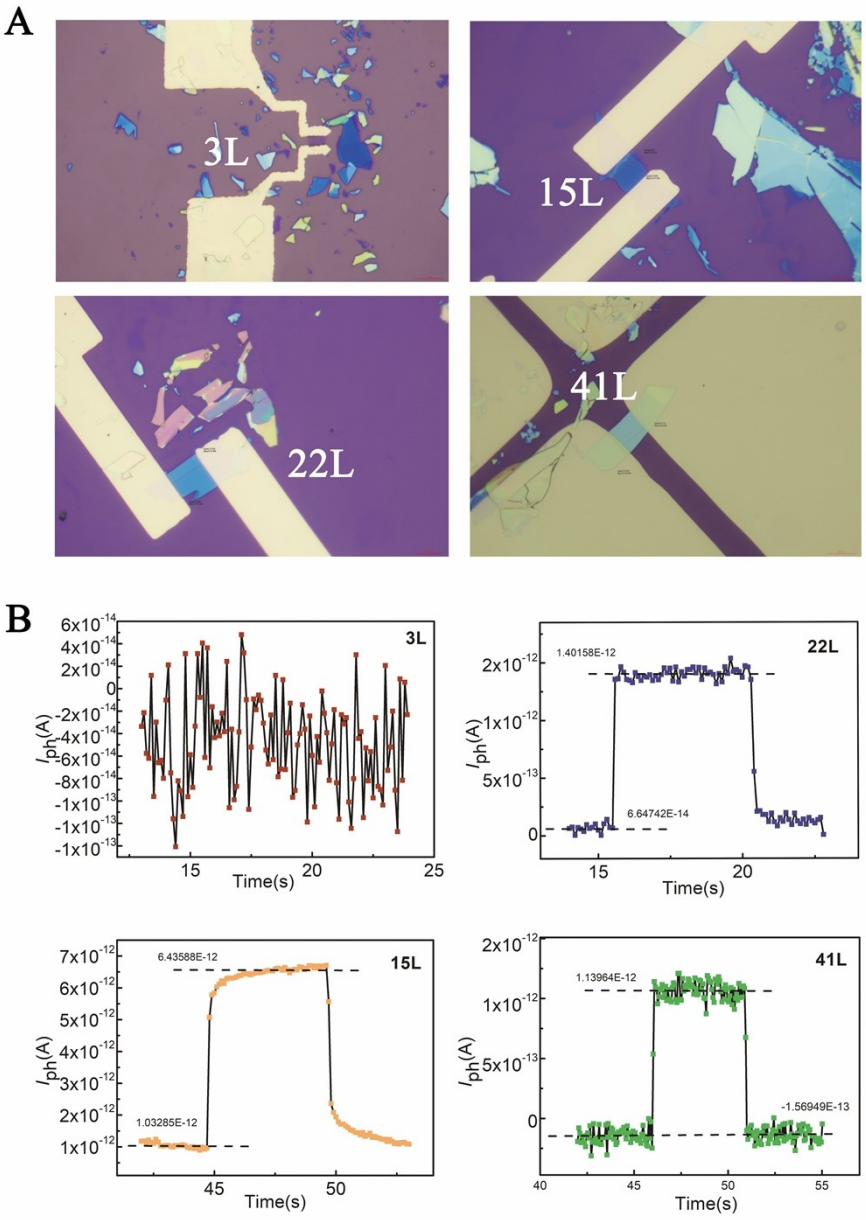


fig S2. **Photoelectric properties of SnP_2S_6 with different thickness.**

(A) Schematic of photocurrent of the different-thickness SnP_2S_6 photodetector on Si substrate. The samples with the thickness of 3 layers, 15 layers (12.7 nm), 22 layers and 41 layers were identified[3], respectively. (B) Time dependent laser ON/OFF measurement of the SnP_2S_6 devices above. As the material is very thin (same colour as the substrate in the OM image), due to the lack of carriers, the photoresponse of device is weak and the current passing through its channel is almost zero.

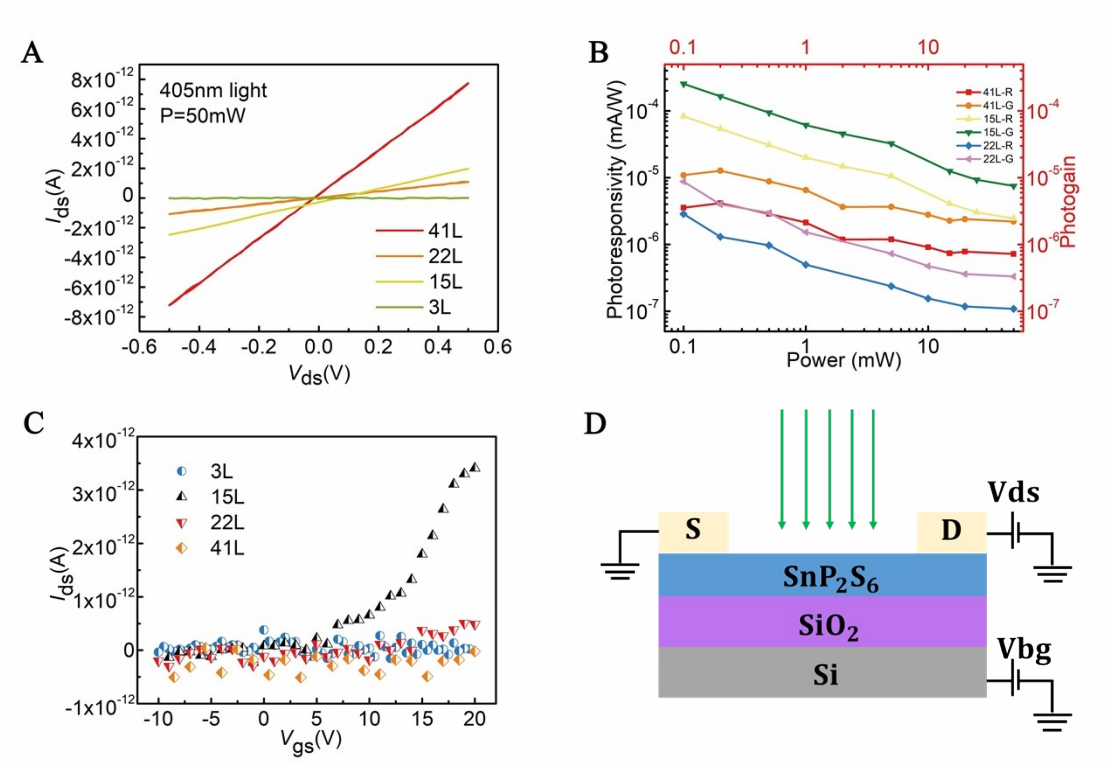


fig S3. (A) I_{ds}-V_{ds} curves of different-thickness SnP_2S_6 under 50 mW 405 nm laser. (B) Photoresponsivity (R) and photogain (G) of various SnP_2S_6 samples as a function of laser power. SnP_2S_6 with 15 layers shows best R and G of $R_{max} = 8.3 \times 10^{-5}\, mA/W$ and $G_{max} = 2.6 \times 10^{-4}$. (C) I_{ds}-V_{gs} curves of different-thickness SnP_2S_6. SnP_2S_6 of 15L has the best electric gating effect. (D) Schematic of SnP_2S_6 phototransistor on Si/SiO_2 substrate.

According to the results in fig.S2 and fig.S3, SnP_2S_6 with 15 layers has better light response, so we only list results of 15L in the main text.

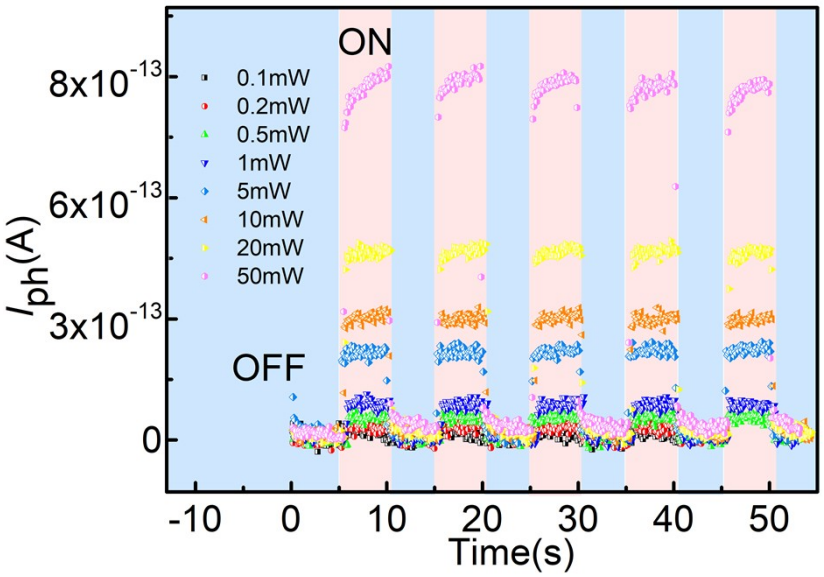


fig. S4. Time dependent ON/OFF test of 15L device under 405 nm light, whose power varies from 0.1 mW to 50 mW.

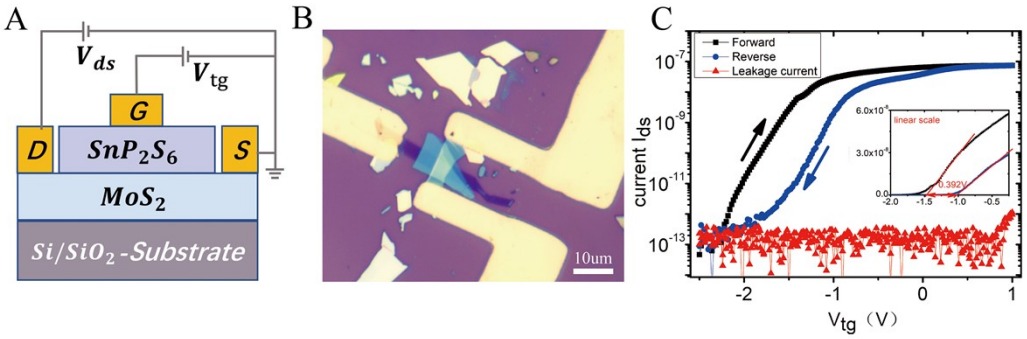


fig. S5. (A) Schematic of SnP_2S_6/MoS_2 FETs using Si/SiO_2 as substrate. (B) Optical image of a SnP_2S_6/MoS_2 FET on Si/SiO_2. (C) Double-sweep I_{ds}-V_{tg} curves show a big hysteresis of SnP_2S_6/MoS_2 FET in fig(B), and the inset is the current in linear scale (hysteresis gap $\Delta V_T \approx 0.392$ V).

We fabricate tens of top-gate FETs on Si/SiO_2, but only to find that the hysteresis is too big. The worse device performance results from the coupling, scattering from charged surface states, impurities, defects as well as the surface roughness and optical phonons. Compared with traditional substrates Si/SiO_2, 2D h-BN is considered promising together with 2D materials, because of the minimal lattice mismatch (～1.7%) involved and almost atomically flat surface that can be free of dangling bonds or surface charge traps. According to the clarification in our paper, we insert a layer of h-BN as our substrate to improve the hysteresis instability.

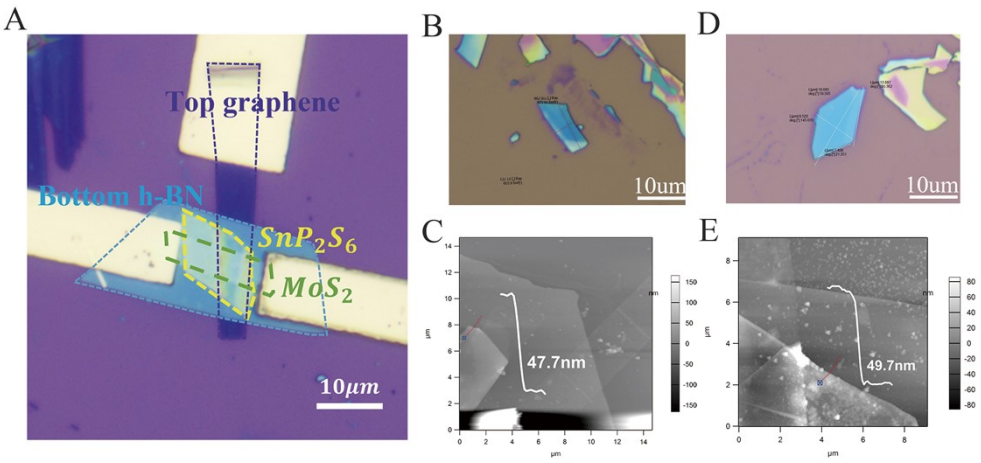


fig. S6. (A)Optical image of the FET device on h-BN substrate following the schematic of a top-gate FET. (B)(D) Optical images of SnP_2S_6 film on SiO_2/Si substrate, and (C)(E) the corresponding measured AFM profiles.

As shown in fig. S6 (B) and (D), the SnP_2S_6 sheet with estimated thickness of **48nm** was chosen to fabricate our FETs, and it shows a good gate tunability (details in **fig. S8**).

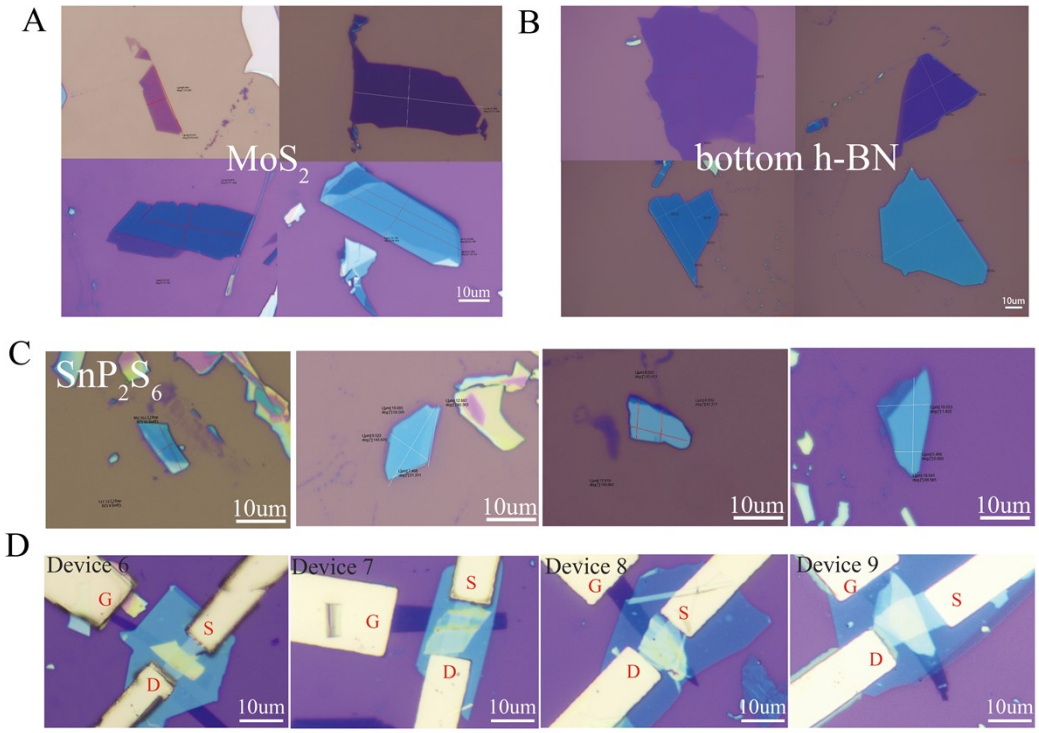


fig. S7. 2D materials obtained through a mechanical exfoliation process, and the FETs fabricated using the materials above. (A)(B) The optical image of MoS_2 sheets and h-BN substrate with different thicknesses, respectively. (C) Optical image of SnP_2S_6 sheets used as dielectric material in top-gate FETs. (D) Optical image of 4 SnP_2S_6/MoS_2 FETs on h-BN substrate using SnP_2S_6 sheets in (C), named **Device 6, 7, 8 and 9** respectively.

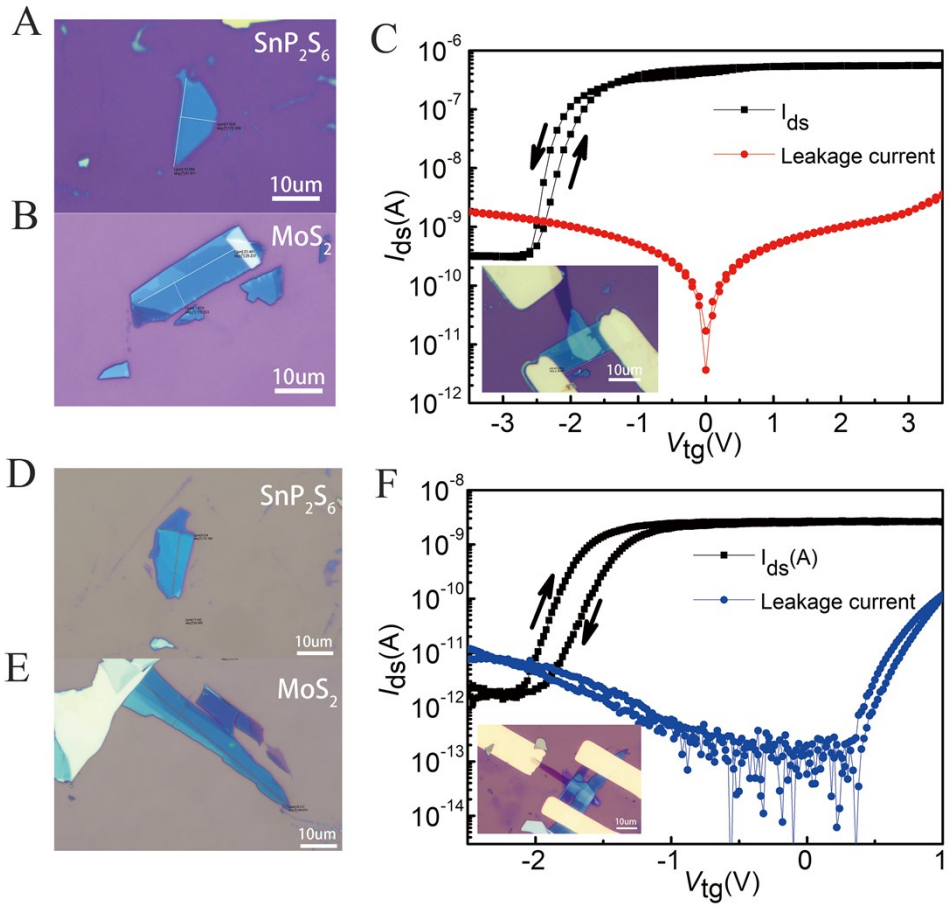


fig. S8. The SnP_2S_6/MoS_2 FETs on h-BN substrate with performance of a low ON/OFF ratio and a high leakage current. The FET using SnP_2S_6 in (A) and MoS_2 in (B) has a ON/OFF ratio of 10^4 and leakage current of 10^9 A shown in (C), and the FET using SnP_2S_6 in (D) and MoS_2 in (E) has a ON/OFF ratio of 10^3 and leakage current of 10^{10} A in (F).

As shown in **fig. S8** (C) and (F), these two FETs exhibit poor performances. We infer that the dielectric layer of MoS_2 FET is too small to regulate the carrier concentration in the channel, resulting in low ON/OFF ratio. Thus, it suggests the channel parts should be covered by SnP_2S_6 as much as possible. Meanwhile, the band gap of monolayer SnP_2S_6 is small, namely 2.23 eV[4], and the SnP_2S_6 used in these two FETs are very thin, leading to dielectric breakdown easily happen. Therefore, in our case, a SnP_2S_6 film with thickness about 49.7 nm was chosen to fabricate the device.

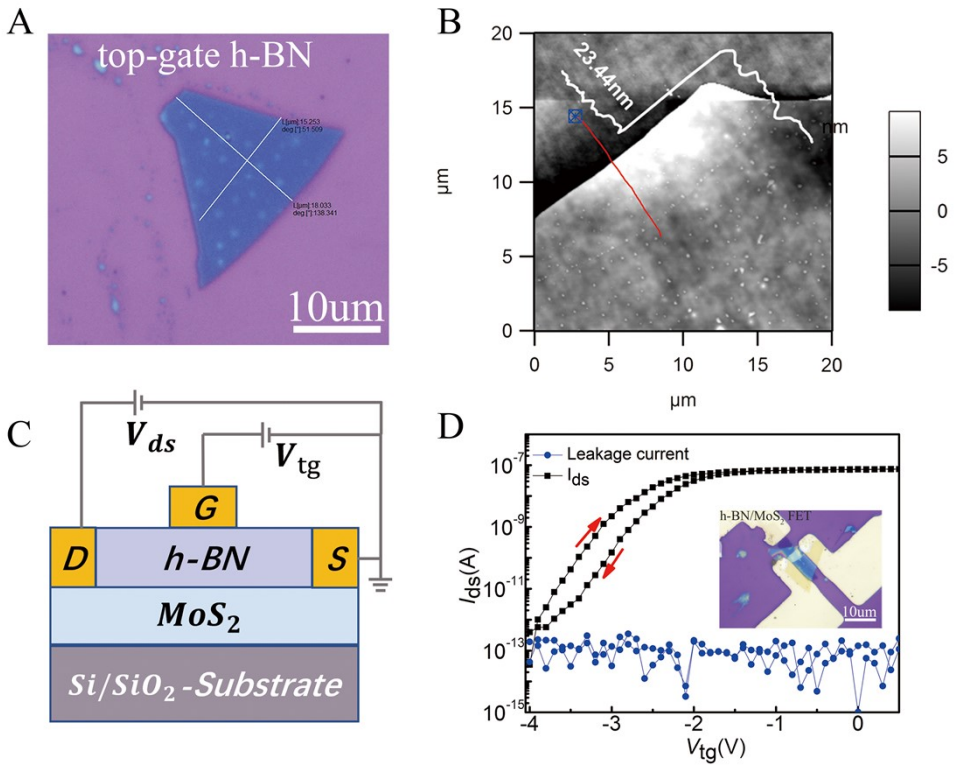


fig. S9. (A) Optical image of h-BN sheets used as dielectric material in top-gate FETs. (B) AFM profiles of h-BN sheet in (A). (C)Schematic of h-BN/MoS_2 FET on Si/SiO2 substrate (D) I_{ds}-V_{tg} curves of h-BN/MoS_2 FET on Si/SiO_2 substrate at 300K, and the inset shows optical image of the device.

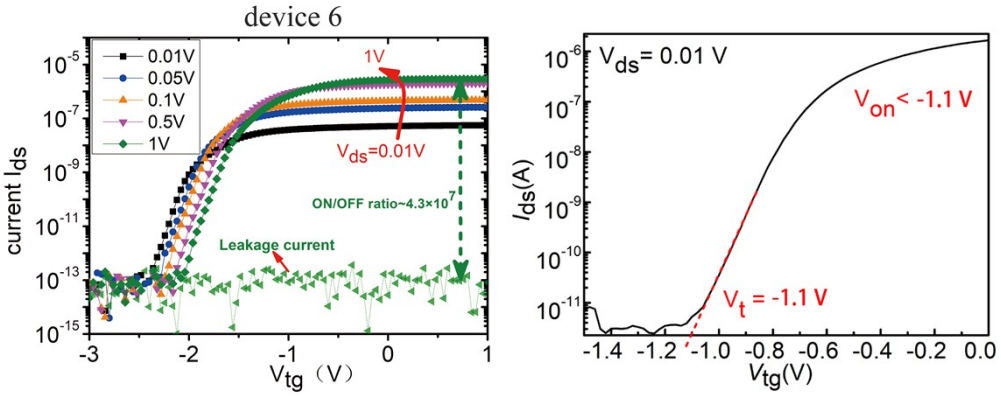


fig. S10. (A) I_{ds}-V_{tg} characteristics of device 6 in **fig.S9D** at various drain bias, where the high ON/OFF ratio of 10^7 is achieved at drain bias of 0.5 V and 1 V. The green dotted line shows low leakage current of 10^{-13} A at drain bias of 1 V. (B) Threshold voltage calculation of device 6. The value of Vt is as low as -1.1 V.

Device 6 shows high ON/OFF ratio of 10^7. What's more, we have calculated the carrier mobility of SnP_2S_6/MoS_2 FET (device 6) and h-BN/MoS_2 FET by the formula

$$\mu = \frac{L}{WV_{ds}} \times C \times g_m$$

where L and W are length and width of channel, C is the capacitance, and g_m is the transconductance. The SnP_2S_6/ MoS_2 device exhibits a high carrier mobility of 28.498 $cm^2V^{-1}s^{-1}$, while for h-BN/ MoS_2 device, a value of 4.344 $cm^2V^{-1}s^{-1}$ is obtained.

The power consumption of MOS transistor device can be calculated by formula

$$P = CV_{on}{}^2\alpha f + I_{leak}V_{on}$$

Where C is capacitance, Von is the working voltage of the device, α is a dynamic factor, f is the working frequency, I_{leak} is leakage current. According to this formula, the power consumption of transistor devices is mainly determined by the working voltage Von. The devices we fabricated show low threshold voltage of -1.1 V and low on voltage (**Figure R7**), which can reduce the switching power consumption without affecting high performance speed.

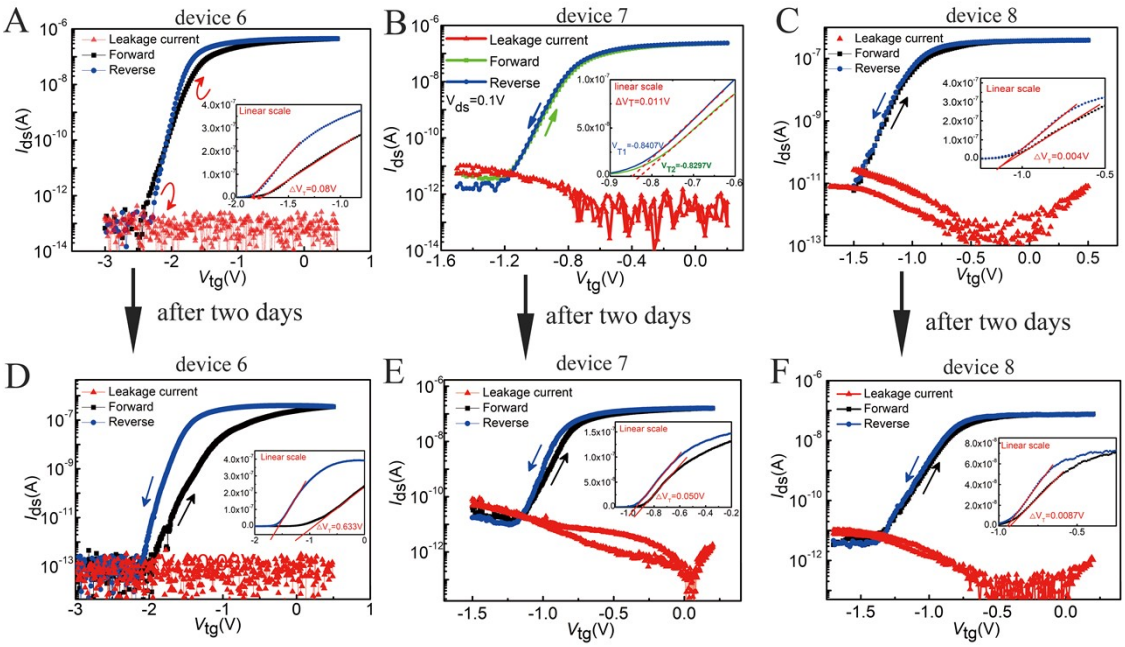


fig. S11. (A)(B)(C) Double-sweep I_{ds}-V_{tg} curves and leakage current of device 6, 7 and 8 mentioned in **fig. S9D**, respectively. The insets are the current in linear scale. While (D)(E)(F) show the corresponding I_{ds}-V_{tg} curves measured after two days in the glove box.

As we can see from **fig. S11 (A-C)**, the SnP_2S_6/MoS_2 devices on h-BN substrate show a varied hysteresis behaviors. **fig. S11(A)** demonstrates electrically tunable hysteresis crossover at room temperature (from clockwise (CW) at lower gate voltages to anti-clockwise (ACW) at higher gate voltages). This is likely induced by the gate-channel underlap areas, which engineers a differential response from traps near the channel-gate dielectric interface in the overlap and underlap gate regions, as reported in previous studies[5]. For the results in **fig. S11(B, C)**, both of device exhibit ACW at room temperature (RT), and I_{ds}-V_{tg} curves of the devices mentioned in **fig. S11(F)** show CW at RT, and so on. Based on the discussions above, it indicates that the devices show instable hysteresis behavior, which is possibly due to the underlap of the gate-channel region. Furthermore, during the fabrication process, impurities such as bubbles and absorbates may be introduced and form traps. Thus, during the fabrication, the coverage of the gate-channel should be big enough and the interface should be as clear as possible.

Subsequently, we test our devices in vacuum after placing the devices to the glove box two days. It is obvious that the ON/OFF ratio becomes very small, and the hysteresis gap becomes bigger, suggesting an increase of active defects. This behavior may be attributed to the trapping of carriers at interface and oxide defects which is produced by dissociative adsorption of oxygen and moisture on the surface of MoS_2[6]. Actually, these devices have been measured repeatedly and the electrodes have been partially damaged, so we indicate that the mechanical degradation of the electrode from multiple measurements are one of the likely causes for the decrease in performance.

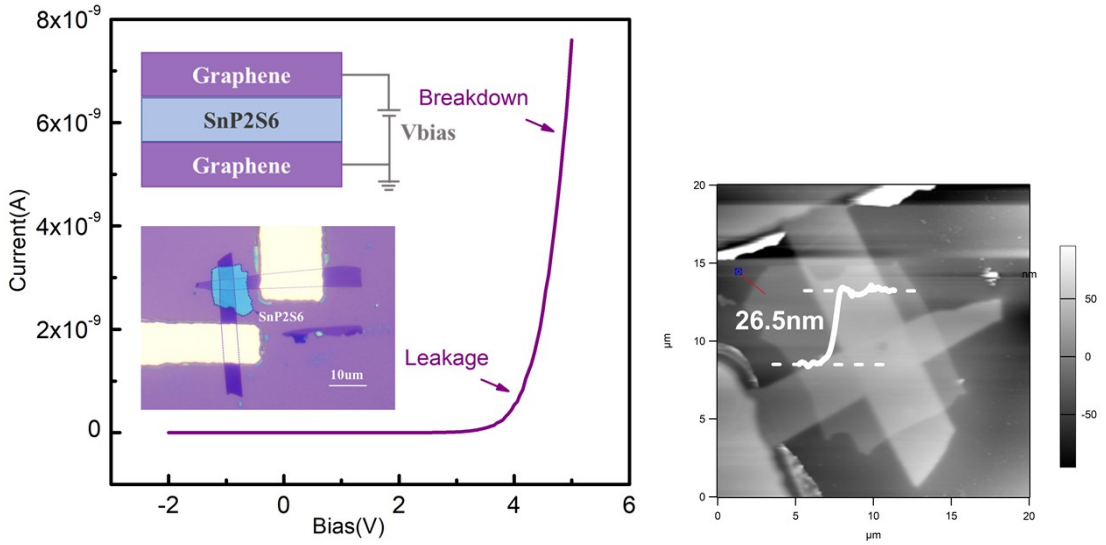


Fig.S12 Current leakage and breakdown measurement of the SnP_2S_6 film. For the material with thickness of 26.5 nm shown in the right, the breakdown voltage is around 5 V. Insets: schematic of the measurement device (top) and optical images of the measured devices (bottom). V_{bias} is the biased voltage applied on the top of device.

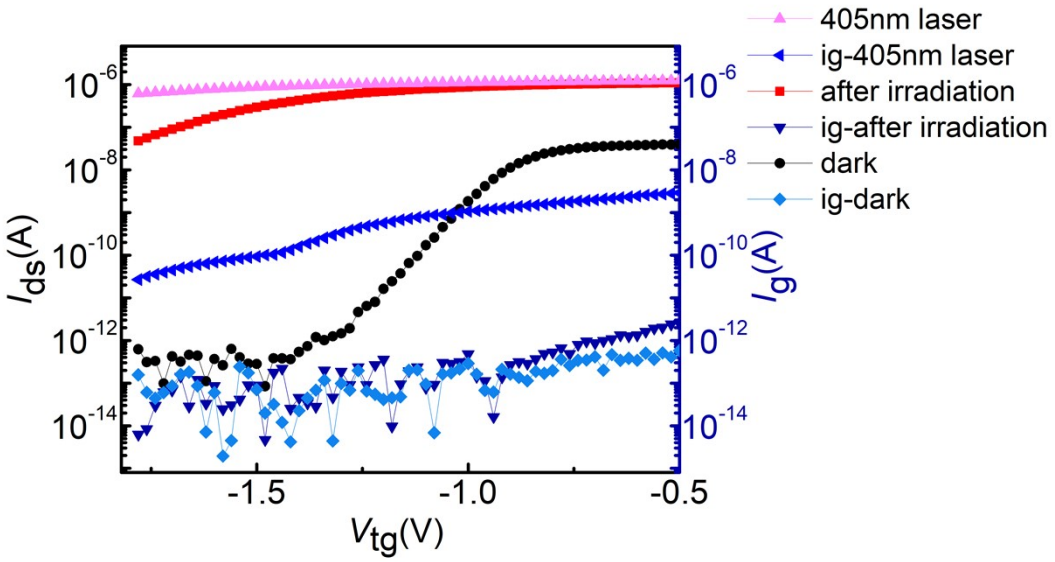


Fig.S13. Ids-Vtg curves and Ig-Vtg curves without light, under illumination of 405 nm laser and after irradiation.

The leakage current of the top-gated SnP_2S_6/MoS_2 FET was monitored under the conditions of darkness, illumination and after illumination, respectively. As shown in **Fig.s13**, the maximum leakage current under illumination is 10^9, far less than the photocurrent of which indicates SnP_2S_6 has little effect on the optical response of the device.

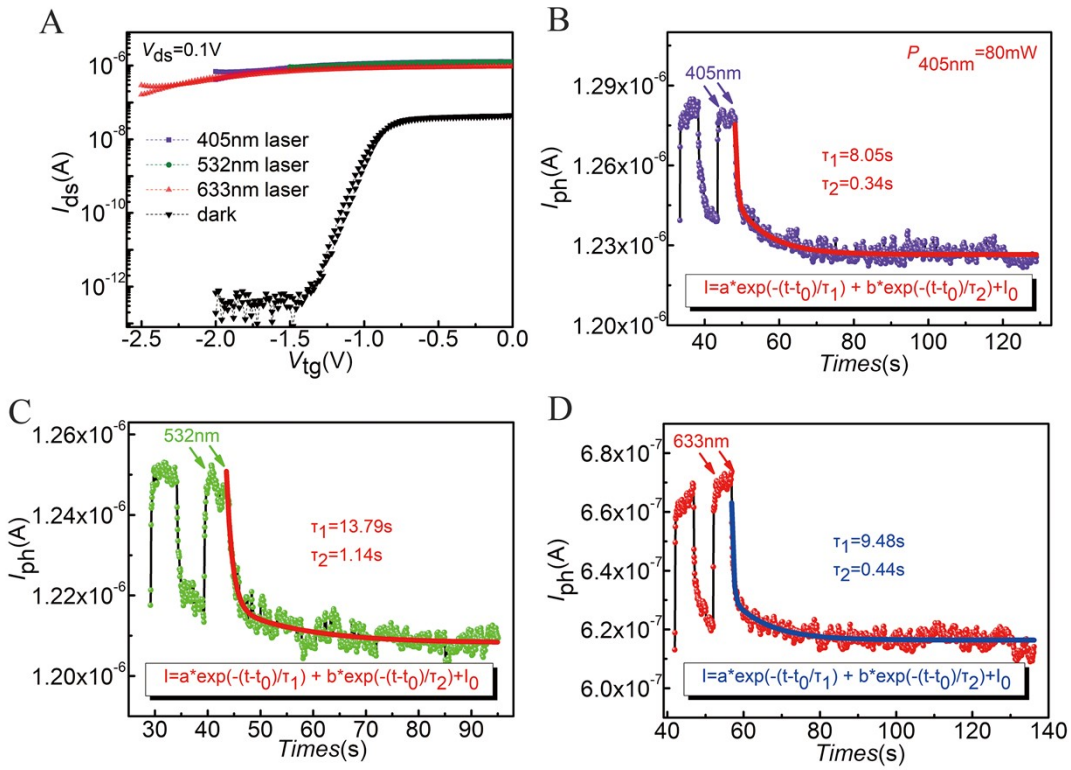


fig. S14. Transfer characteristics and transient properties of **Device 9** (on h-BN substrate) under laser irradiation with different wavelengths. (A) I_{ds}-V_{tg} characteristics at dark (Blue) and under 405 nm (Purple)/532 nm (Green)/633 nm (Red) irradiation, where the difference of photo response to different wavelengths is negligible. (B)(C)(D) The data is fitted with biexponential equation, and the time constants are attracted. Longer time constants of 8.66 s(B), 13.79 s(C) and 9.48 s(D) are obtained.

Since that **fig. S14** shows negligible distinction under the irradiation of 405 nm, 532 nm and 632 nm, we can conclude that the longer time constant caused by PG effect varies independently of the wavelength of laser.

Table 1. Detailed parameter of biexponential equation in **fig. S14**.

	t_0(s)	a	τ_1(s)	b	τ_2(s)	I_0(A)
B	47.88	2.22×10^{-8}	8.05	7.01×10^{-8}	0.34	1.23×10^{-6}
C	43.53	9.11×10^{-9}	13.79	3.45×10^{-8}	1.14	1.21×10^{-6}
D	55.95	1.54×10^{-8}	9.48	2.69×10^{-7}	0.44	6.16×10^{-7}

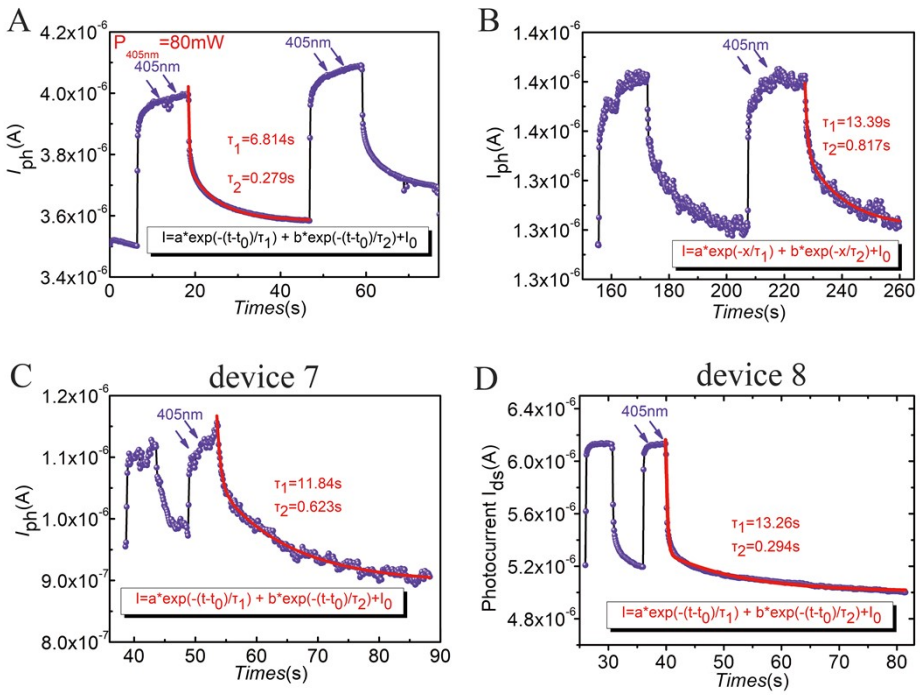


fig. S15. Transient property of the MoS_2 transistors under 405 nm laser irradiation, where data is fitted with biexponential equation. (A)(B) represent the channel current of two SnP_2S_6/MoS_2 FETs built **on Si/SiO_2 substrate.** (C)(D) show the channel current of two SnP_2S_6/MoS_2 FETs built **on h-BN substrate**. The longer relaxation time constants are separately 3.871 s(A), 13.39 s(B), 11.84 s(C) and 13.26 s(D).

fig. S15 shows that the longer time constants of FETs on h-BN substrate caused by PG effect, which is similar to that on Si/SiO_2 substrate. Thus, as discussed in main text, it is inferred that the long persistent photocurrent measured in our devices is not likely due to the traps at the MoS_2/SiO_2 or MoS_2/h-BN interface. The detained parameter of biexponential equation in **fig. S15** is Table 1.

Table 2. Detailed parameter of biexponential equation in **fig. S15**.

	t_0(s)	a	τ_1(s)	b	τ_2(s)	I_0(A)
A	18.14	1.81×10^{-7}	6.814	6.37×10^{-7}	0.279	3.58×10^{-6}
B	226.2	3.28×10^{-8}	13.39	9.12×10^{-8}	0.817	8.97×10^{-8}
C	52.96	1.64×10^{-7}	11.84	2.71×10^{-7}	0.623	8.97×10^{-7}
D	39.6	3×10^{-7}	13.26	2.04×10^{-6}	0.294	5×10^{-6}

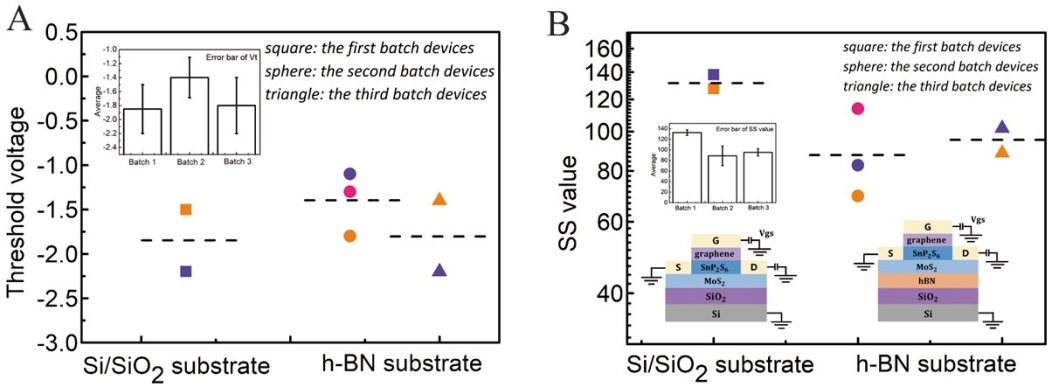


fig. S16. The good reliability and reproducibility of the devices. (A) The distribution of SS value for the devices. Inset: Schematic of the Si/SiO_2 substrate devices and h-BN substrate devices. Error bar of SS value for devices from three batches. (B) The distribution of threshold voltage for the devices. Inset: Error bar of threshold voltage for devices from three batches.

Device reliability and reproducibility are the key factors for future commercialization, so discuss these factors with seven as-prepared successful devices in total. In order to characterize the repeatability and reliability of the device, **Fig.S16** gives the distribution, average and error bar of SS value (A) and threshold voltage (B) of devices from three batches on two kinds of substrates (Si/SiO_2 and h-BN). There are two successful devices in batch 1 (Si/SiO_2 substrate), three successful devices in batch 2 (h-BN substrate) and two devices in batch 3 (h-BN substrate). The devices in the same batch show general reproducibility and uniformity with a less than 20% deviation from the average SS value and less than 0.5 standard deviation of threshold voltage. From batch to batch, there are errors associated with device performance. Initially, devices were built on Si/SiO_2 substrate (batch 1), which show higher SS value, higher threshold voltage and bigger hysteresis instability (as shown in **Fig.S5**) than devices on insulated h-BN substrate (batch 2 and batch 3).

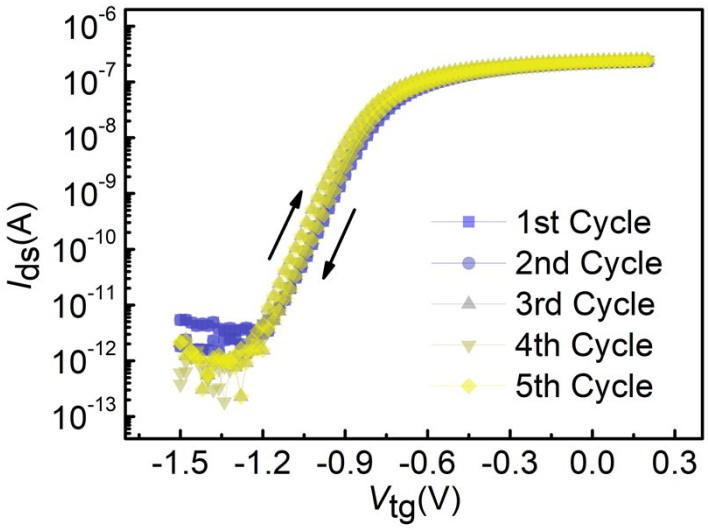


Fig. S17. The stability of the devices. Ids-Vtg characteristics of the device while applying a double-sweep voltage ranging from -1.5 V to 0.2 V and from 0.2 V to -1.5 V for five times. The arrows denote the sweeping directions.

As shown in **Fig.S17**, the stability and reliability of the device have been studied by applying a double-sweep voltage ranging from -1.5 V to 0.2 V and from 0.2 V to -1.5 V for five times. In the process of five sweeps, the transfer characteristic curves of the device almost coincide completely and have only a small fluctuation amplitude, which is caused by the instability from the equipment and environment during the sweep. The results show very low variability indicating that the FET device have good stability and reliability.

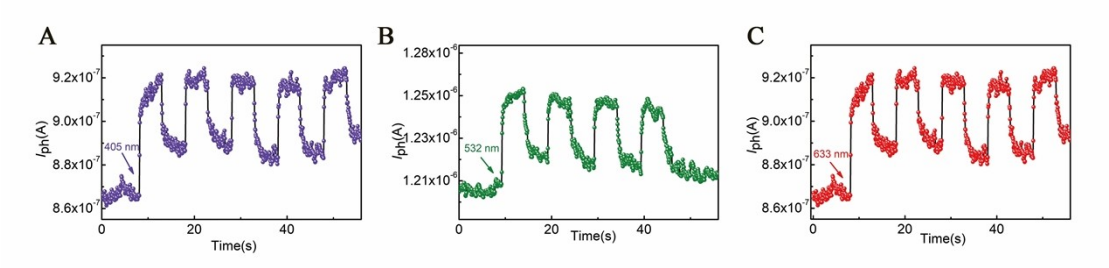


Fig. S18. Stability measurement of devices is studied by recording the optical response irradiated under different wavelengths laser (B) 405 nm, (C) 532 nm and (D) 633 nm, repeatedly.

As shown in **Fig.S18**, under the laser irradiation of different wavelength under periodic switch, the states of opening and closing for many times in i-t curves are recorded. The photocurrent and photogating effect of every switch are repeatable, which shows good stability.

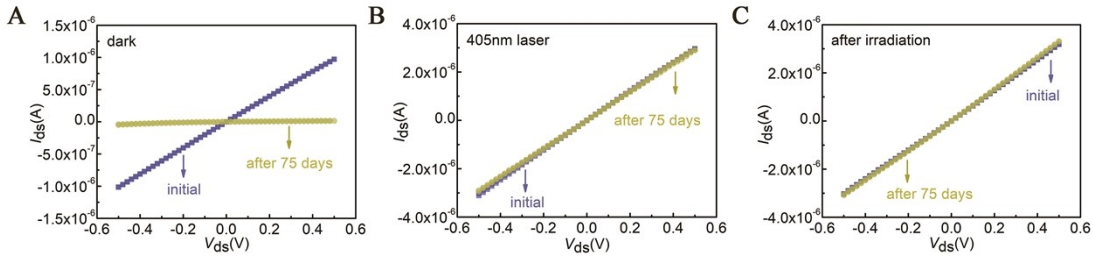


Fig. S19. Ids-Vds curves of initial (blue) and after 75 days (yellow). (A) Ids-Vds curve without light. (B) Ids-Vds curve under 405 nm laser illumination. (C) Ids-Vds curve after irradiation.

Furthermore, we have measured the device again after 75 days. As shown in **Fig.S19**, the current of the device without light has two orders of decrease compared to its initial state, which confirms the device instability in a long time. The device has not been encapsulated, and was exposed to laboratory environment. Charge trapping at the interface, adsorption/desorption of ambient molecules or oxygen and atmospheric moisture in the exposed active layers may cause the degradation of device performance. However, under the conditions of 405 nm laser illumination and after irradiation, the device shows similar optical response and photocurrent attenuation after 75 days. It's illumination that removes the defect traps and restores the device.

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