Supporting Information

Influence of Indium Tin Oxide Residues on Electrical Performance of hydrogenated amorphous silicon Thin Film Transistors in Backplane of Active Matrix Displays

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Orthogonal Design of ITO Thin-film Deposition

Table S1. Combination of parameters for $L_9(3^4)$ orthogonal test.

Note: **Table S1** was designed with the help of the software "Orthogonality Experimental Assistant" (Sharetop Software Studio).[1] *Y*ⁿ means a residual percentage of ITO in the etching area, and column C is a blank column used for checking the significance degree of the three parameters, in which parameter C has no actual values for I, II, and III. The I, II, and III are distributed according to the orthogonal principle, ensuring that the three experiments corresponding to each value of each parameter could be attributed to I, II, and III, such as ITO-s1~ITO-s3 with a deposition power of 10, 30, and 50 kW corresponding to I, II, and III, respectively. Multi-step deposition

(times) refers to dividing the original film deposition into several short parts without the final film thickness change. During each intermediate pause, turn off the power and maintain ventilation for 10 seconds. K_{ij} ($i=1-3$, $j=1-4$) means the sum of residual percentage of the samples adopting a same parameter level, where the subscript $i=1, 2$, 3 refers to the three values of each deposition parameter and the subscript $j=1,2,3,4$ corresponds to the deposition power, water vapor flow, multi-step deposition, and parameter *C*, respectively. For example, K_{II} is the sum of residual percentage of the samples obtained using a deposition power of 10 kW (i.e., ITO-s1, ITO-s2, ITO-s3), calculated as $K_{11} = (Y_1 + Y_2 + Y_3) = (10 + 2 + 1) = 13$, e.g., Y_1 represents the residual value of ITO-s1. *K²³* is the sum of residual percentage of the samples produced using a 2-steps deposition (i.e., ITO-s2, ITO-s4, ITO-s9), calculated as $K_{22} = (Y_2+Y_4+Y_9) = (2+60+45)$ =107, e.g., *Y²* represents the residual value of ITO-s2.

Table S1 lists nine experimental parameter combinations based on the orthogonal arrangement principle with the help of the software "Orthogonality Experimental Assistant" (Sharetop Software Studio).[1] The orthogonal arrangement principle means that the significant effect of all these parameters can be investigated without considering their interactions since the interactions are uniformly distributed in each column.[2] The three-parameter three-value orthogonal design consists of four discussed parameters, i.e., deposition power, water vapor, multi-step deposition and parameter *C* in this study. Parameter *C* was kept empty to analyze the effect of random errors on the experimental results, $[3]$ which can evaluate the significance level of the other three parameters.[4]

Range Analysis and Variance Analysis of ITO Residual Percentage

The mathematical analysis of $L_9(3^4)$ orthogonal experiment includes the range analysis and the variance analysis of the residual percentage:

(1) The range analysis was used to assess the various trends of the average residual percentage with the increase of respective parameter values. The average residual rate of a value of a parameter is denoted as \overline{K}_{ij} , in which *i*, ranging from one to three, denotes the values of respective processing parameters and *j* represents the four discussed parameters (e.g., *K¹¹* is the average residual value of ITO-s1-3 using a deposition power of 10 kW). \overline{K}_{ij} is calculated by taking average residual value of the three samples for a same parameter value using Eq. S-1.

$$
\overline{K_{ij}} = \frac{1}{3} \sum_{i=1}^{9} Y_n
$$
 (S-1)

Where the subscript *i*=1,2,3 indicates the three values of each deposition parameter, the subscript *j*=1,2,3,4 corresponds to the deposition power, water vapor flow, multistep deposition, and parameter *C*, respectively. For example, \overline{K}_{11} is an average sum of residual percentage of three samples using same deposition power of 10 kW (i.e., ITOs1, ITO-s2, ITO-s3), calculated as $K_{11} = 1/3*(Y_1+Y_2+Y_3)=1/3*(10+2+1)=4$, e.g., Y_1 represents the residual value of ITO-s1.

(2) The variance analysis was performed to identify the most relevant parameters on etching residues. In the $L_9(3^4)$ orthogonal experiment, the sum of mean deviation squares of the parameters' residual percentage is denoted as *SS^j* (i.e., deposition power, water vapor, multi-step deposition and parameter C) and is calculated using Eq. 2 in the manuscript. Then, F rate value was defined as the ratio of SS_i of three deposition parameters and *SS4*, which is the sum of mean deviation squares of parameter C (Eq. 3 in the manuscript). F_α is the standard value in variance analysis used to judge the correlation between parameters and etching residue, which can be gained from the *F* distribution table invented by George Snedecor, according to the freedom degree of parameters and significance level α . [5-8] In the L₉(3⁴) orthogonal design, α is a statistical concept and usually takes a value of 0.1, which indicates a 10% risk of concluding that a difference exists when there is no actual difference.[9] Subsequently, *F* rate of three deposition parameters is compared with the standard *F* value (*Fα*). A parameter has a significant effect when *F rate* is larger than the standard value *Fα*. Alternatively, the parameter has no significant impact on the test results if *F*≤*Fα*.[4, 10]

Methods for Measuring and Calculating Internal Stresses of Gate and SiN^x Layers

The silicon wafers used for stress measurement were attached to clean glass substrate with high-temperature double-sided adhesive tape, and went through the fabrication of ITO film electrode, Al/Mo gate electrode, and SiN_x insulating layer together with the glass substrate.

FLX-2320 film stress measurement system was used to calculate the layer internal stress by measuring curvature radius variation of the silicon wafer before and after film deposition. Twelve points of internal stress for each layer were measured at different locations on the entire glass substrate, and the average value was taken. The internal stress is calculated using Eq. S-2:

$$
\sigma = \frac{1}{6R} \times \frac{E}{(1-\mu)} \times \frac{d_{\text{sub}}^2}{d}
$$
 (S-2)

Where σ and d represent the internal stress and thickness of the layer, respectively. E , *μ*, and *dsub* are the Young's modulus, Poisson's ratio, and thickness of the silicon wafer, respectively. *R* is the relative radius of silicon wafer curvature after film deposition and $R=R_1R_2/(R_1-R_2)$, R_1 and R_2 are the curvature radii of the silicon wafer before and after film deposition, respectively.

Fig. S1. Distribution of twelve stress tests of silicon wafers for Al/Mo gate and SiN_x layers on glass substrate.

Table S2. FWHM values of {222} crystal plane of ITO-s5 and ITO-s7~9 films after

deposition and annealing.

Note: The origin software fits the FWHM value of the {222} crystal plane. ITO-s1-4 and ITO-

s6 have no FWHM value after deposition because there is no diffraction peak at $2\theta = 32.3^{\circ}$.

Fig. S2. (a) SEM top view and (b) cross-sectional images of TFT-s3.

Fig. S3. TFT sample used to measure TFT electrical properties.

Fig. S4. AFM topographies of ITO films: (a) ITO-s1, (b) ITO-s4, (c) ITO-s5, (d) ITOs6, (e) ITO-s8, and (f) ITO-s9.

Fig. S5. SEM residue morphologies of etched areas of (a) ITO-s1, (b) ITO-s4, (c) ITO-s5, (d) ITO-s6, (e) ITO-s8, and (f) ITO-9, after lithography and wet etching.

Fig. S6. SEM residue morphology and EDX spectrum of etched areas of ITO-s7, after lithography and wet etching.

Fig. S7. ITO residue distribution of ITO-s7 electrode on the glass substrate, where red area indicates the residue.

Fig. S8. Total yield rate of vehicle displays based on TFT-s3 and TFT-s7, as well as the rate of dark-area defect of TFT-s3 and TFT-s7. Note: Total yield rate of vehicle display for TFT-s3 is not 100% is due to some display defects unrelated to our experiment.

Fig. S9. (a) Transfer characteristics (forward and reverse), (b) Current switching ratio I_{on}/I_{off} , and (c) V_{th} and mobility of TFT-s1, TFT-s4-6, and TFT-s9.

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