Supporting Information

High on/off ratio SiO$_2$-based memristors for neuromorphic computing: Understanding the switching mechanisms through theoretical and electrochemical aspects

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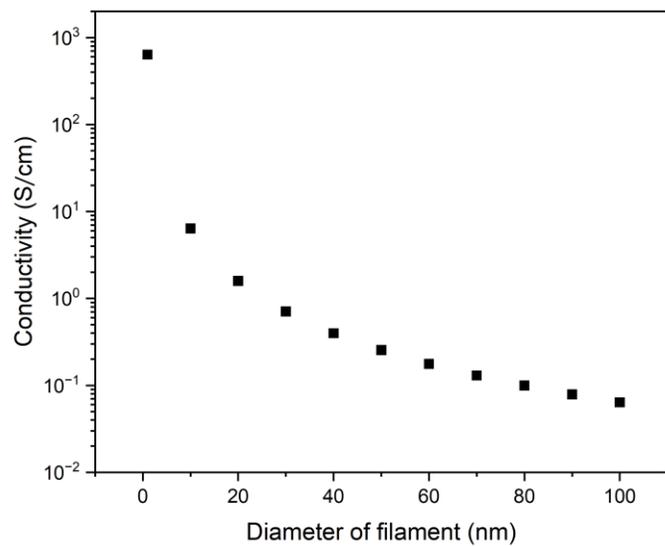
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Figure S1. The estimated filament conductivity as a function of the filament size.
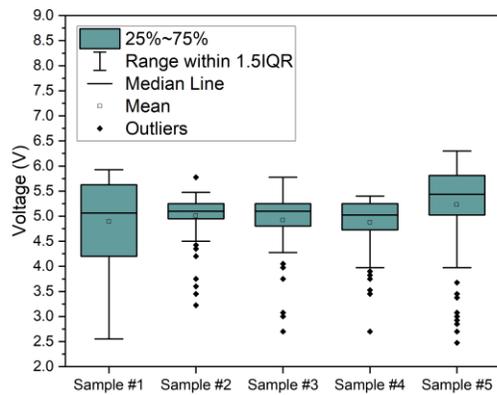
Figure S2. The statistical distribution of SET voltages for 5 different devices. The median SET voltages of these devices were extracted from the statistical distribution, by which very small variation of 2.90% is determined for device-to-device SET voltages.
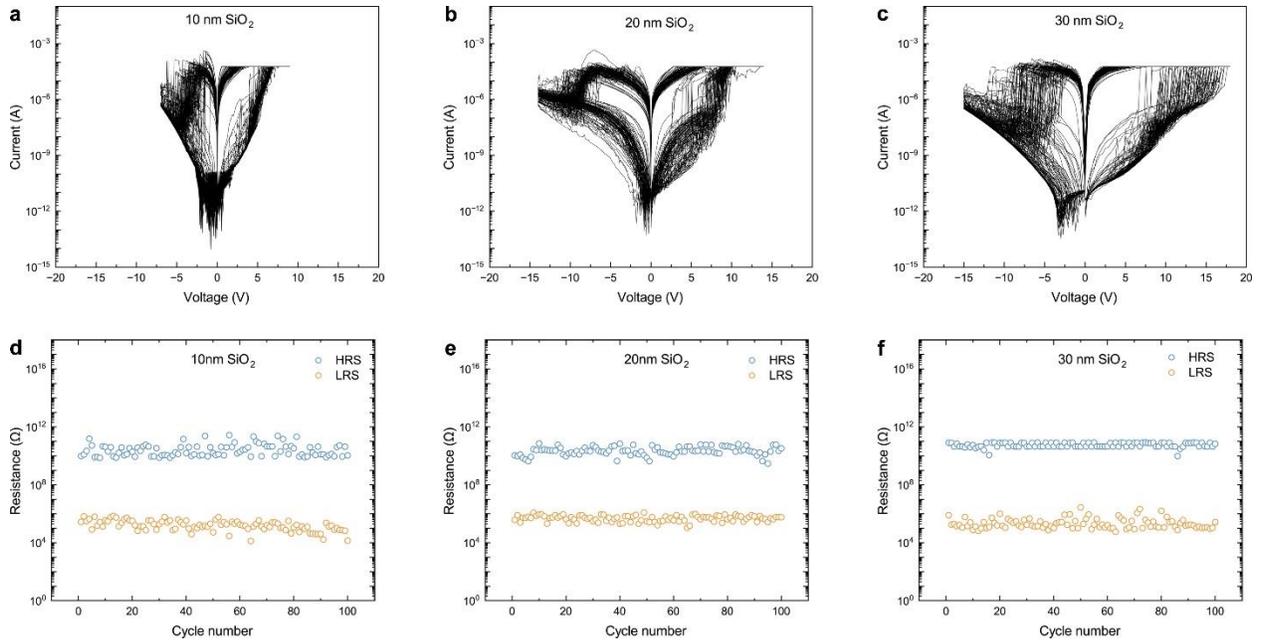
Figure S3. (a) - (c) are 100 cycles of I-V DC sweeping characteristics of different thicknesses of SiO2 switching layer. (d) – (f) are associated endurance characteristics, the read voltage is 0.3 V.

Figure S3a-c shows the I-V characteristics of devices with different thicknesses of the SiO_2 switching layer. All devices show typical bipolar non-volatile resistive switching behavior. Figure S3d-f shows associated endurance characteristics, indicating good reliability without any decay of LRS and HRS and high on/off ratio of 10^4-10^5. Increasing switching layer thickness requires higher SET voltage. The corresponding statistical summarization for the variational SET voltage requirements has been displayed in Figure 2f of the main text.
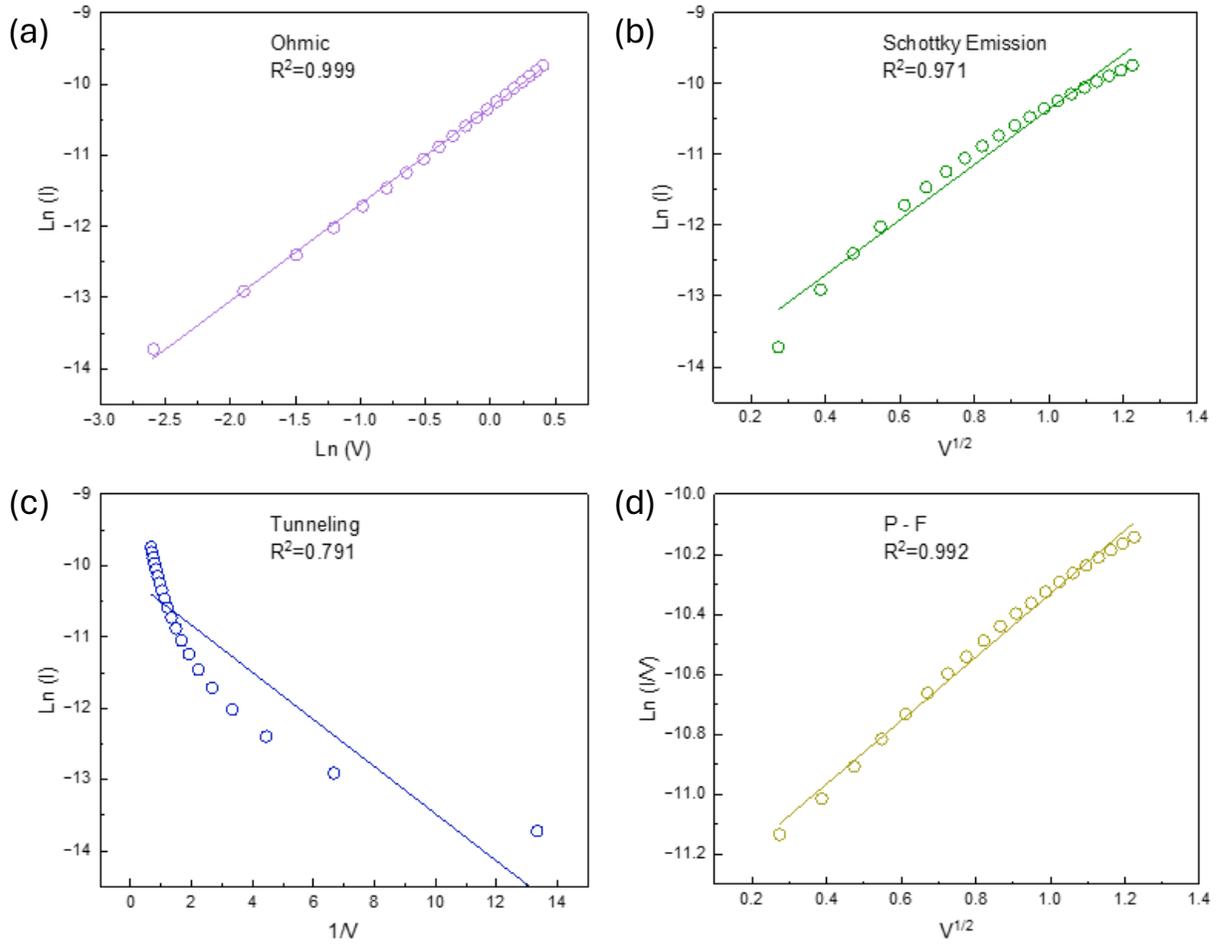
Figure S4. The fittings with different current transport mechanisms. All R square values are labeled.

We revisited our data and conducted additional examinations of other current transport mechanisms, including Schottky emission, tunneling, and Poole-Frenkel (P-F) emission.[1] We compare the Ohmic conduction in the main text with these three other mechanisms in Figure S4. All R square values are labeled in Figure S4, and it is observed that the Ohmic conduction has the best fit where the R square value is 0.999.
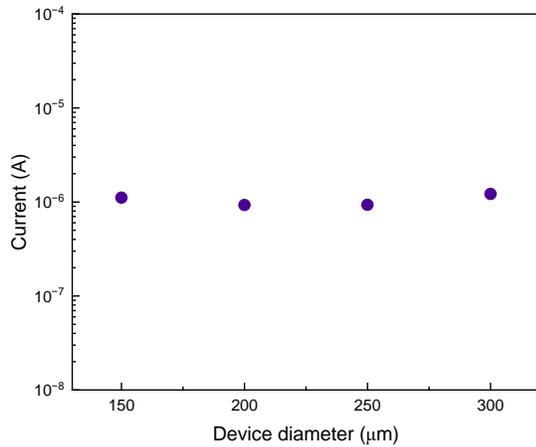
Figure S5. The current values at LRS for four different sizes (areas) of devices: 150, 200, 250 and 300 μm are the diameters of devices.

The analysis of area scaling was conducted, and our results in Figure S5 show that the current levels in the LRS do not significantly vary with the size of the electrode, suggesting the presence of filamentary conduction.[2] This result (i.e., no significant size effect on the performance) is further supported by several reports available in the literature where similar results were obtained from $SiOx$, Ta_2O_5 and IGZO-based memristors. [2]
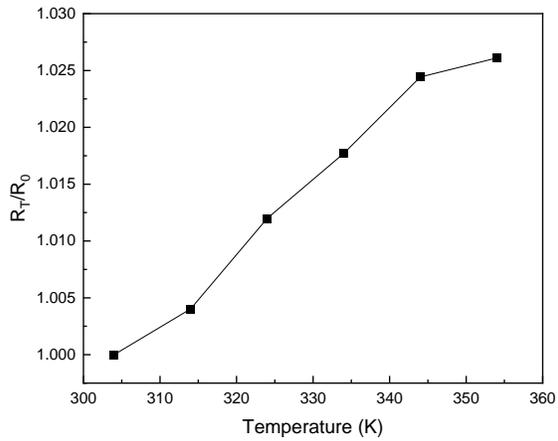
Figure S6. Temperature dependence of the LRS. Measurement temperatures ranged from 304 K to 354 K.

To further substantiate the qualitative analysis of conductive filament formation, we assessed how the temperature affects the samples, measuring their temperature dependence from 304 K to 354 K. To enable a consistent comparison, we adjusted the resistance values to a standard by normalizing them with the value at initial temperature (304 K) in every instance. The results in Figure S6 show that the resistance values increase along with the increase in temperature, a metallic characteristic, indicating the filament is established at LRS.[3]

Figure S7. The oxygen vacancy evolution and the electric field distribution of memristor with 10 nm SiO$_2$ switching layer at different stages.

Figure S8. The oxygen vacancy evolution and the electric field distribution of memristor with 20 nm SiO_2 switching layer at different stages.

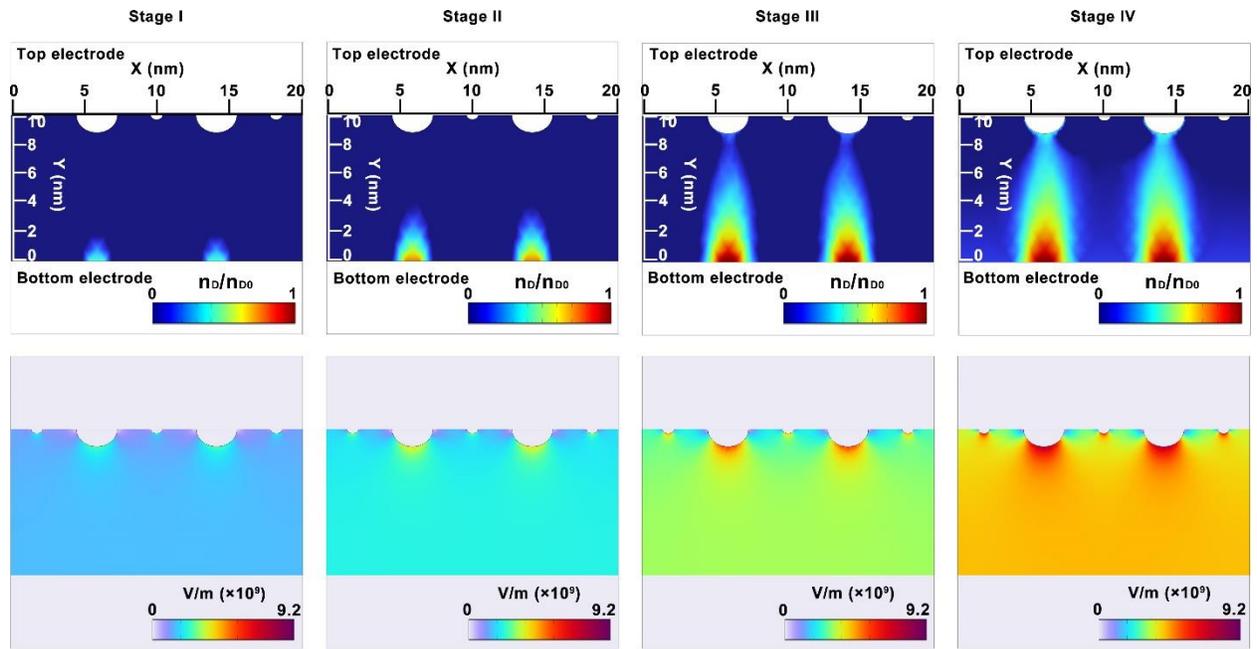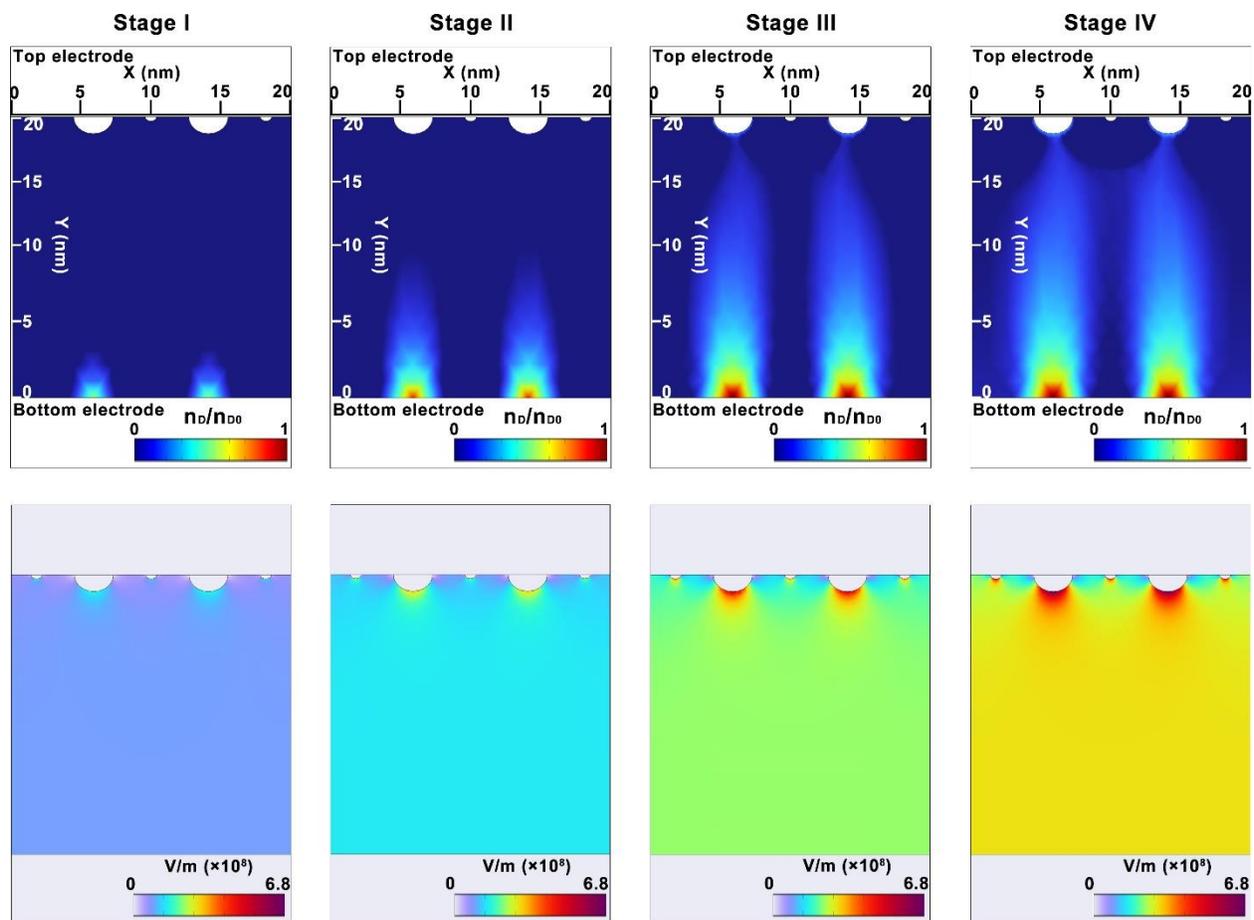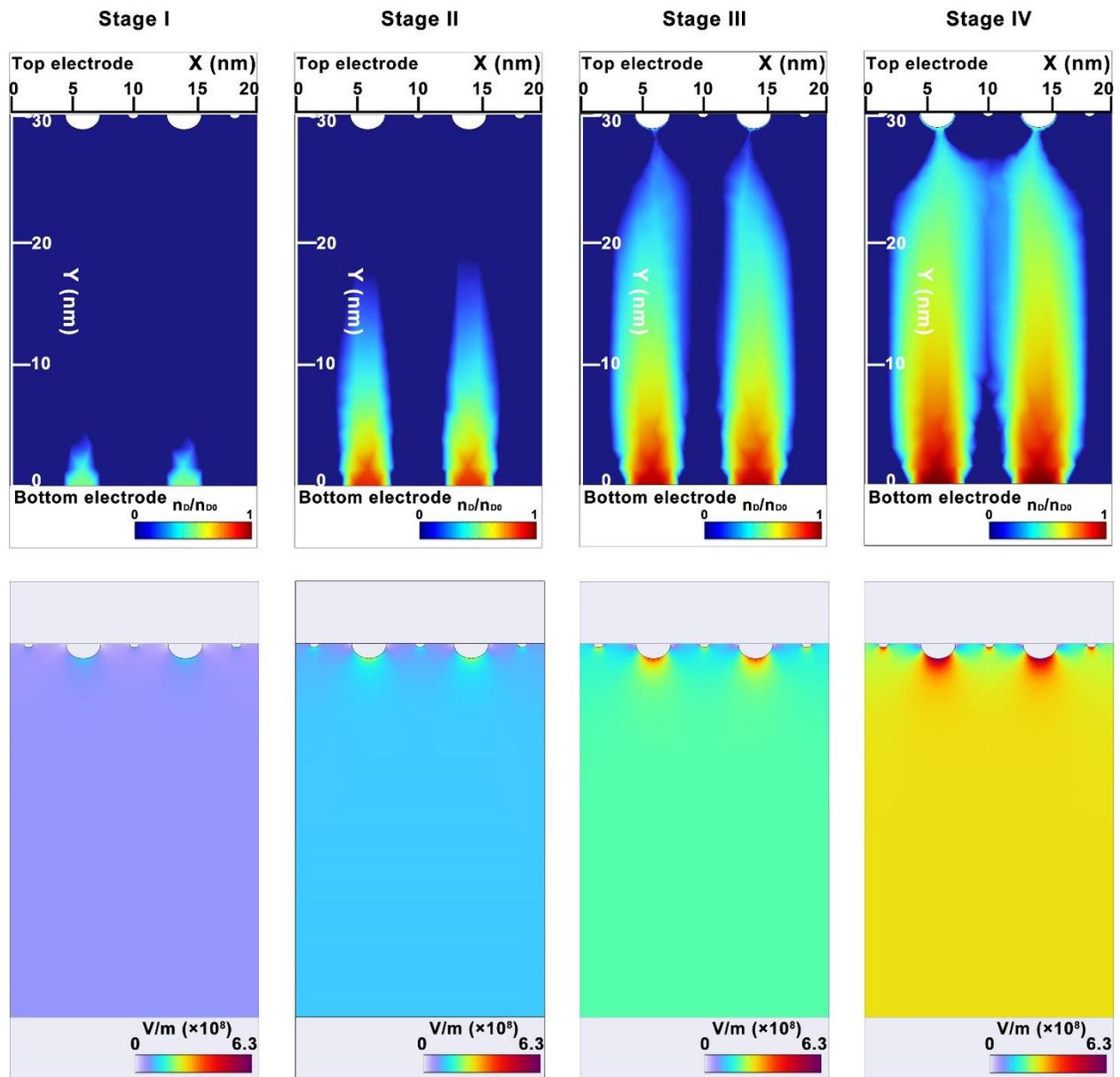**Figure S9.** The oxygen vacancy evolution and the electric field distribution of memristor with 30 nm SiO$_2$ switching layer at different stages.
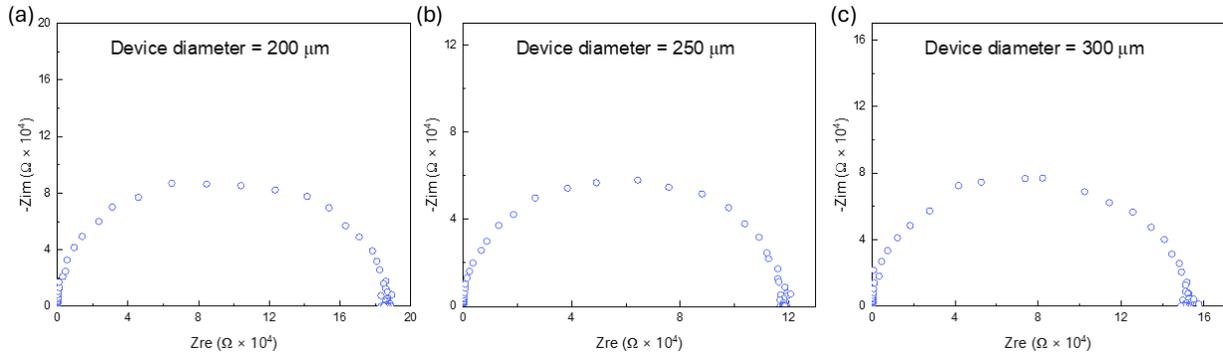
Figure S10. The Nyquist plots from EIS measurements on devices with top electrodes having diameters of 200 µm, 250 µm, and 300 µm at LRS, where no significant size effects on the device performance (conductance) is identified.

The Nyquist plots in Figure S7 for devices with top electrodes having diameters of 200 µm, 250 µm, and 300 µm are presented within this section, showing semicircle characteristics like the one observed for the 150 µm. These findings reinforce our proposed filamentary switching mechanism detailed in area effect study in Figure S5.
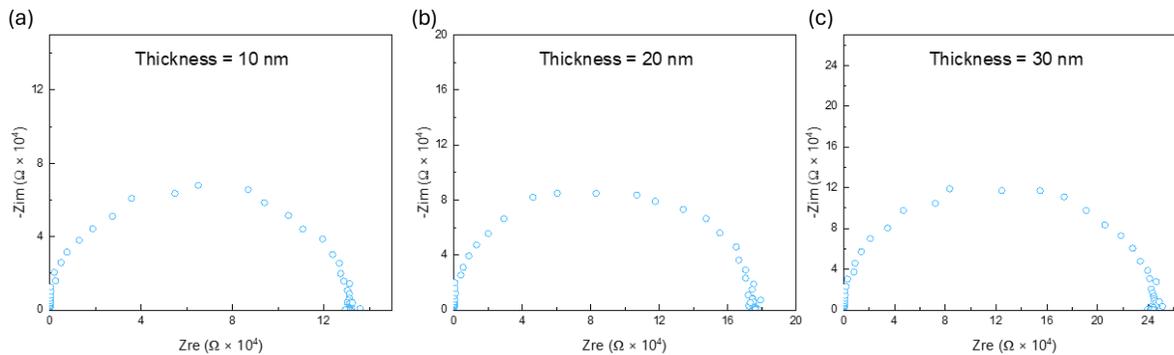
Figure S11. The Nyquist plots from EIS measurements on devices with thicknesses of (a) 10 nm, (b) 20 nm, and (c) 30 nm at LRS.

The Nyquist plots for devices with thicknesses of 10 nm, 20 nm, and 30 nm at LRS exhibit semicircles similar to those observed for the 5 nm device, indicating the presence of filaments. This observation is consistent with the results from our Finite Element Analysis in supporting information.
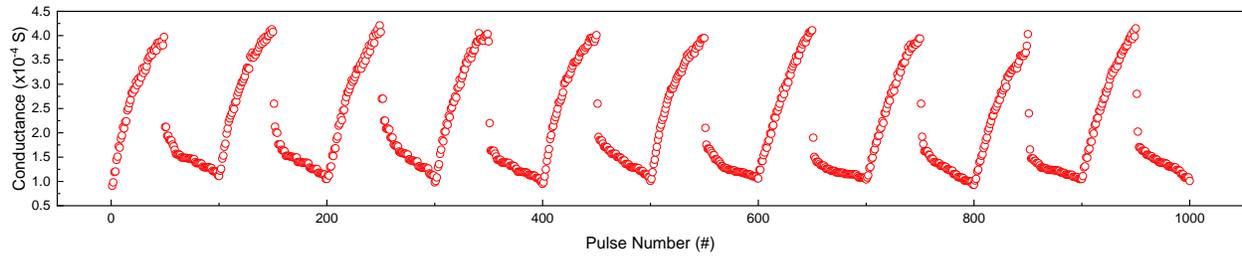
Figure S12. 10 cycles (a total of 1000 pulses) of LTP and LTD behaviors are achieved from our SiO$_2$-based memristor, demonstrating consistent repeatability with a relatively linear potentiation behavior and a less linear trend in depression.
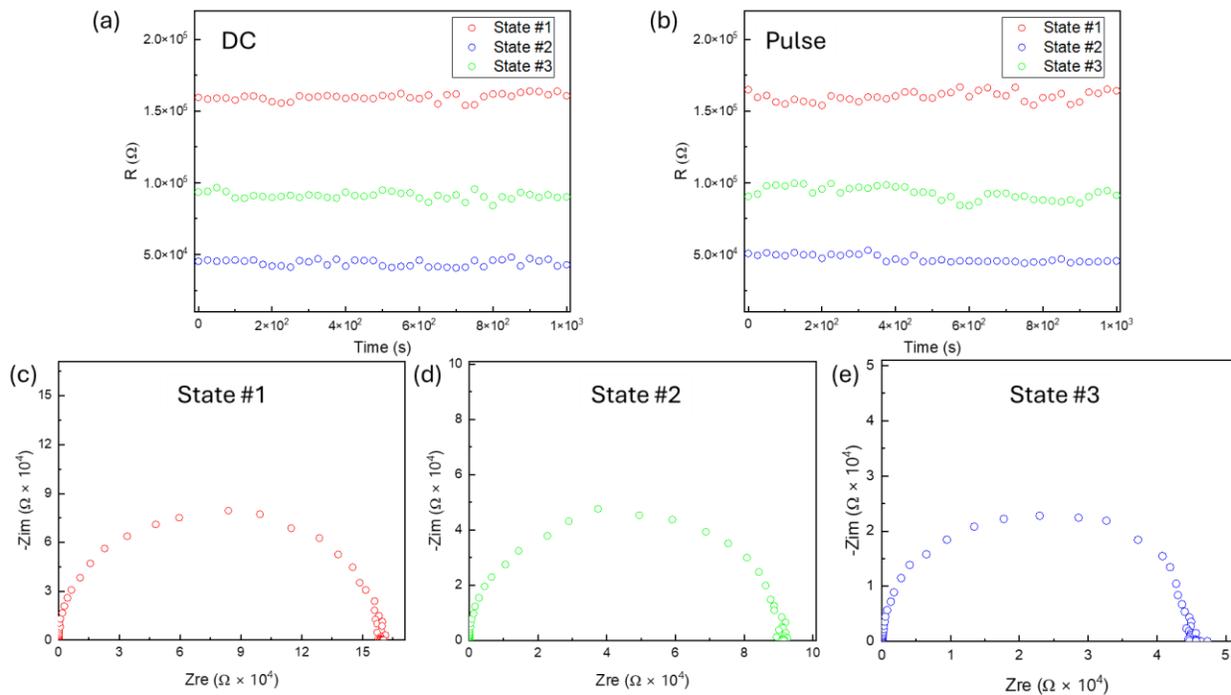
Figure S13. The retention characteristics for three different conductance states evaluated with (a) DC and (b) pulse. The Nyquist plots from EIS measurements at (c) state #1 (d) state #2 (e) state #3.

Table S1. Comparisons of retention and endurance.

	Retention (s)	Endurance by DC (number of cycles)
HfOx Work1[4]	3.6×10^3	100
HfOx Work2[5]	1×10^2	100
HfOx Work3[6]	2×10^4	1000
TaOx Work1[7]	2×10^4	100
TaOx Work2[8]	$<1 \times 10^4$	N/A
TaOx Work3[9]	1×10^4	100
SiOx Work1[10]	N/A	1000
SiOx Work2[11]	3×10^3	800
SiOx Work3[12]	1×10^4	N/A
SiOx This Work	1×10^4	100

Table S2. Comparison of Asymmetric Non-Linearity (ANL) of different materials systems.

Switching Layer	Si[13]	HfO$_2$[14]	Cu$_2$O[15]	TaOx/TiO$_2$[16]	MoS$_2$[17]
Asymmetric Non-Linearity Factor (ANL)	0.30 to 0.59	0.843 to 0.959	0.12 to 0.71	0.70	0.55

Note S1. Physical Modeling detail

The 2D physical model for the turn-on process of the memristor was carried out through a numerical solver. All equations and definitions of the parameters employed in this simulation were referenced from the previous work. The simulation process was simplified by only considering the drift/diffusion migration of the $V_{\ddot{O}}$. The concentration of $V_{\ddot{O}}$ was described by the model proposed by Mott and Gurney, which can be expressed as the following continuity equation:

$$\frac{\partial n_D}{\partial t} = \nabla \cdot (D\nabla n_D - vn_D + DSn_D\nabla T) \tag{S1}$$

Here, D is the diffusion coefficient and given by $D = \frac{1}{2} \cdot a^2 \cdot f \cdot e^{\frac{-E_a}{kT}}$, where f is the escape-attempt frequency, a is the effective hopping distance and E_a is the activation energy for migration. v represents the drift velocity and is expressed by $v = a \cdot f \cdot e^{\frac{-E_a}{kT}} \cdot \sin h(\frac{qaE}{kT})$. S is the Soret coefficient, which can be expressed by $S = -\frac{E_a}{kT}$. $D\nabla n_D$, vn_D and $DSn_D\nabla T$ represent the Fick diffusion flux, drift flux, and Soret diffusion flux, respectively. Equation (S1) can be solved when coupled with the current continuity equation (S2) for electrical conduction and the steady-state Fourier equation (S3) for Joule heating as indicated below:

$$\nabla \cdot \sigma\nabla\psi = 0 \tag{S2}$$

$$-\nabla \cdot k_{th}\nabla T = J \cdot E = \gamma \cdot \sigma|\nabla\psi|^2 \tag{S3}$$

Here, σ is the electrical conductivity and defined by the Arrhenius equation, $\sigma = \sigma_0 \cdot e^{\frac{-E_{AC}}{kT}}$, in which σ_0 is a pre-exponential factor and E_{AC} is the activation energy for conduction. k_{th} is the thermal conductivity, which can be expressed as $k_{th} = k_{th0}(1 + \lambda(T - T_0))$.

In the actual calculations, the SiO_2 layer thickness, which is sandwiched by the top electrode (5 nm) and the bottom (5 nm) electrode, was considered for 5, 10, 20, and 30 nm. The width (i.e., x-axis dimension considered in the simulation) of all layers is 20 nm. 6 protrusions with a radius of 0.3, 0.6, and 1 nm are placed at the boundary between the bottom electrode and the SiO_2 layer to simulate the surface heterogeneity. The temperature at the top electrode, SiO_2 layer, and bottom electrode is set to 300 K. The filaments are formed by applying a constant voltage to the top electrode and grounding the bottom electrode. n_D, ψ, and T can be acquired by solving the partial differential equation (S1), (S2), and (S3).

Note S2. Image Processing detail

In our image recognition tests, we utilize a multilayer perceptron (MLP) implemented with PyTorch, a popular deep-learning library known for its comprehensive tools for neural network development and training. The MLP architecture consists of an input layer with 784 neurons, corresponding to the dimensionality of the flattened input figures. The hidden layer comprises 500 neurons, and the output layer consists of 10 neurons, representing the 10 different classes in the classification task.

For weight initialization, we employ Kaiming's initialization, a widely used technique that initializes the weights of the neurons. The biases are initialized to zero, a common practice in many neural network implementations. To introduce non-linearity into the network, we utilize the rectified linear unit (ReLU) activation function for all neurons in the hidden layers.

To optimize the MLP, we employ stochastic gradient descent (SGD) as the optimizer, with a learning rate of 0.001. SGD is a popular optimization algorithm that iteratively adjusts the weights and biases based on the computed gradients in mini-batches to minimize the loss function. The chosen loss function for this multi-class classification problem is cross-entropy, which measures the discrepancy between the predicted class probabilities and the true labels.

The training process is conducted using batches of size 64, a common practice that balances computational efficiency and model convergence. For evaluation, we utilize the MNIST and Fashion-MNIST datasets, both well-known datasets for image classification tasks. The datasets are randomly shuffled, and an 80:20 train-test split is applied, ensuring that the model's performance is assessed on unseen data. The training set is used for model training, while the test set is used to evaluate its generalization ability and overall performance. The number of training

epochs is set to be 2000, which is chosen based on experimentation and observations of

achieving high accuracy without overfitting the training data.

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