Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Carrier Tuning of 2D Electron Gas Field-Effect Devices Based on Al_2O_3/ZnO Heterostructures

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As shown in Figure S1, the Al_2O_3 layer is in amorphous state, and the ZnO films are polycrystalline (improved crystallization observed with 25 nm thickness sample). As discussed in the main text, the electron accumulation at the interface of Al_2O_3/ZnO heterostructure is free from "polar catastrophe" with charge mismatch effect, and can be explained by redox reaction at the ZnO surface during Al_2O_3 deposition. The selected area electron diffraction and fast Fourier transform (FFT) in Figure S2 indicate the (101), (002), and (100) planes of wurtzite for 7.5 nm annealed ZnO film.

Figure S3 shows the X-ray photoelectron spectroscopy (XPS) spectra of 7.5 nm annealed ZnO with and without Al_2O_3 overlayer. The Zn 2p XPS spectra of Al_2O_3/ZnO is obtained at the depth near the interface of Al_2O_3/ZnO by using Ar etching. The Zn 2p peak around 1022 eV is deconvoluted into two Gaussian curves of Zn species: O-deficient $Zn^{0\text{-}1+}$(1021.8 eV), and full oxidation Zn^{2+} (1022.3 eV). Compared to the single-layer ZnO, the Al_2O_3/ZnO shows an increased ratio of $Zn^{0\sim1+}/Zn^{2+}$ peak area, which suggests that more $Zn^{0\sim1+}$ species are induced in the interface due to the chemical reduction on the ZnO surface.

From Figure S4, the generated electrons show a carrier density of ~2×10^{14} cm^{-2} and Hall mobility of 20~30 $cm^2V^{-1}s^{-1}$ after 25 cycles of ALD Al_2O_3 (~2.5 nm), which remains stable with thicker Al_2O_3 thickness. Figure S5 shows the temperature-dependent conductivity for Al_2O_3/ZnO. According to the slope of the Arrhenius curves, the activation energy (E_a) for electrons released from Vo-related donor levels is larger in thinner as-grown ZnO films, which has great impact on the carrier density of 2DEG.

The energy band diagrams of Al_2O_3/ZnO-based FET with top gate and back gate modes are shown in Figure S6 to further understand the operation principle of 2DEG FETs. Top gate and back gate manipulate the bottom and tail electrostatic boundary conditions of the asymmetric

quantum well, respectively. Figure S7 compares the drain current (I_D) of the back-gate FETs with annealed and as-grown ZnO. The current of Al_2O_3/ZnO channel increases with increasing thickness and annealing process of ZnO underlayer, which is consistent with the Hall result of sheet carrier density. The improved crystallinity of ZnO underlayers facilitates the formation of 2DEG. Figure S8 shows the hysteresis characteristic in the transfer curve of a 2DEG back-gate device, indicating a slight positive V_{th} shift of 1 V by electron trapping from 2DEG channel to gate dielectric layers.

From the transfer characteristics shown in Figure S9, improved transfer curves are observed upon engineered top-gate FET structure with optimized thickness control and annealing process of ZnO underlayer. The threshold voltage (V_{th}) and switching speed of FETs are significantly increased by decreasing ZnO thickness to 7.5 nm. On/off ratio (I_{on}/I_{off}) over 10^8 is obtained for 7.5 nm ZnO with annealing due to high n_s and more 2DEG-like carriers. The I_G values of all top-gate FETs are below ~10^{-11} A, as shown in Figure S10. An increase of I_G at high negative V_G for 15 nm ZnO-based FETs is caused by low channel resistance and high electric field on the gate dielectric.

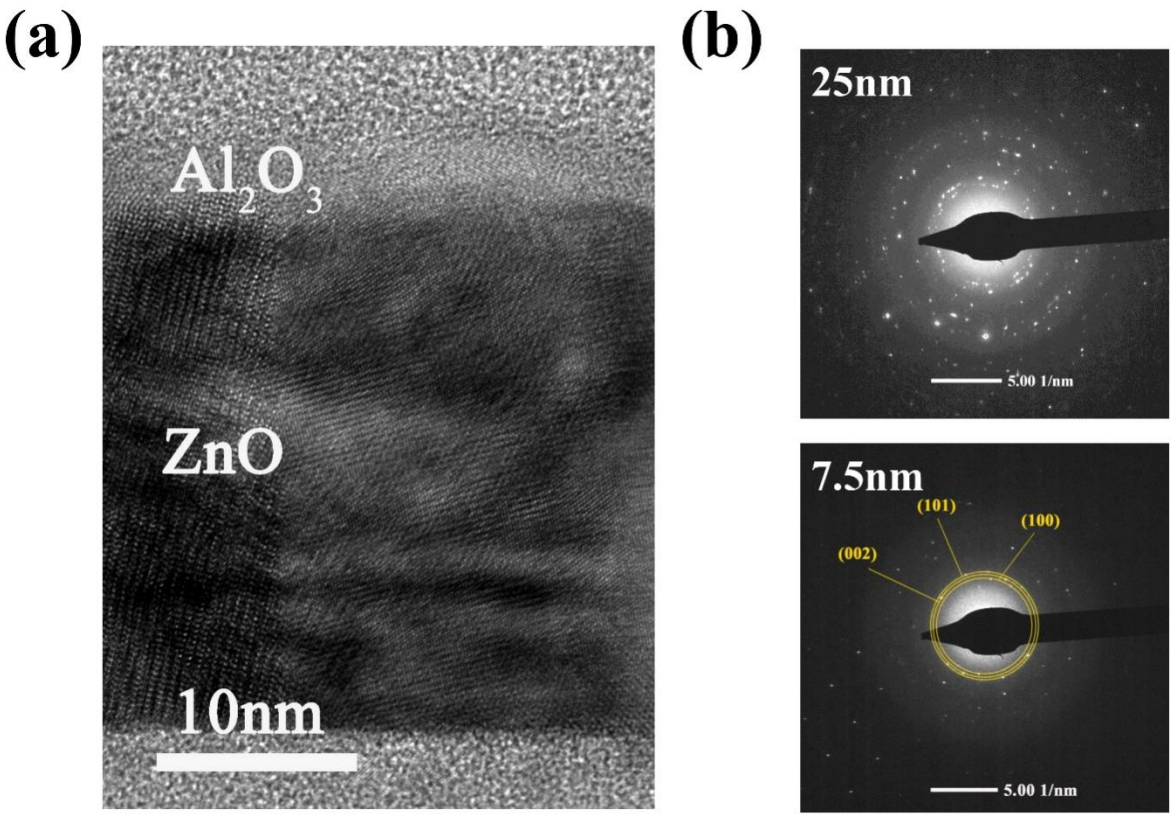

Figure S1. (a) TEM image of Al_2O_3/ZnO heterostructure with 25 nm annealed ZnO. (b) Diffraction patterns of annealed ZnO underlayer with 25 nm and 7.5 nm thickness, respectively, in Al_2O_3/ZnO heterostructures.

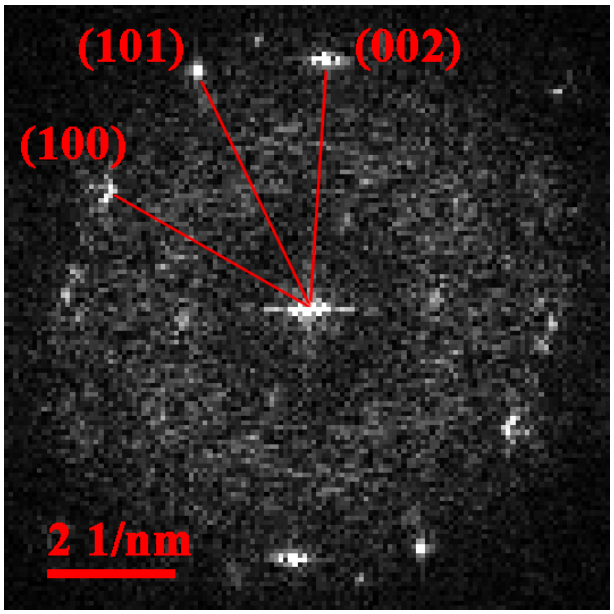

Figure S2. FFT image of the ZnO region in TEM image for Al_2O_3/7.5 nm annealed ZnO.

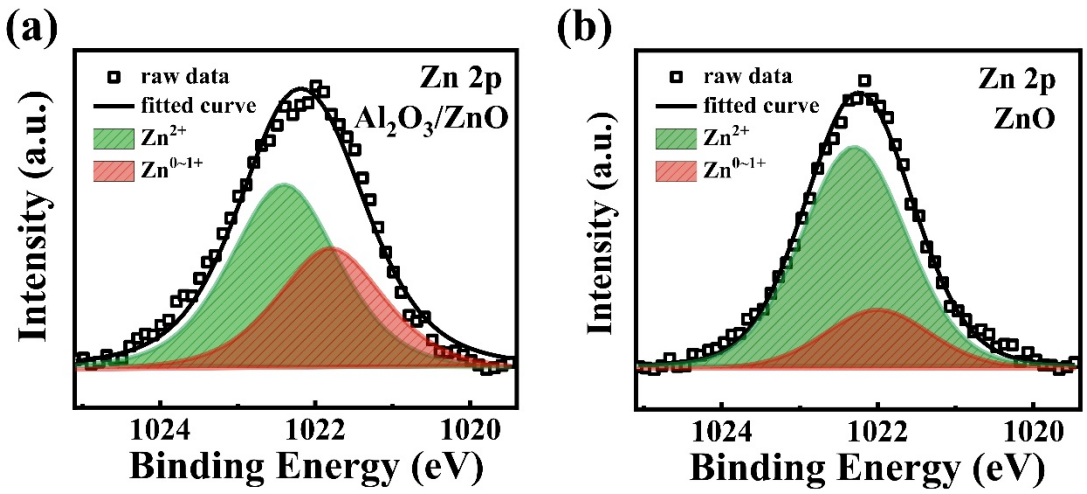

Figure S3. XPS analysis in normalized Zn 2p spectra of 7.5 nm annealed ZnO (a) with and (b) without Al_2O_3 overlayer, respectively.

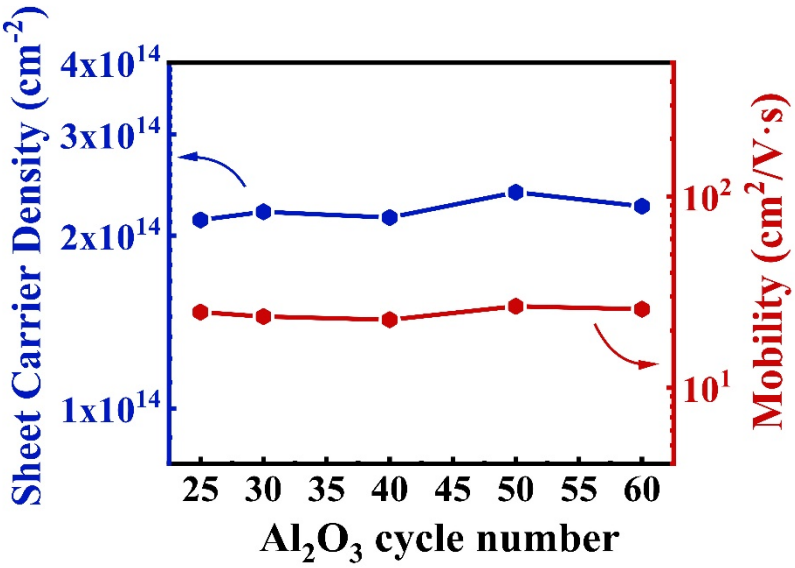

Figure S4. Sheet carrier density and Hall mobility of Al_2O_3/ZnO with 25 nm annealed ZnO as a function of Al_2O_3 cycle number obtained from Hall measurement.

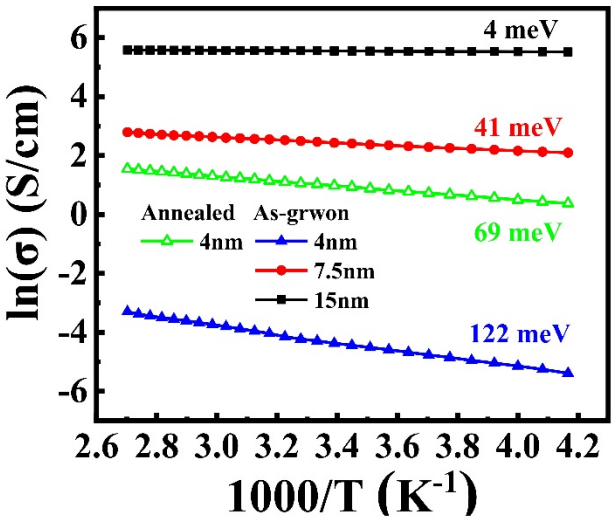

Figure S5. Temperature dependence of conductivity of various Al_2O_3/ZnO heterostructures.

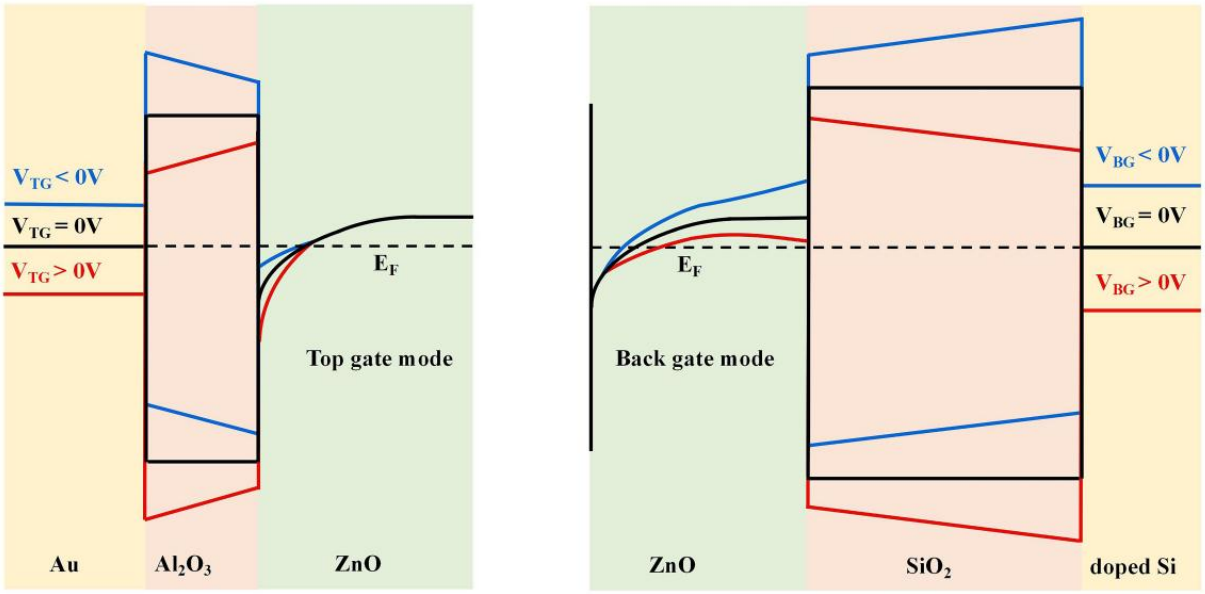

Figure S6. Energy band diagram of Al_2O_3/ZnO-based FET for top gate (left) and back gate (right) modes, respectively.

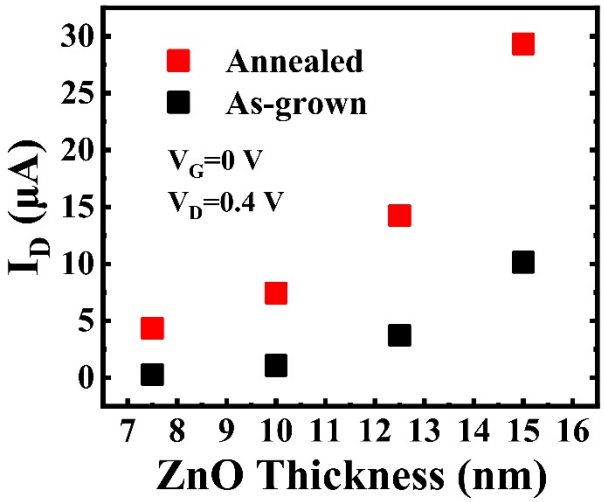

Figure S7. Drain current (I_D) of the back-gate FETs with annealed and as-grown ZnO, respectively, as a function of ZnO thickness. The length/width of the channel (L_C/W_C) is 20 μm/10 μm and I_D is measured at V_G of 0 V and V_D of 0.4 V.

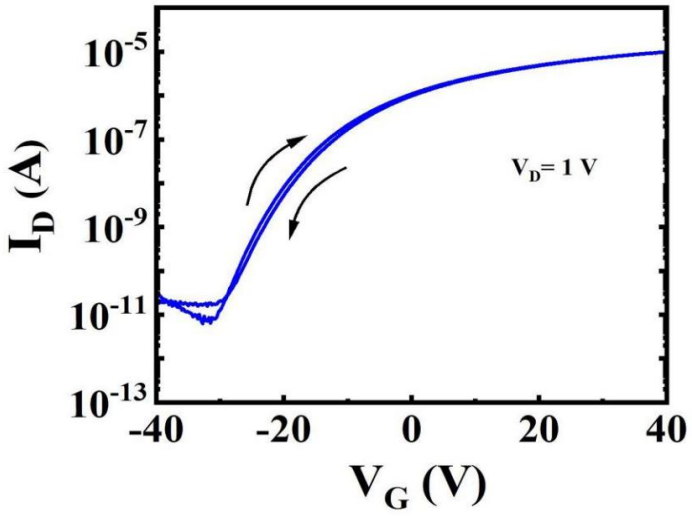

Figure S8. Hysteresis characteristic in the transfer curve of a 2DEG back-gate device with 7.5 nm annealed ZnO. The V_{BG} was continuously varied from -40 V to 40 V, then back to -40 V. The L_C/W_C is 20 μm/10 μm and V_D is 1 V.

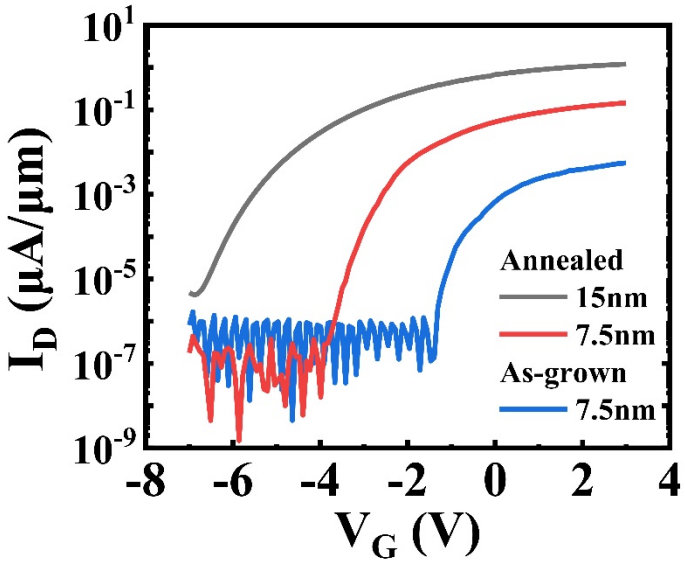

Figure S9. Transfer curves of top-gate Al_2O_3/ZnO-based 2DEG FETs with various ZnO underlayers. The L_C/W_C is 20 μm/10 μm and V_D is 0.5 V.

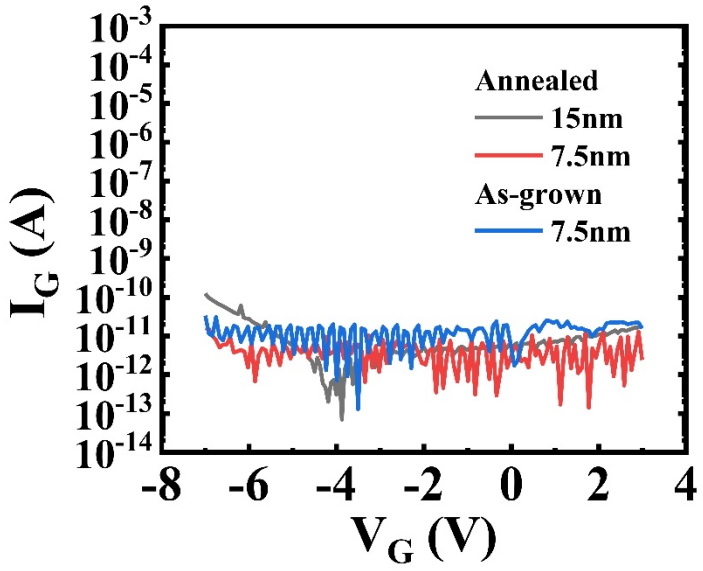

Figure S10. Gate leakage current (I_G) of top-gate Al_2O_3/ZnO-based 2DEG FETs as a function of gate voltage. The L_C/W_C is 20 μm/10 μm and V_D is 0.5 V.