Supplementary Materials

Controllable Modulation of Oxygen Vacancies Induced Adjustment of Memristive Behavior for Direct Differential Operation with Transistor-free Memristor

Qin Xie^a, Xinqiang Pan^{a,b,*}, Wenbo Luo^{a,b}, Yao Shuai^{a,b}, Huizhong Zeng^a, Jiejun Wang^a, Yuting Liu^a, Xudong Yang^a, Lu Lv^a, Jiaqi Xu^a, Hao Yan^b, Chuangui Wu^{a,b}, Wanli Zhang^{a,b}

^a State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 611731, P. R. China

^b Chongqing Institute of Microelectronics Industry Technology, UESTC, Chongqing 401332, P. R. China

*E-mail: panxinqiang@uestc.edu.cn

Supplementary Figures:



Fig. S1 (a)-(f) A flowchart of the fabrication process of the OVs-LN-OVs memristor. (g)-(k) A flowchart of the fabrication process of the OVs-LN memristor.



Fig. S2 The cross-section SEM image of memristors.



Fig. S3 Electroforming process of (a) OVs-LN-OVs memristor with the sequence of sweeping voltage of $0 \lor V \rightarrow + \lor_{max} \rightarrow 0 \lor V \rightarrow - \lor_{max} \rightarrow 0 \lor$. Electroforming process of (b) OVs-LN memristor with the sequence of sweeping voltage of $0 \lor V \rightarrow - \lor_{max} \rightarrow 0 \lor V \rightarrow + \lor_{max} \rightarrow 0 \lor$. The sequence of sweeping voltage is opposite to the sweeping sequence of curves in manuscript (Fig. 1). The cycle-to-cycle test of (c) OVs-LN-OVs memristor and (d) OVs-LN memristor. Reproducibility of HRS and LRS of the two memristors during 200 cycles were inserted.



Fig. S4 XPS of O1s on the surface of the (a) pristine single crystalline LN thin film, (b) single crystalline LN thin film irradiated by Ar^+ at 80 eV for 60 min.



Fig. S5 The schematic diagram of the sequence of voltage pulses used to test synaptic plasticity in (a) OVs-LN-OVs memristor and (b) OVs-LN memristor.



Fig. S6 Cycle-to-cycle test of plasticity of (a) OVs-LN-OVs memristor and (b) OVs-LN memristor. During each cycle, the voltage pulse sequence consists of 20 set voltage pulses and 5 reset voltage pulses, and pulse width is 0.1 s. The corresponding multi-RS of (c) OVs-LN-OVs memristor and (d) OVs-LN memristor at each cycle during the cycle-to-cycle test.



Fig. S7 Resistance retention properties of (a) OVs-LN-OVs memristor, (b) OVs-LN memristor.



Fig. S8 The current flowing through two memristors ($^{I}_{OVS-LN}$ and $^{I}_{OVS-LN-OVS}$) during the differential operation to denote (a) *W1*, (b) *W2*, (c) *W3*, (d) *W4*, (e) *W5* and (f) *W6*. In each differential operation, $^{I}_{OVS-LN}$ and $^{I}_{OVS-LN-OVS}$ were measured for three times. In each measurement, $^{I}_{OVS-LN}$ and $^{I}_{OVS-LN-OVS}$ were read for 100 times. The data in the lilac part represents $^{I}_{OVS-LN}$, and the data in the orange part represents $^{I}_{OVS-LN-OVS}$.