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Supplementary Information

Interface Roughness Effects and Relaxation Dynamics of an Amorphous Semiconductor Oxide-based Analog Resistance Switching Memory

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The variation of Schottky barrier height with temperature

The variation of Schottky barrier height with voltages at different temperatures is presented in Fig. 5(f). The barrier height is found to be decreased with increase in the applied bias voltage value for each temperature. Owing to this, the device could settle in a LRS state with the application bias in a gradual way. However, for a particular value of voltage, a linear increase in the barrier height is observed with temperature. Following from the eqn. 1, of the manuscript, ln (I/V) =Φ_B (q/kT), for a particular value of the applied bias voltage V, $\Phi_B \propto$ T (since, ln(constant)= 0) . As the temperature increases, the number of thermally generated carriers increases causing an increment in the reverse current which leads to the increase in the barrier height.