Supporting Information

Tunable Non-volatile Memory Based on 2D InSe/*h*-BN/GaSe heterostructure towards potential multifunctionality

Xiang Gong [†], *Yueying Zhou* [†], *Jiangnan Xia* [†], *Li Zhang* [†], *LiJie Zhang* [†], *Long-Jing Yin* [†], *Yuanyuan Hu* [‡, §, *], *Zhihui Qin* [†, *], *and Yuan Tian* [†, §, *]

[†] Key Laboratory for Micro/Nano Optoelectronic Devices of Ministry of Education & Hunan Provincial Key Laboratory of Low-Dimensional Structural Physics and Devices, School of Physics and Electronics, Hunan University, Changsha 410082, P.R. China

[‡] College of Semiconductors (College of Integrated Circuits), Hunan University, Changsha 410082, China.

[§] International Science and Technology Innovation Cooperation Base for Advanced Display Technologies of Hunan Province

*E-mail: ytian@hnu.edu.cn; zhqin@hnu.edu.cn; yhu@hnu.edu.cn

The supporting information includes Figures S1-S9 and Table S1.

S1: The fabrication process schematics of the InSe/*h*-BN/GaSe FG-FET device

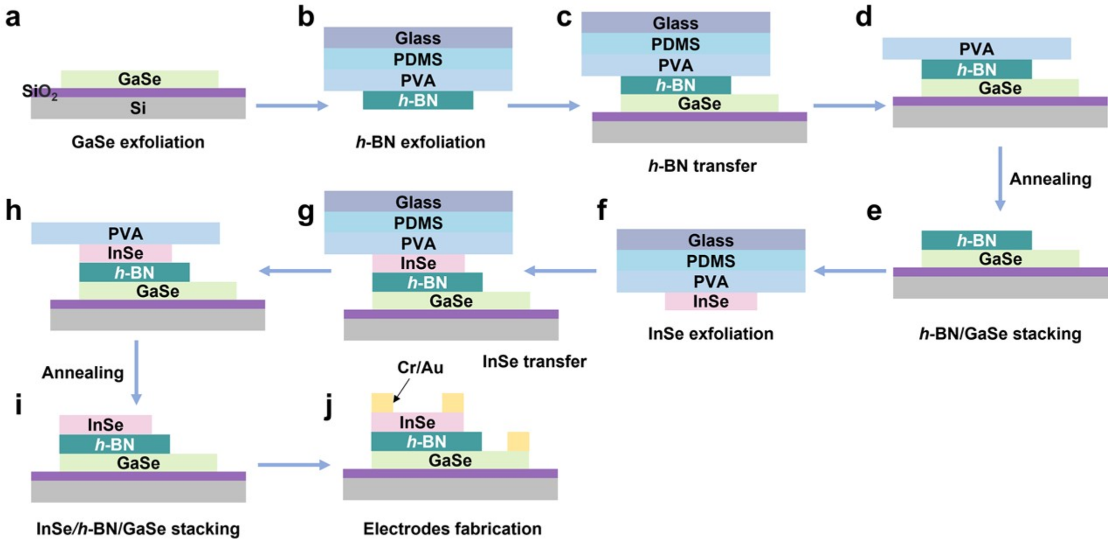


Figure S1. Schematic fabrication process of the 2D InSe/*h*-BN/GaSe heterostructure based floating-gate memory. (**a**) preparation of GaSe nanosheets on the SiO_2/Si substrate. (**b-i**) construction of InSe/*h*-BN/GaSe heterostructure, including exfoliation, transfer and stacking process of *h*-BN and InSe. (**j**) Electron beam evaporation was used to define Cr/Au electrodes on the obtained heterostructures.

S2: AFM images of the *h*-BN/GaSe, InSe/*h*-BN/GaSe heterostructures

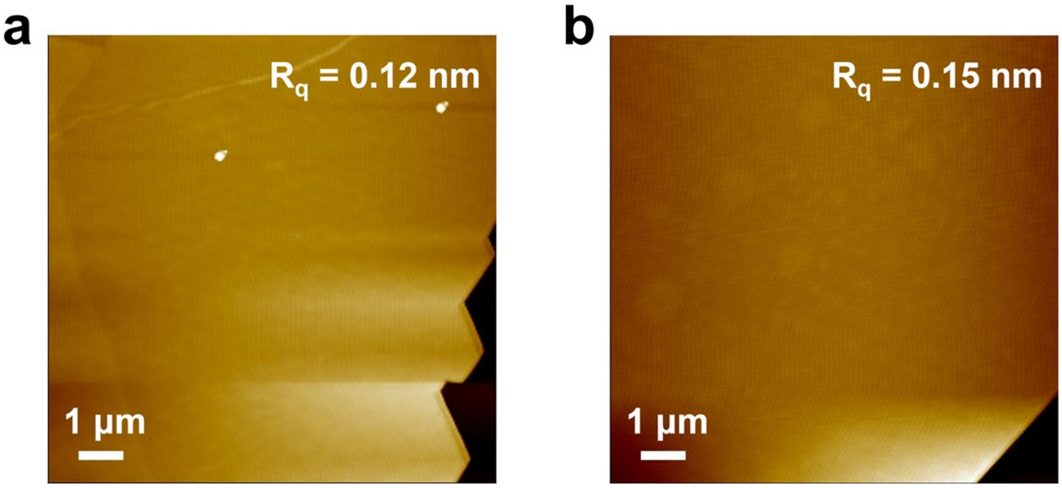


Figure S2. Surface morphology of *h*-BN/GaSe and InSe/*h*-BN/GaSe heterostructures. (**a**) The topography of the *h*-BN/GaSe heterostructure in the stacking process, with surface roughness R_q about 0.12 nm after annealing. (**b**) The topography of the InSe/*h*-BN/GaSe heterostructure in the stacking process, with surface roughness R_q about 0.15 nm after annealing.

S3: OP and AFM images of the InSe, *h*-BN, GaSe

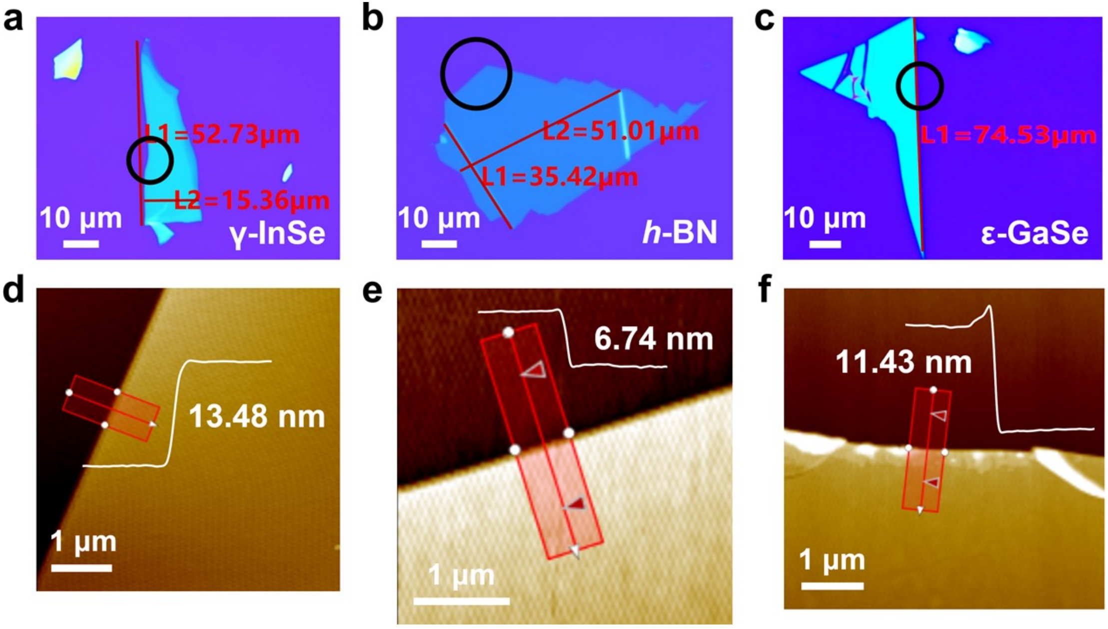


Figure S3. Morphology and thickness characterizations of the InSe, *h*-BN, GaSe nanosheets. (**a-c**) Optical images of InSe, *h*-BN, GaSe on Si/SiO_2 substrate. The typical size of each flake is around tens of micrometers. (**d-f**) AFM images of the InSe, *h*-BN, GaSe area within the corresponding circle in (**a-c**). Thickness line profiles of the InSe, *h*-BN and GaSe flakes measured at positions marked in red lines in (**d-f**), respectively. The results show that the thicknesses of InSe, *h*-BN and GaSe are about 13.48 nm, 6.74 nm and 11.43 nm, respectively.

S4: Optical microscope images of the devices with different *h*-BN thickness and corresponding AFM characterizations

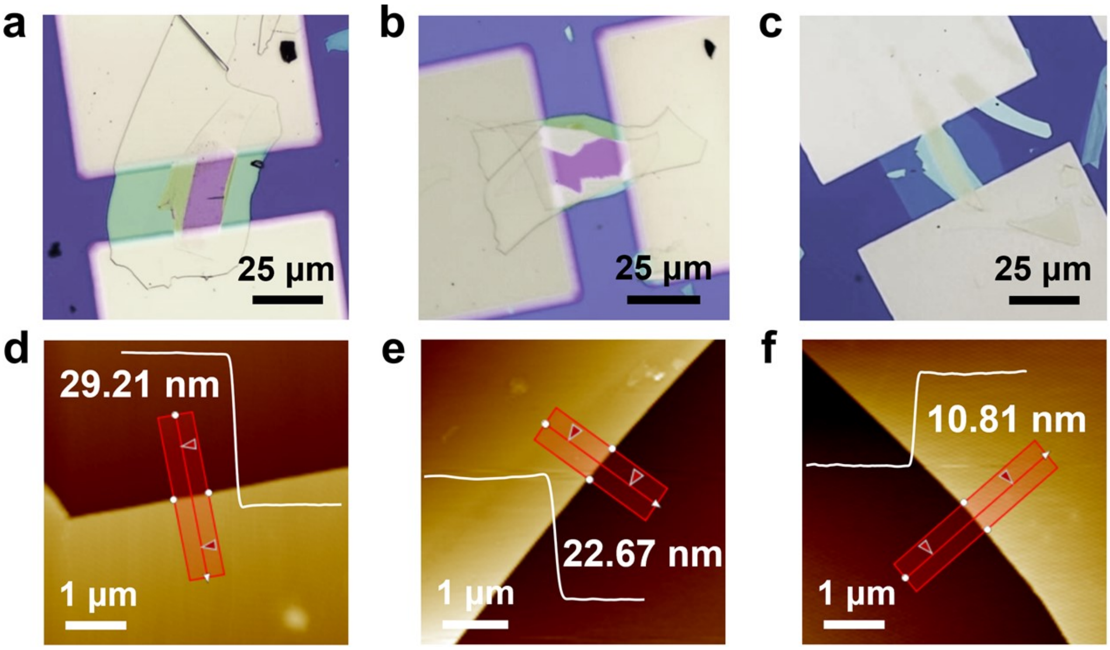


Figure S4. Thickness characterizations of different *h*-BN related devices. (**a-c**) False-colour optical images of the InSe/*h*-BN/GaSe heterostructure Device 1-3 respectively. (**d**) AFM characterization of *h*-BN in the Device 1 in Figure (**a**). The thickness of the *h*-BN flake measured at the position marked in red lines, showing that the thickness of *h*-BN is about 29 nm. (**e**) AFM characterization of *h*-BN in the Device 2 in figure (**b**). The thickness of the *h*-BN flake measured at the position marked in red line, showing that the thickness of *h*-BN is about 23 nm. (**f**) AFM characterization of *h*-BN in the Device 3 in figure (**c**). The thickness of the *h*-BN flake measured at the position marked in red line, showing that the thickness of *h*-BN is about 11 nm.

S5: More details about the Device 2

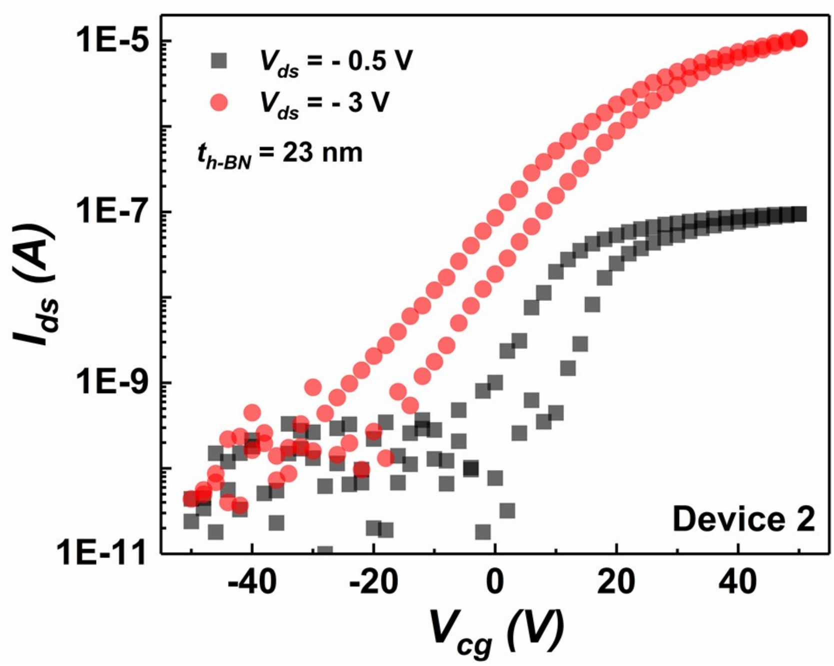


Figure S5. Memory characteristics of InSe/*h*-BN/GaSe FG-FET Device 2.

S6: More details about the Control Device 3

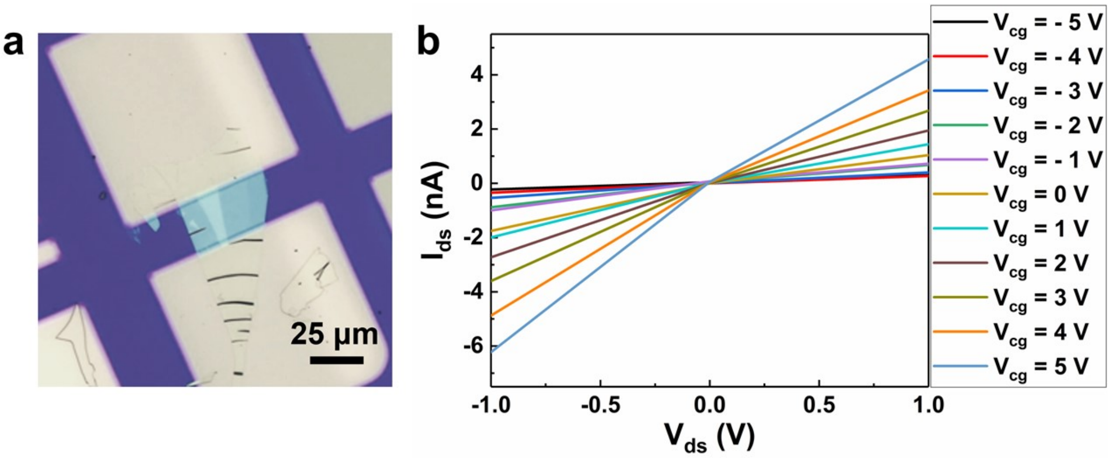


Figure S6. Transfer curves of InSe related devices under Control Device 3 configuration. (**a**) False-colour optical image of the Control Device 3. (**b**) Output characteristics (drain-source current I_{ds} vs. drain-source voltage V_{ds}) of the floating gate transistor in the ON state, for control gate bias V_{cg} from -5 V to 5V. The curves show almost linear at small V_{ds}, indicating good ohmic contacts.

S7: Photoluminescence (PL) characterizations of few layers InSe, GaSe

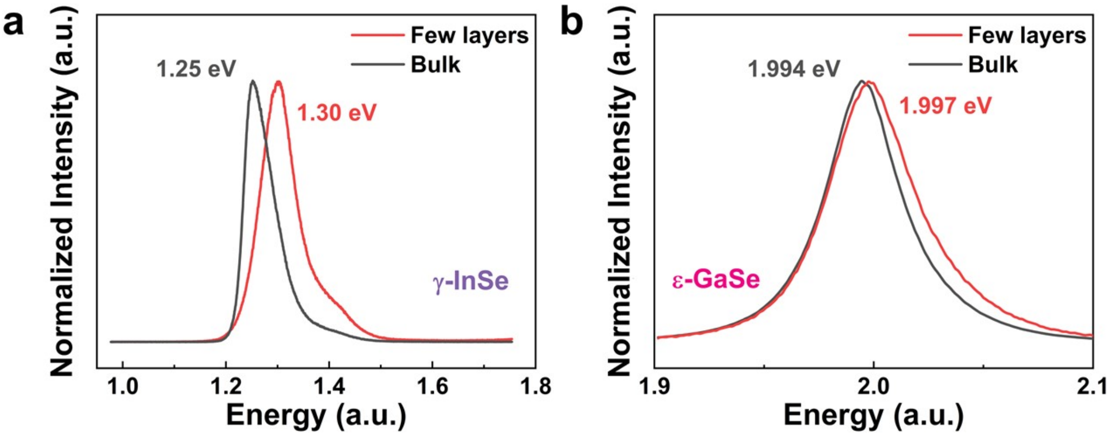


Figure S7. PL spectra of the InSe (a) and GaSe (b) flakes comparing with bulk. Corresponding band gap values are use in Figure 4.

S8: Extinction Ratio of the Device 4

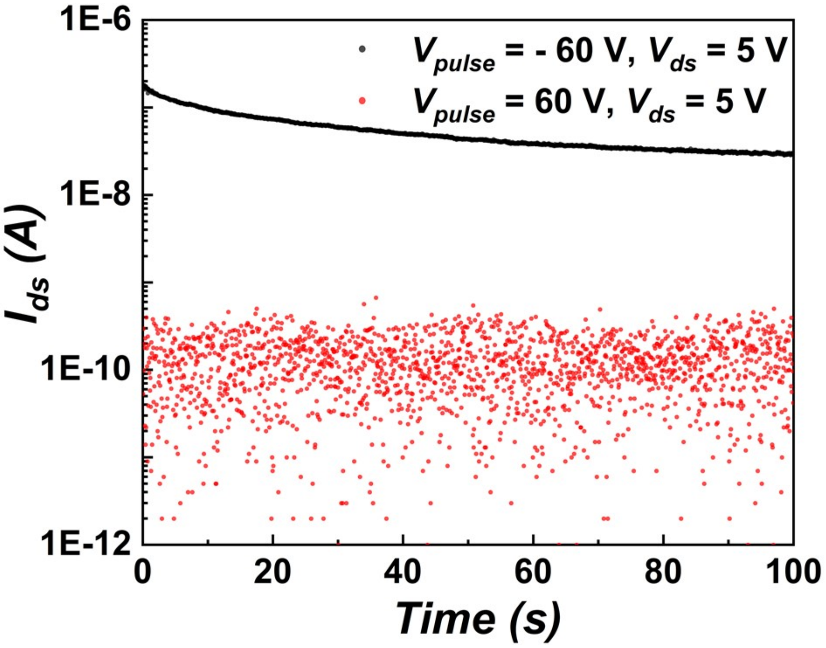
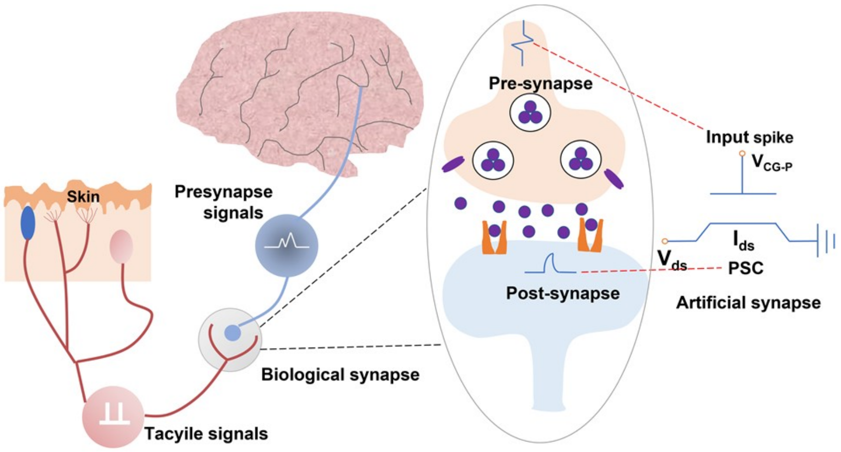


Figure S8. More details in erasing non-volatile of InSe/*h*-BN/GaSe FG-FET Device 4. Temporal evolution of drain-source currents (I_{ds}) in the erase (ON) and program (OFF) states. The curves are acquired independently for the erase (10^{-7}-10^{-6} A) and program (10^{-11}-10^{-10} A) current states and plotted on a common time scale. The drain-source bias voltage is 5 V, with the V_{cg} = ± 60 V and the duration of the control-gate voltage (V_{cg}) pulse is 2 s. The resulted extinction ratio is close to 10^3.

S9: Simulation of synaptic features in the Device 3



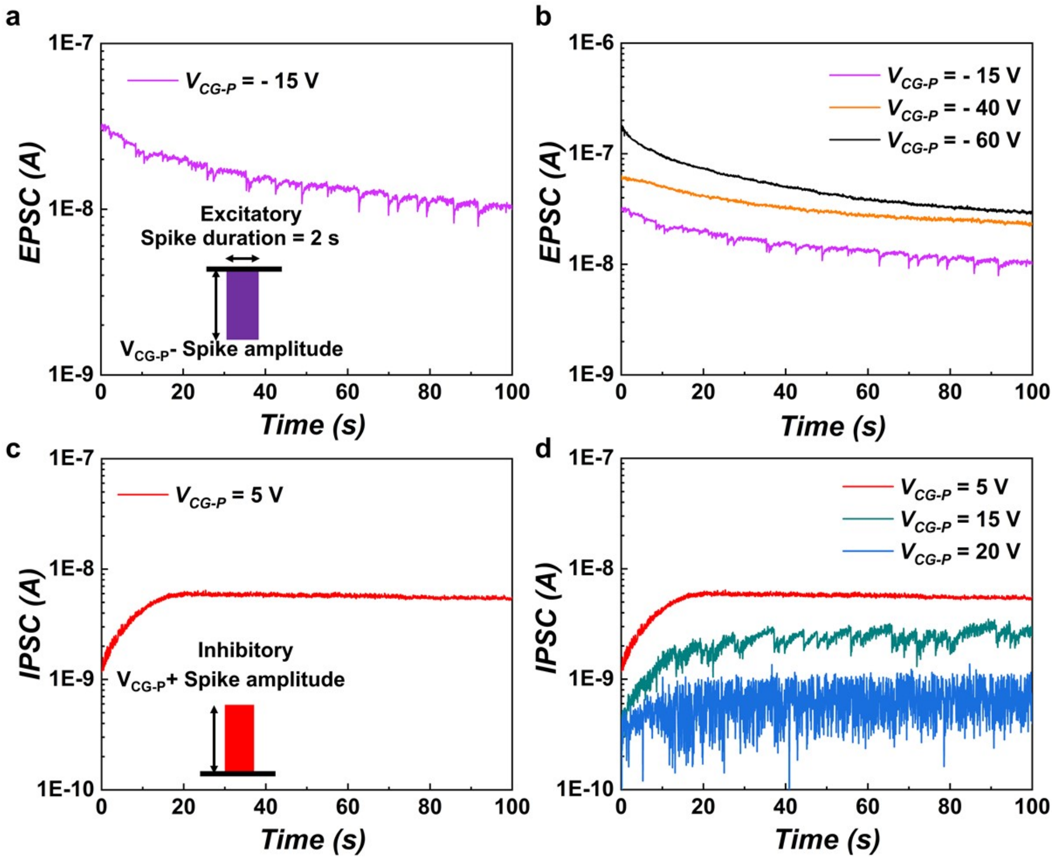


Figure S9. **Simulation of synaptic features based on the floating gate FET Device 3.** (**a**) The generation of excitatory postsynaptic current (EPSC) when a pulse voltage of -15 V is applied to the device. (**b**) The generation of EPSC when negative pulse voltages of different magnitude are applied to the device. (**c**) Inhibitory postsynaptic current (IPSC) generation when a pulse voltage of + 5 V is applied to the device. (**d**) The generation of IPSC when forward pulse voltages of different amplitudes are applied to the device.

Table S1. Details of Devices 1-4 and Control Devices 1-3.

Configurations	t_{InSe} (nm)	$t_{h\text{-}BN}$ (nm)	t_{GaSe} (nm)	Floating gate
Device 1	11	29	13	floating
Device 2	14	23	15	floating
Device 3	14	11	12	floating
Device 4	13	7	11	floating
Control Device 1	13	7	11	grounded
Control Device 2	15	8	-	-
Control Device 3	10	-	13	floating

Table S2. Overall performance of Devices 4.

Configurations	ON/OFF	ΔV (V)	V_{ds} (V)	V_{cg} (V)
Device 4	10^4	72	5	± 60
	10^3	75	-5	± 60
	10^3	58	-5	± 50
	10^3	50	-1	± 60
	10^3	50	1	± 60