Supporting information

for

Photogating interfacial effects in carbon nanotube-based transistors on Si/SiO_2 substrate toward highly sensitive photodetection

Svetlana I. Serebrennikova, Daria S. Kopylova, Yuriy G. Gladush, Dmitry V. Krasnikov, Sakellaris Mailis, Albert G. Nasibulin

Skolkovo Institute of Science and Technology, Nobel 3, 121205, Moscow, Russia

S1. CV-measurement of silicon substrates

The existence of surface potential at the silicon/dielectric interface, which is necessary for photogating, can be caused by the bulk or surface oxide charges density Q_{ox} [1-6]. The properties of the photogating-based FETs depend directly on the silicon's characteristics because the photogating process happens in the substrate. One of the ways to find the substrate's characteristics, such as the type of doping, approximate level of doping N and value of surface potential φ_s, is to measure the capacitance-voltage (CV) characteristic of the substrate. It can be done by applying a high-frequency signal on a metal gate contact sputtered on the oxide layer and measuring a displacement current I_{displ}, which is proportional to the capacitance of this metal–oxide–semiconductor (MOS) structure and to the time derivative of the voltage applied on the substrate [7, 8]:

$$I_{displ} = C\frac{dV_c}{dt}. \quad \text{(S1)}$$

The capacitance of the silicon/dielectric structure is determined by the following formula [3-6]:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \rightarrow C = \frac{C_{ox}C_s}{C_{ox} + C_s}, \quad \text{(S2)}$$

where C_{ox} is an oxide capacitance, i.e. a constant term, $C_s = \frac{\varepsilon_S \varepsilon_0 A}{w}$ is a silicon capacitance, i.e. a variable term, where A is an area of the substrate, ε_0 is a vacuum permittivity, and ε_S = 11.7 is a

silicon permittivity. C_s also depends on the thickness of the depletion layer w, which is set by the applied gate voltage [3-6].

The relation between the maximum of the capacitance, which is oxide capacitance C_{ox}, and the minimum of the capacitance C_{min} on the CV curve can help to estimate the density of doping N [3, 6]:

$$N = \frac{4\varphi_F \quad C_{min}^2}{e\varepsilon_S\varepsilon_0 A^2(1 - C_{min}/C_{ox})^2}, \tag{S3}$$

where e is the elementary charge and φ_F is Fermi energy.

For silicon substrate at room temperature, it can be rewritten more simply [3, 6]:

$$\log_{10}(N) = 30.38759 + 1.68278\log_{10}(C_1) - 0.03177\left(\log_{10}(C_1)\right)^2, \tag{S4}$$

where $C_1 = \frac{C_{min}}{A(1 - C_{min}/C_{ox})}$.

To find the surface potential φ_s (or the value of the initial band bending at the silicon/dielectric interface, Figure 1a), a value of applied voltage necessary to restore the flat-band condition (so-called flat-band potential V_{FB}) has to be found. It is determined from the CV characteristic at the value of flat-band capacitance C_{FB}, which can be calculated for Si/SiO_2 substrate at temperature T by the following formula [3, 6]:

$$\frac{C_{FB}}{C_{ox}} = \left(1 + \frac{136\sqrt{T/300}}{d_{ox}\sqrt{N}}\right)^{-1}, \tag{S5}$$

where d_{ox} is an oxide thickness.

The surface density of oxide surface charges Q_{ox} can be found from the flat-band potential and the difference between work functions φ_{ms} of semiconductor and metal contact [1- 5]:

$$V_{FB} = \varphi_{ms} - \frac{Q_{ox}}{C_{ox}}. \tag{S6}$$

The presence of oxide surface charges induces a surface charge in silicon $Q_s = -Q_{ox}$ which entails the band bending and appearance of surface potential φ_s in silicon. The surface charge and surface potential are connected in the following way [1-5]:

$$Q_s = -\sqrt{2k_BT\varepsilon_S\varepsilon_0 n_i} * F(\varphi_s), \tag{S7}$$

$$F(\varphi_s, \Delta n) = \left(\frac{N}{n_i}\left(e^{-u_s} + u_s - 1\right) + \frac{n_i}{N}\left(e^{u_s} - u_s - 1\right) + \frac{N}{n_i}\left(e^{-u_s} + e^{u_s} - 2\right)\frac{\Delta n}{N}\right)^{\frac{1}{2}}, \tag{S8}$$

where $F(\varphi_s, \Delta n)$ is a normalised interfacial electric field, $u_s = \frac{e\varphi_s}{k_B T}$ is a normalised surface potential, $n_i \approx 10^{10}$ cm^{-3} is the number of intrinsic carriers at room temperature for silicon, and Δn is the number of photoexcited (or excess) carriers in silicon.

To obtain the characteristics of the silicon substrate, we conducted the *CV* measurement (Figure S1a) [7, 8]. We applied the triangle signal with a peak-to-peak amplitude of 20 V and frequency of 200 kHz using waveform generator Keysight 33500B Series to the deposited on the SiO_2 gold contact with a square of $A \approx 25$ mm^2. We measured the voltage on the MOS capacitor with the digital oscilloscope Tektronix MDO3102 (bandwidth 1 GHz) and found the displacement current by measuring the voltage drop on the resistor also with the oscilloscope. Then, we calculated the capacitance as a ratio of displacement current to the time derivative of the applied voltage (formula S1).

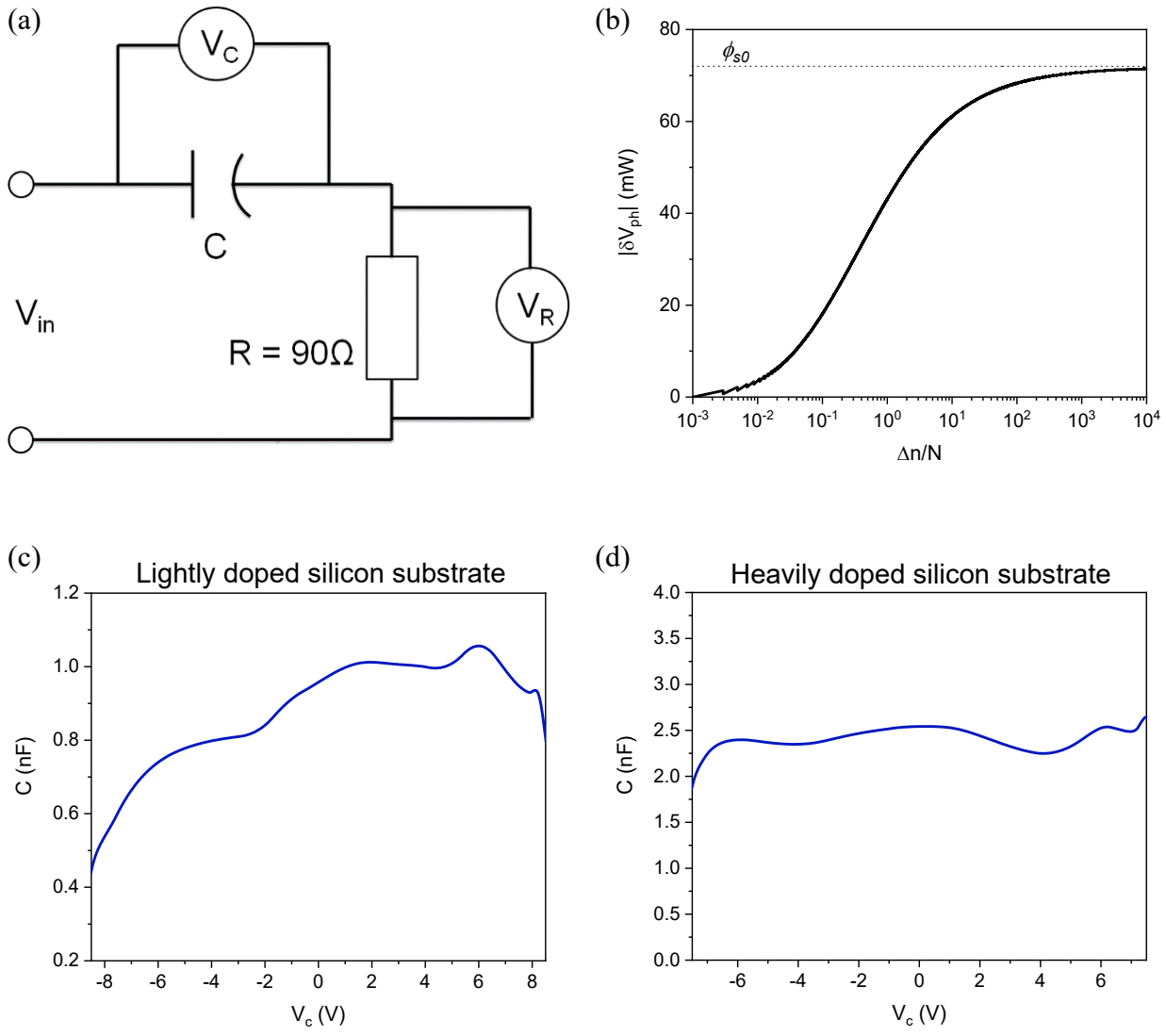

Figure S1. (a) Circuit for *CV*-measurement; (b) Absolute value of photogate voltage δV_{ph} calculated as a function of the ratio of the number of photoexcited carriers to the doping density (c) *CV* curve for lightly doped silicon; (d) *CV* curve for heavily doped silicon.

Figure S1c shows the result of the *CV* measurement of the substrate where the photogating is observed. From this *CV* curve, we found the oxide capacitance C_{ox} of ~ 1 nF and its thickness $d_{ox} \approx 800$ nm, silicon has n-type of doping, and the doping density estimated from the formula S4 is $N \sim 10^{15}$ cm^{-3}. After calculating flat-band capacitance C_{FB} by formula S5, finding the flat-band voltage $V_{FB} = -0.5$ V and paying attention to the difference in work functions of gold and silicon $\varphi_{ms} \approx 0.5$ V, we found the oxide surface charges density by formula S6 $Q_{ox} \approx 2.5 * 10^{10}$ cm^{-2}. This value allowed us to estimate the surface potential as $\varphi_{s0} \approx 72$ mV by the formula S7 considering dark conditions ($\Delta n = 0$). Figure S1b shows an absolute value of the photogate voltage $|\delta V_{ph}| = |\varphi_s - \varphi_{s0}|$ as a function of the ratio of the photoexcited carrier number to the doping density calculated from Formulas S7-S8. According to the graph, this value cannot exceed the value of the initial surface potential φ_{s0}.

For comparison, we also carried out a *CV* measurement of a heavily doped substrate (Figure S1d), on which we did not observe the photoresponse. The curve is flat, like for a conventional capacitor, so the type and level of doping of silicon cannot be found. We calculated the oxide capacitance of this substrate as $C_{ox} \sim 2.5$ nF and its thickness as $d_{ox} \approx 300$ nm.

S2. Electronic characteristics of phototransistors and their photoresponse

The gate capacitance per area C_g of transistors with a channel consisting of SWCNTs sparse network is estimated with the following formula proposed by Cao *et al.* [9]:

$$C_g = \frac{1}{\Lambda}\left(\frac{1}{2\pi\varepsilon_{ox}\varepsilon_0}\ln\left(\frac{\Lambda\sinh\left(2\pi d_{ox}/\Lambda\right)}{r\qquad\pi}\right)+\frac{1}{C_q}\right)^{-1}, \tag{S9}$$

Where $\varepsilon_{ox} = 4$ is SiO_2 permittivity, $d_{ox} = 800$ nm is oxide thickness calculated from *CV* measurement, $\Lambda \sim 1$ μm is the average distance between SWCNTs in the network determined from SEM imaging, $r \sim 1$ nm is the mean radius of SWCNTs, $C_q \sim 0.4$ nF/m is the quantum capacitance per nanotube length [10]. Cao *et al.* [9] showed this formula of such a gate capacitance model is accurate enough to fit experimental results. The calculated gate capacitance allows us to estimate the maximum mobility μ of carriers in studied FETs' channels as 10-100 cm^2/V·s with the formula [4, 5]:

$$\mu = \frac{L}{WC_g V_{SD}} g_m, \tag{S10}$$

where $g_m = \frac{\partial I}{\partial V_g}$ is transconductance, V_{SD} = 1 V is applied source-drain voltage.

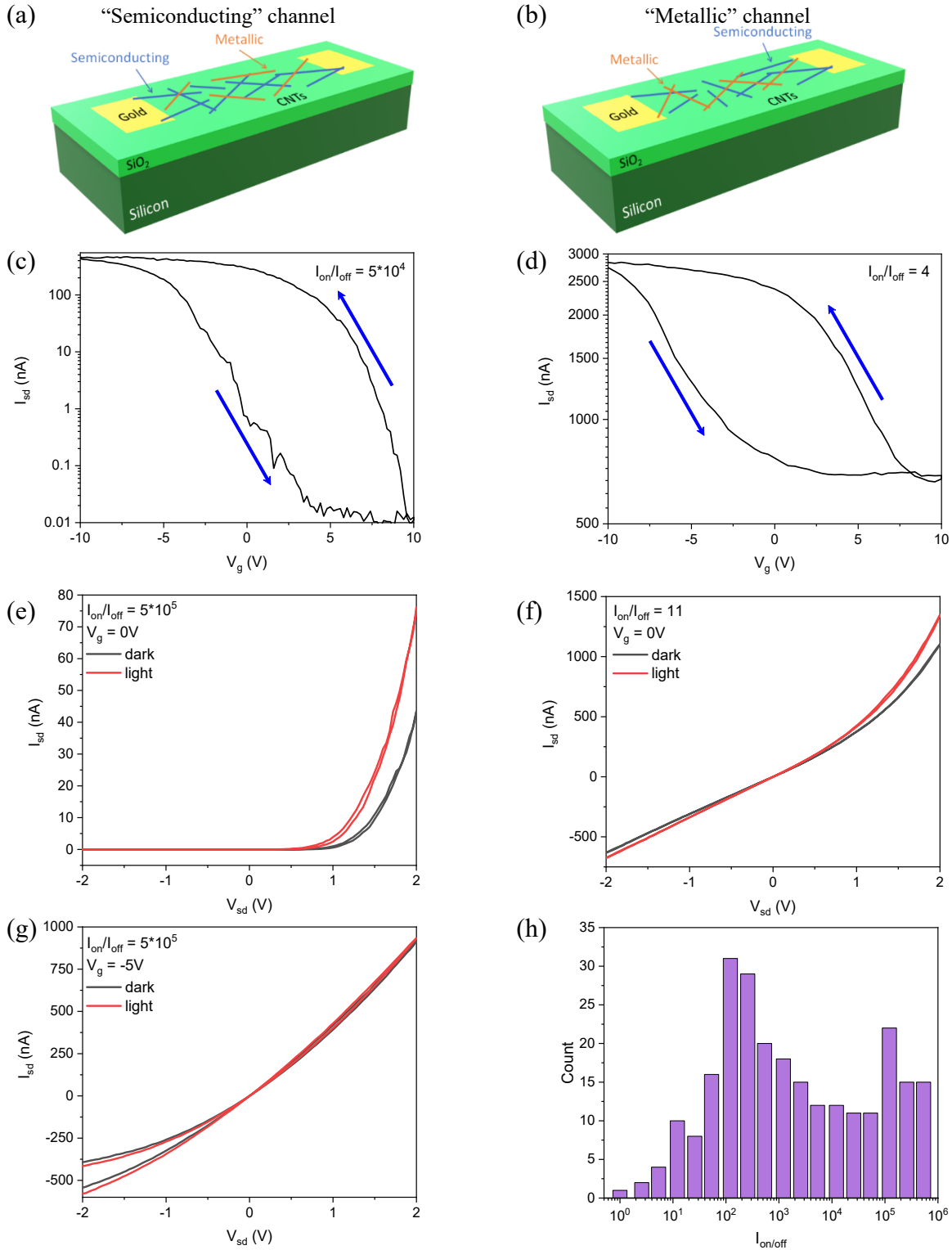

Figure S2. (a) Schematic of the “semiconducting” channel – current flows through semiconducting nanotubes (blue); (b) Schematic of the “metallic” channel – metallic nanotubes (red) close the contacts; (c) Transfer characteristic of “semiconducting” device; (b) Transfer characteristic of “metallic” device; (e) IV curves of ”semiconducting” devices at gate voltage V_g = 0 V; (f) IV curves of “metallic” devices at gate voltage V_g = 0; (g) IV curves of ”semiconducting” devices at the gate voltage V_g = -5 V (open channel); (h) Distribution of the phototransistors according their I_{on}/I_{off} ratio.

Table S1. Map of the devices on one chip (green – “metallic”, blue – “semiconducting”; in cells – I_{on}/I_{off} ratio).

line\column	1	2	3	4	5	6
1	-	-	-	-	820	5000
2	2200	1800	205	2000	2100	950
3	200000	2800	370	1190	1070	-
4	600000	4000	61000	770	200	1000
5	180	45000	630	2100	260	170
6	6700	180000	44000	310	57	72
7	1600	495	61000	320	120	850
8	30	188	87000	60	110	90
9	15	71	8700	-	160	-
10	61	83	63	31000	260	120
11	46	52	-	160	-	-
12	150	300	150	140	7600	85000
13	-	1300	100	150	530	-
14	-	500	970	-	-	-

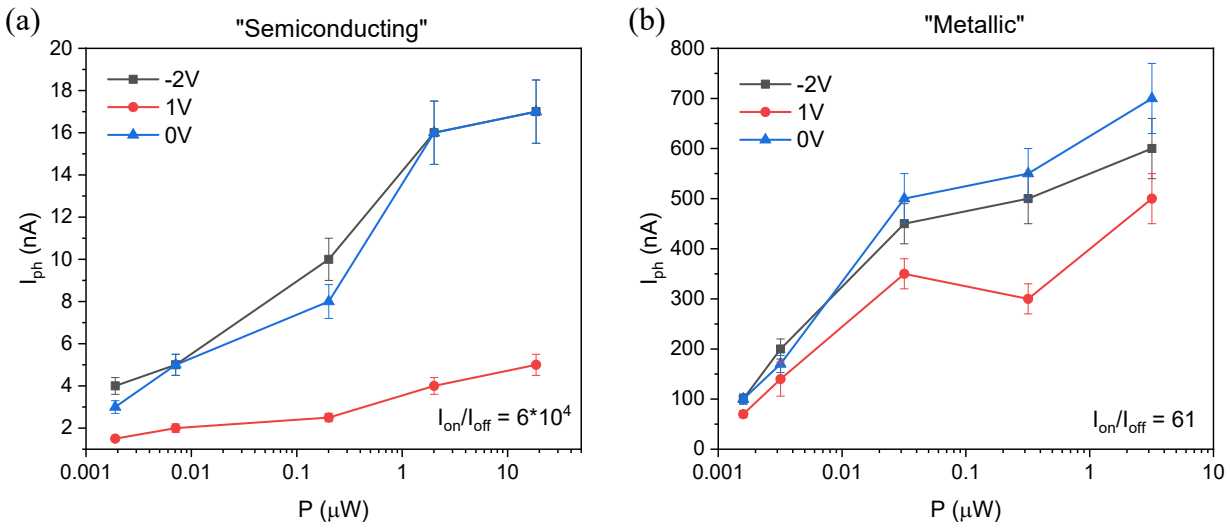

Figure S3. (c) Photocurrent of “semiconducting” device as a function of incident light power at different gate voltages; (d) Photocurrent of “metallic” device as a function of incident light power at different gate voltages.

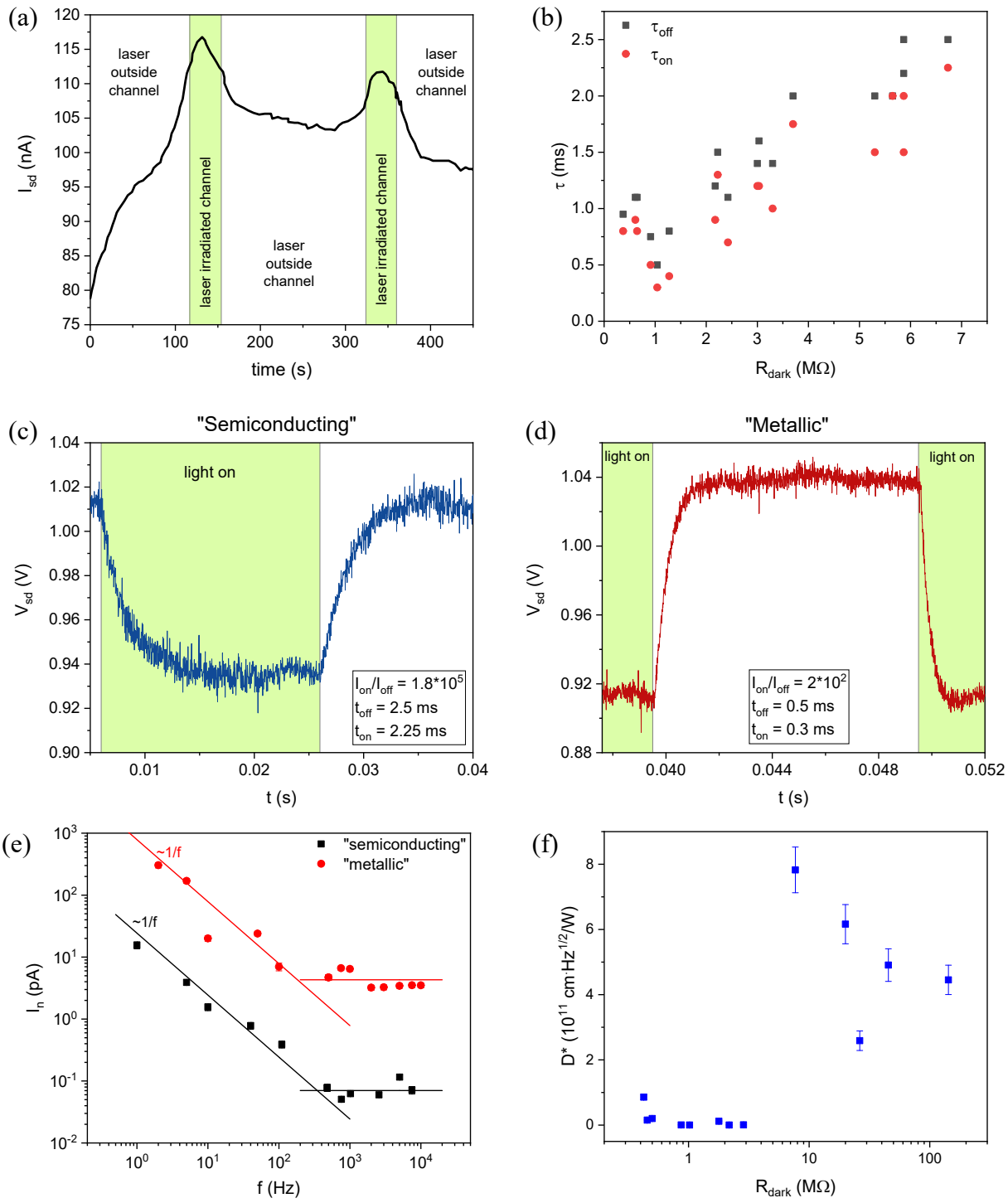

Figure S4. (a) Current through the channel while scanning the device with narrow laser beam with λ = 532 nm and P = 617 μW (beam spot << device area); (b) τ_{on} and τ_{off} of devices as a function of their dark resistances; (c) Voltage responses as a function of time of "metallic" device on the silicon substrate (applied I_{SD} = 1 μA); (d) Voltage responses as a function of time of "semiconducting" device on the silicon substrate (applied I_{SD} = 150 nA); (d) Noise current of the transistors as a function of frequency. Lines are guides for the eye; (e) Specific detectivity of transistors as a function of the channel's dark resistance.

S3. Fabrication of devices

We used UV lithography to pattern the contacts of phototransistors (μPG101 Heidelberg instruments Micro Pattern Generator). Firstly, we covered the substrate with SWCNTs network on it with resist Lor5b [11] in a spin-coater and dried it at 180°C for 10 minutes. Secondly, we applied the resist AZ1505 [12] to the sample and dried it at 100°C for 1 minute (Fig. S5a). The first resist (Lor5b) was used to create the undercut to facilitate further lift-off process [11]. After exposure to the lithographer, we developed resists in the AZ726 developer for 30 seconds (Fig. S5b). Then, we deposited the gold (60 nm) contacts with the chromium (5 nm) underlayer on the substrate by a thermal evaporation method (Tecuum AG vacuum evaporator) (Fig. S5c). After the lift-off process in DMSO (70°C for 10 minutes) (Fig. S5d), we made the second step of lithography (with only AZ1505 resist) (Fig. S5e) to pattern trenches around the devices (Fig. S5f) and isolated devices from each other by etching SWCNTs from trenches in oxygen plasma (Fig. S5g).

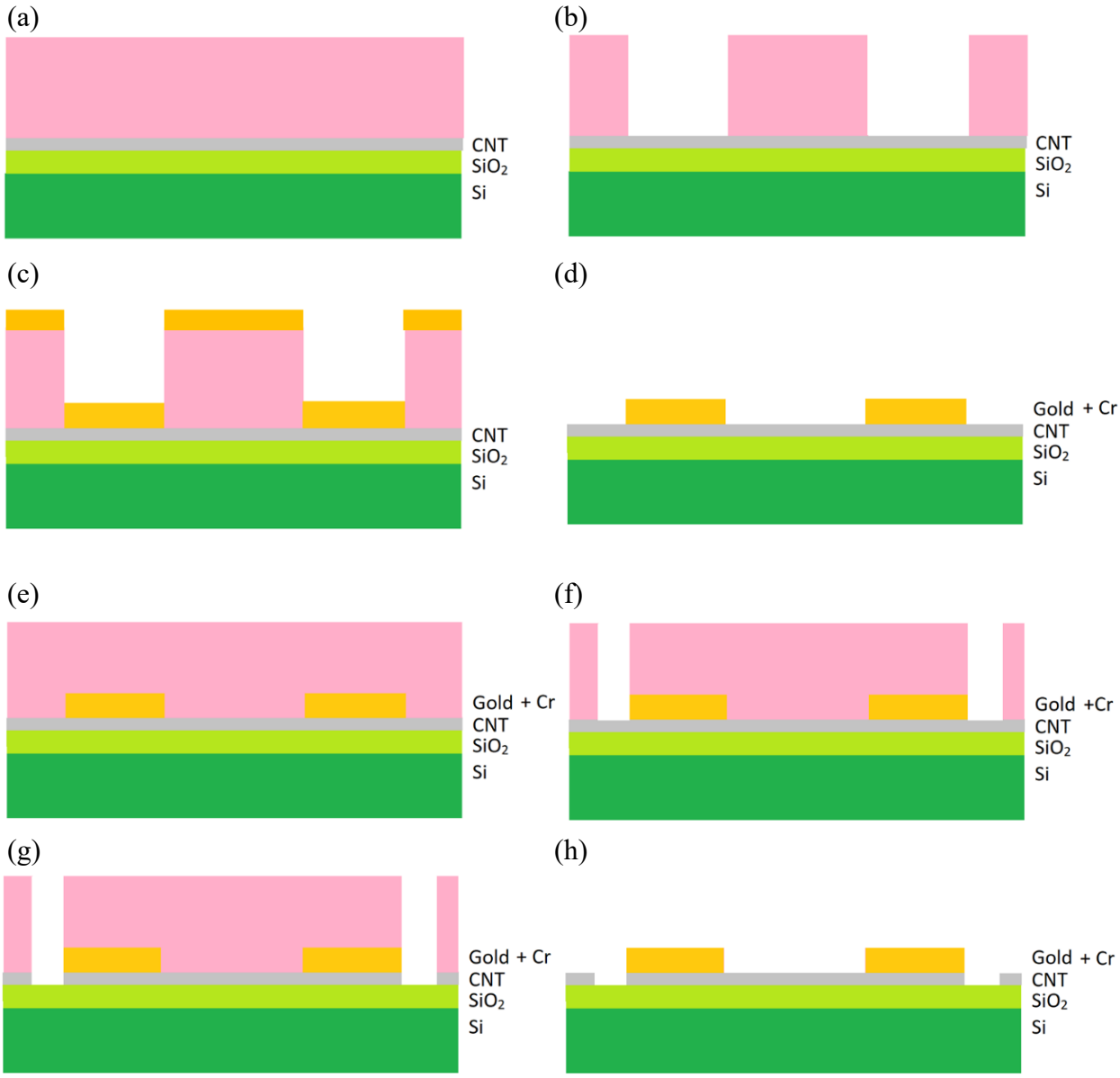

Figure S5: Steps of samples preparation of the devices: (a) covering with resists Lor5b and AZ1505; (b) UV lithography and development of contacts; (c) deposition of the gold; (d) lift-off; (e) covering with resist AZ1505; (f) UV lithography and development of trenches; (g) etching of SWCNTs with oxygen plasma; (h) washing away the rest of the resist.

References

[1] Kronik, L.; Shapira Y. Surface photovoltage phenomena: theory, experiment, and applications. *Surface Science Reports*. **1999**, *37*, 1–206.

[2] Schroder, D. K. Surface voltage and surface photovoltage: history, theory and applications REVIEW ARTICLE. *Meas. Sci. Technol*. **2001**, *12*, R16–R31.

[3] Schroder, D. K. *Semiconductor material and device characterization*; John Wiley Sons, Inc.: Hoboken, New Jersey, 2006.

[4] Sze, S. M. *Semiconductor Devices, physics and technology*; 2nd ed.; John Wiley Sons, Inc.: Hoboken, New Jersey, 2002.

[5] Sze, S. M.; Ng, K. K. *Physics of Semiconductor Device*; John Wiley Sons, Inc.: Hoboken, New Jersey, 2007.

[6] Deen, M. J.; Pascal, F. Electrical characterization of semiconductor materials and devices. In *Springer Handbook of Electronic and Photonic Materials*; 2nd ed.; Springer International Publishing: Cham, Switzerland, 2017; pp 453–481.

[7] Shrestha, P. R.; Cheung, K. P.; Member, S.; Campbell, J. P.; Ryan, J. T.; Baumgart, H. Accurate Fast Capacitance Measurements for Reliable Device Characterization. *IEEE TRANSACTIONS ON ELECTRON DEVICES*. **2014**, *61*, 2509–2514.

[8] Kim, J.-H.; Shrestha, P. R.; Campbell, J. P.; Ryan, J. T.; Nminibapiel, D.; Kopanski, J. J.; Cheung, K. P. Rapid and Accurate C–V Measurements. *IEEE TRANSACTIONS ON ELECTRON DEVICES*. **2016**, *63*, 3851–3856.

[9] Cao Q., Xia M.; Kocabas, C.; Shim, M.; Rogers, J. A.; Rotkin, S. V. Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors. *Appl. Phys. Lett*., **2007**, *90*.

[10] Saito, R.; Dresselhaus, G; Dresselhaus, M. *Physical Properties of Carbon Nanotubes*; Imperial College Press: London, 1998.

[11] https://amolf.nl/wp-content/uploads/2016/09/datasheets_LOR_datasheet.pdf

[12] https://www.microchemicals.com/micro/tds_az_1500_series.pdf