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Supplementary Information

Modulated wafer-scale WS_2 films based on atomic-layer-deposition for various device applications

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Fig. S5 †Process diagram of Nb-doped WS_2.

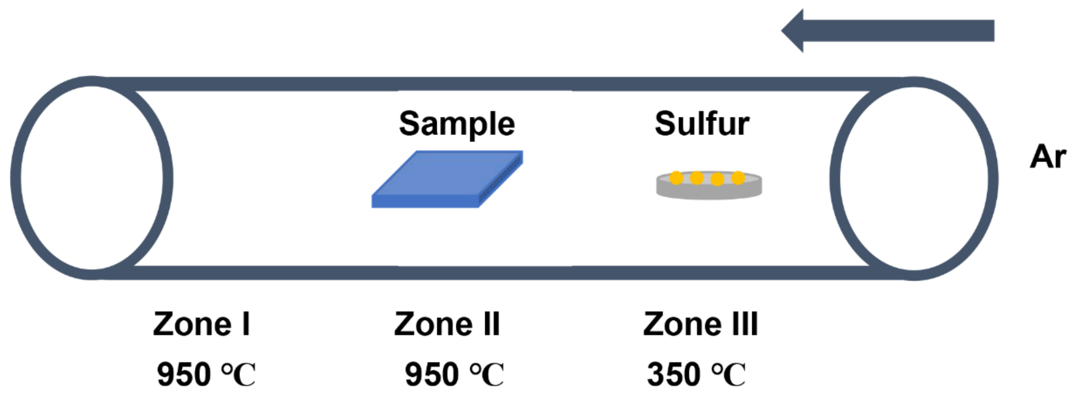

Fig. S1 | The annealing process of WS_2 film. The as-deposited samples were placed in a quartz boat in the center of Zone II, and 0.5 g sulfur powder was placed in Zone III carried by a quartz boat. The distance of samples and sulfur powder is 30cm. Argon (10 sccm, 99.999%) was chosen as the carrier gas. The samples were annealed for 2 h in a 4-inch quartz tube at a base pressure of 10 Pa.

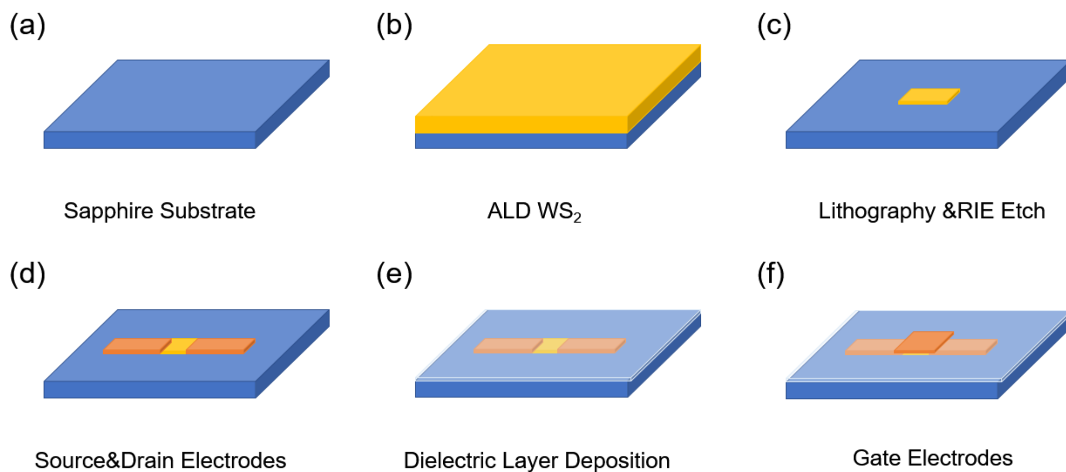

Fig. S2 | Detailed fabrication process of WS_2 FETs. Top-gate FETs for WS_2 and Nb-doped WS_2 films were fabricated through CMOS-compatible processes. After annealing in S atmosphere, photolithography was used to define channel area and was etched by CF_4/Ar (20/10 sccm) in RIE. Source and drain electrodes were patterned by photolithography and metalized by Ti/Au (10/70 nm) for WS_2 N-FETs and Ti/Pt (10/70 nm) for Nb-doped WS_2 P-FETs via PVD. Al_2O_3 gate oxide was deposited by ALD at 250 °C. The precursors for Al_2O_3 were TMA and H_2O, respectively. After top-gate patterning, 10/70 nm Ti/Au was deposited by PVD.

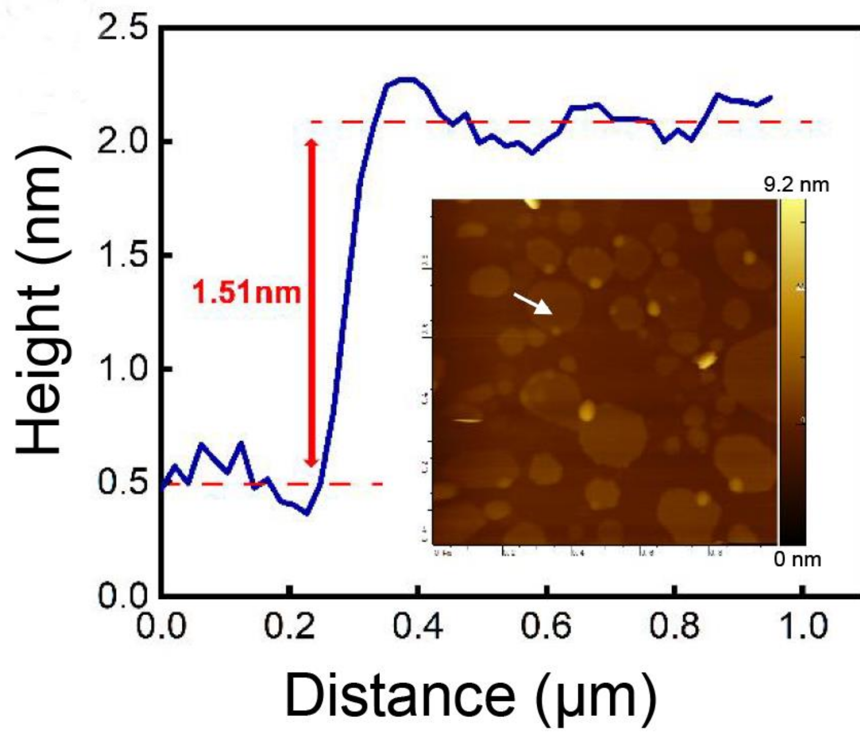

Fig. S3 | Thickness of WS_2 with 200 ALD cycles.

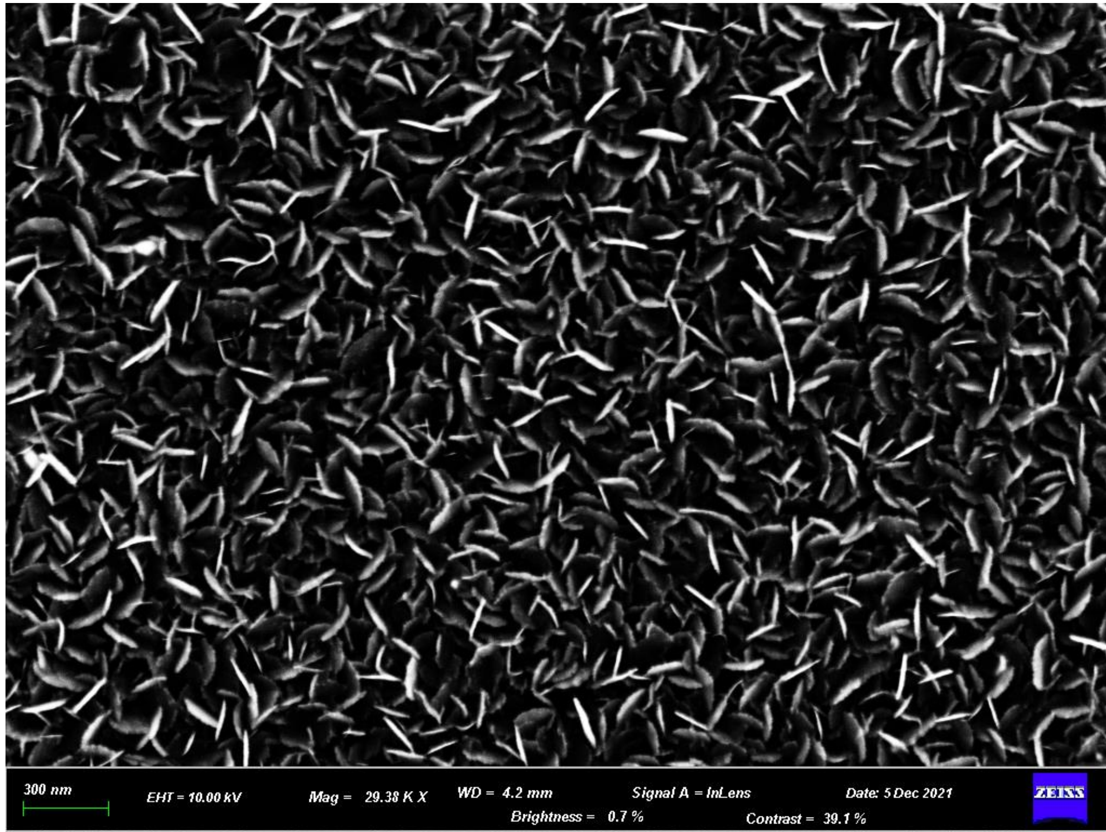

Fig. S4 | SEM image of WS_2 film with 800 cycles.

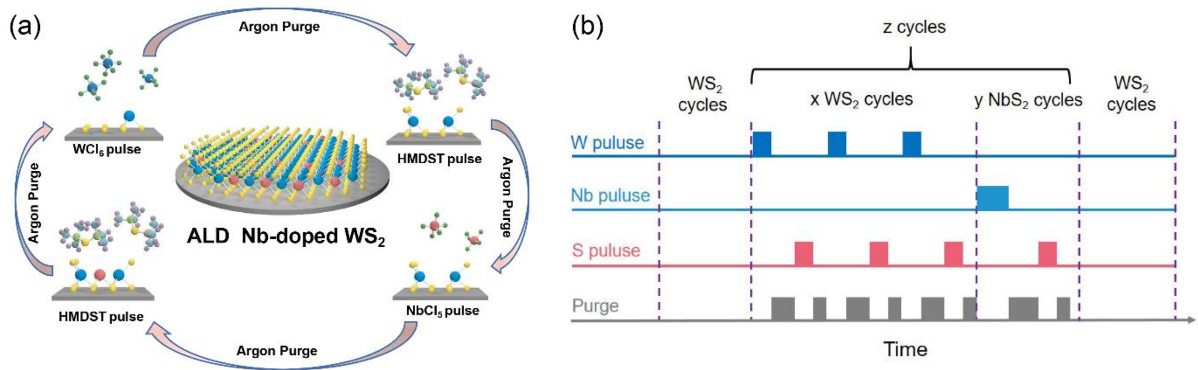

Fig. S5 | Process diagram of Nb-doped WS_2. The Nb doping process consists of z large cycles, and every large cycle contains x cycles of WS_2 and y cycles of NbS_2.