Electronic Supplementary Material (ESI) for RSC Advances.

Supplementary Information

Synaptic plasticity and learning behaviour in multilevel memristive device

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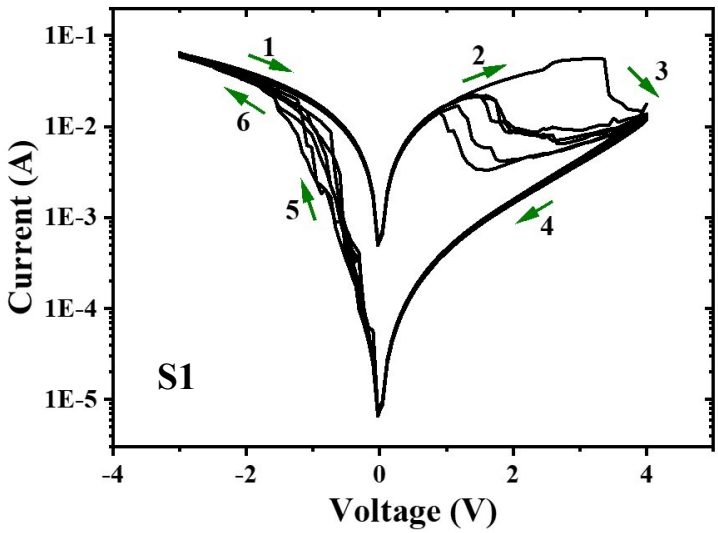

Figure S1: I-V Characteristics by sweeping the voltage from -3V to 0V to 4V for SET operation and 4V to 0V to -3V for RESET operation. V_{RESET} have a wide voltage window but V_{SET} shows the good reproducibility.

Here we sweep the voltage from -3V to 0V to 4V and the 4V to 0V to -3V to switch the device from LRS to HRS and HRS to LRS, respectively. Some of the device was switched easily in the low voltage regime but it was created the problem in the repeatability of RESET voltage (LRS to HRS) as shown in above figure. During SET voltage (HRS to LRS), device was switched easily with the repeatable way. Due to these limitations, we tried to improve it by sweeping the voltage from -3.5V to 0V to 4.5V and 4.5V to 0V to -3.5V as we mentioned in the main manuscript and we obtained the better repeatable results.

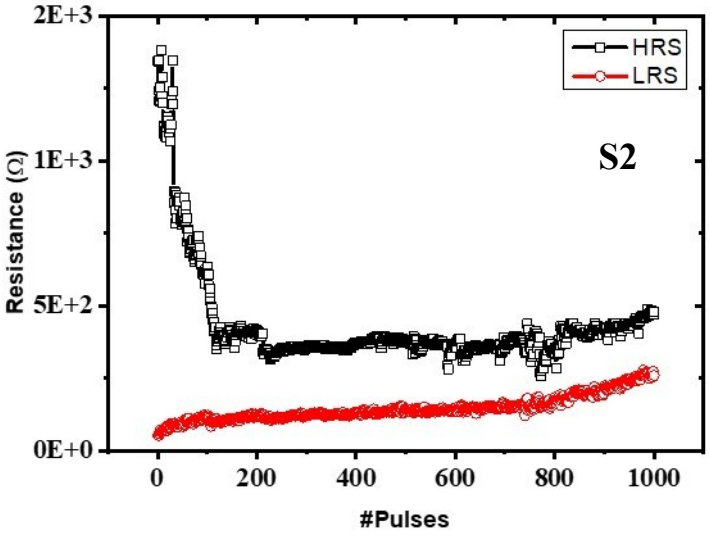

Figure S2: Endurance cycle in a linear scale by applying 10^3 write and read pulse cycles. Initially the HRS decays rapidly and then approaching towards the stable state.

Figure S2 is similar to the inset of figure 3(c) of the main manuscript. It is maintaining the same ratio between two resistance states (HRS and LRS) as we mentioned in the main manuscript.