Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

The Supplemental Material for "Performance Limit of One Dimension SbSI Nanowires Transistors"

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Content

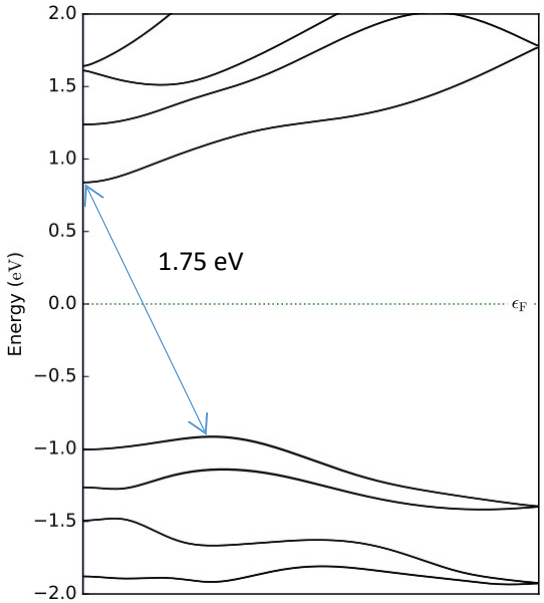

Fig. S1. Band structure of SbSI nanowire.

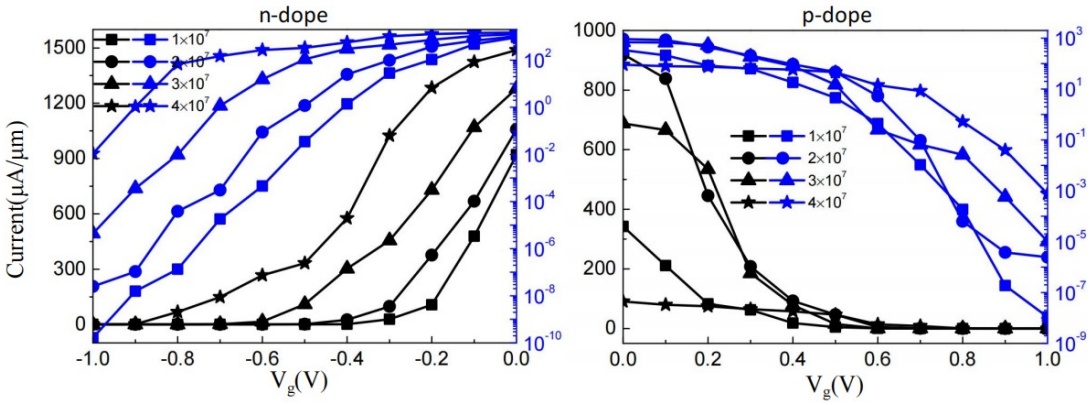

Fig. S2. The Current-Voltage attributes of SbSI FETs with different doping type and doping concentration. The value for bias voltage was 0.64 V.

Table s1. The doping concentration and the maximum currents

Doping type	Doping concentration (/m)	Maximum currents (μA/μm)	SS (mV/dec)
P-type	1×10^7	342.31	79.2
	2×10^7	919.93	58.7
	3×10^7	687.94	107.3
	4×10^7	90.83	207.0
N-type	1×10^7	921.10	57.8
	2×10^7	1058.20	65.7
	3×10^7	1280.33	91.3
	4×10^7	1488.33	454.0

Table s2. Criteria of the sub-5 nm Lg GAA SbSI FETs' ballistic efficiency versus the 2028 requirements of the ITRS 2013 for the HP and LP applications. The n-doped.

	L_g (nm)	UL (nm)	*SS* (mV/dec)	I_{off} (μA/μm)	I_{on} (μA/μm)	I_{on}/I_{off}	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
HP	5	0	100.9	0.1	5791.28	5.79×10^4	0.302	0.100	0.371
		1	73.6	0.1	5684.99	5.68×10^4	0.278	0.094	0.342
		2	62.3	0.1	3296.23	3.30×10^4	0.167	0.097	0.205
		3	57.8	0.1	1643.82	1.64×10^4	0.073	0.085	0.089
	3	0	239.0	0.1	-	-	-	-	-
		1	116.2	0.1	4114.83	4.11×10^4	0.158	0.074	0.194
		2	80.3	0.1	2611.78	2.61×10^4	0.089	0.065	0.109
		3	70.9	0.1	1489.41	1.49×10^4	0.051	0.066	0.063
	1	1	286.3	0.1	-	-	-	-	-
		2	154.0	0.1	536.07	5.36×10^3	0.027	0.095	0.033
		3	105.9	0.1	975.44	9.75×10^3	0.018	0.036	0.023
LP	5	0	100.9	5×10^{-5}	-	-	-	-	-
		1	73.6	5×10^{-5}	1449.66	2.90×10^7	0.113	0.149	0.138
		2	62.3	5×10^{-5}	1233.98	2.47×10^7	0.081	0.126	0.099
		3	57.8	5×10^{-5}	758.92	1.52×10^7	0.048	0.121	0.059
	3	0	239.0	5×10^{-5}	-	-	-	-	-
		1	116.2	5×10^{-5}	-	-	-	-	-
		2	80.3	5×10^{-5}	118.86	2.38×10^6	0.024	0.385	0.029
		3	70.9	5×10^{-5}	489.63	9.79×10^6	0.023	0.092	0.029
	1	1	286.3	5×10^{-5}	-	-	-	-	-
		2	154.0	5×10^{-5}	-	-	-	-	-
		3	105.9	5×10^{-5}	-	-	-	-	-
ITRS HP 2028	5.1	-	-	0.1	900	9.00×10^3	0.60	0.423	0.24
ITRS LP 2028	5.9	-	-	5×10^{-5}	295	5.90×10^6	0.69	1.493	0.28

L_g: the gate length. UL: the underlap length. *SS*: the subthreshold swing. I_{off}: the off-state current. I_{on}: the on-state current. C_g: the gate capacitance. τ: the delay time. PDP: the power dissipation.

Table s3. Criteria of the sub-5 nm Lg GAA SbSI FETs' ballistic efficiency versus the 2028 requirements of the ITRS 2013 for the HP and LP applications. The p-doped.

	L_g (nm)	UL (nm)	*SS* (mV/dec)	I_{off} (μA/μm)	I_{on} (μA/μm)	I_{on}/I_{off}	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
HP	5	0	125.0	0.1	2885.42	2.89×10^4	0.417	0.277	0.512
		1	71.1	0.1	2588.87	2.59×10^4	0.338	0.251	0.416
		2	64.4	0.1	1618.59	1.62×10^4	0.267	0.317	0.328
		3	58.7	0.1	873.82	8.74×10^3	0.168	0.369	0.206
	3	0	224.0	0.1	-	-	-	-	-
		1	135.3	0.1	2071.91	2.07×10^4	0.212	0.197	0.261
		2	86.1	0.1	1240.91	1.24×10^4	0.118	0.183	0.145
		3	80.8	0.1	731.39	7.31×10^3	0.088	0.231	0.108
	1	1	382.8	0.1	-	-	-	-	-
		2	208.1	0.1	418.73	4.19×10^3	0.028	0.128	0.034
		3	177.7	0.1	479.49	4.79×10^3	0.024	0.097	0.030
LP	5	0	125.0	5×10^{-5}	-	-	-	-	-
		1	71.1	5×10^{-5}	977.97	1.96×10^7	0.312	0.613	0.384
		2	64.4	5×10^{-5}	1090.39	2.18×10^7	0.223	0.392	0.274
		3	58.7	5×10^{-5}	672.02	1.34×10^7	0.117	0.335	0.144
	3	0	224.0	5×10^{-5}	-	-	-	-	-
		1	135.3	5×10^{-5}	-	-	-	-	-
		2	86.1	5×10^{-5}	-	-	-	-	-
		3	80.8	5×10^{-5}	306.56	6.13×10^6	0.045	0.284	0.056
	1	1	382.8	5×10^{-5}	-	-	-	-	-
		2	208.1	5×10^{-5}	-	-	-	-	-
		3	177.7	5×10^{-5}	-	-	-	-	-
ITRS HP 2028	5.1	-	-	0.1	900	9.00×10^3	0.6	0.423	0.24
ITRS LP 2028	5.9	-	-	5×10^{-5}	295	5.90×10^6	0.69	1.493	0.28

L_g: the gate length. UL: the underlap length. *SS*: the subthreshold swing. I_{off}: the off-state current. I_{on}: the on-state current. C_g: the gate capacitance. τ: the delay time. PDP: the power dissipation.