Electronic Supplementary Information

High-Performance Logic Inverter by Mixed-Dimensional WSe_2/n^+-Si and MoS_2/p^+-Si Junction Field-effect Transistors

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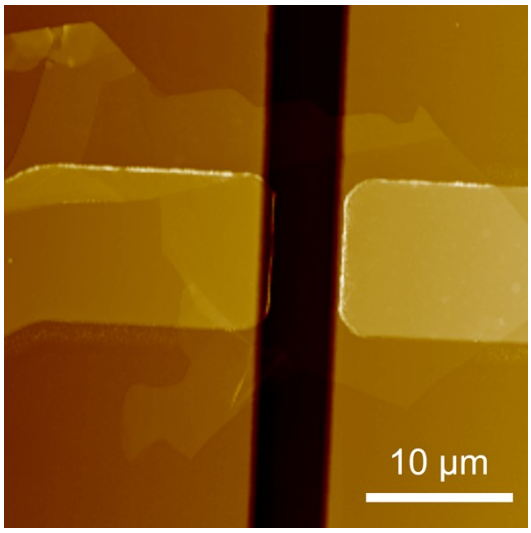

Fig. S1 Atomic force microscopy image of the WSe_2/n^+-Si JFET device.

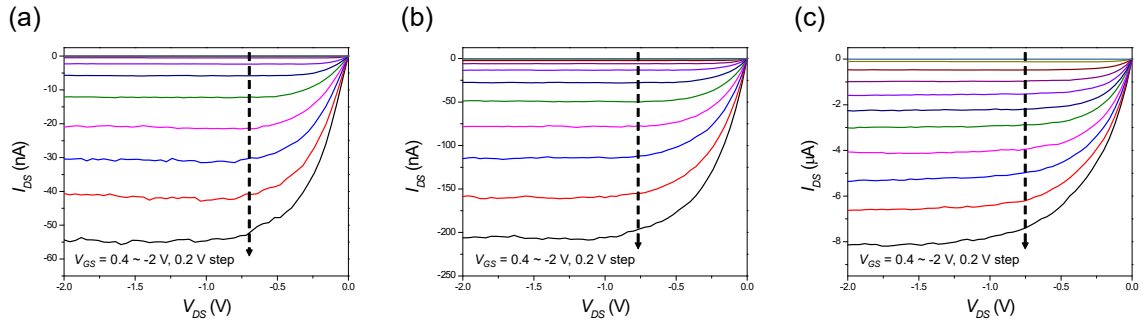

Fig. S2 Output characteristics of (a) pristine, (b) PMMA-coated, and (c) PBVE-coated WSe_2 JFET devices at various gate voltages.

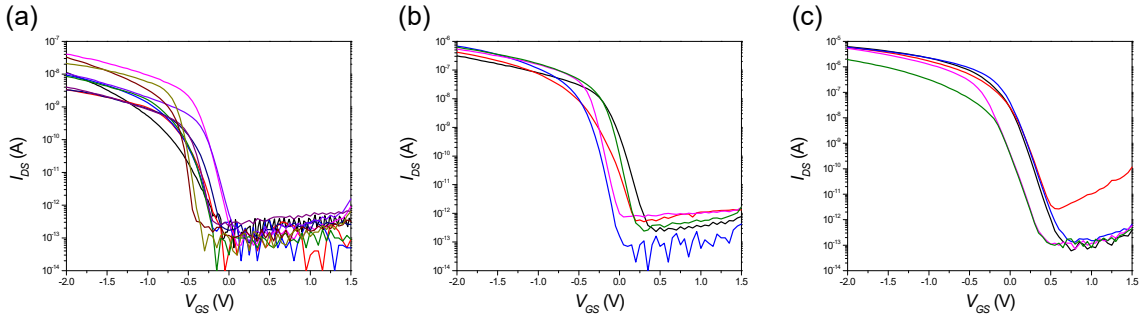

Fig. S3 Transfer characteristics of (a) 10 pristine devices, (b) 5 PMMA-coated devices, and (c) PBVE-coated devices used in the statistical variation analysis (all the data were measured at a drain voltage of −1 V).

Supplementary Note 1) Extraction contact resistance and carrier concentration from typical WSe_2 FETs.

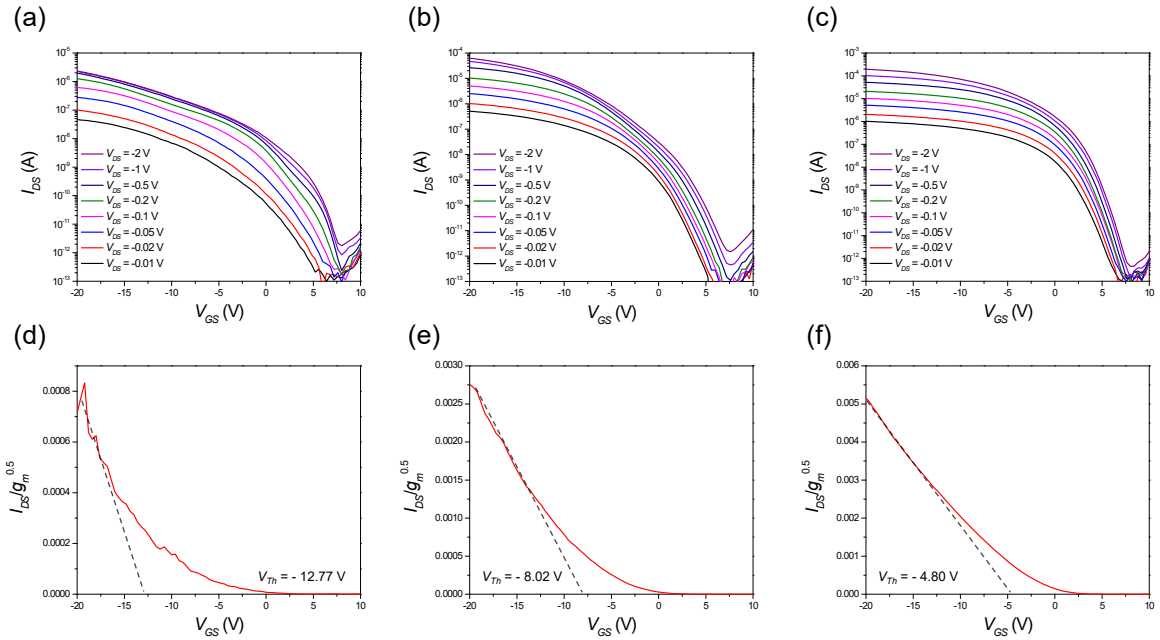

Fig. S4 Transfer characteristics of typical WSe_2 FETs: (a) pristine, (b) PMMA-coated, and (c) PBVE-coated samples; Y-function calculation of FETs with (d) pristine, (e) PMMA-coated, and (f) PBVE-coated samples.

The contact resistance values were obtained using the Y-function method.[1] Considering the contact resistance, the voltage additionally drops at the interface between the source and drain electrodes. The *I–V* characteristics can be described as:

$$I_{DS} = \left(\frac{\mu_0}{1+\theta(V_{GS}-V_{Th})}\right) C_{ox}\frac{W}{L}(V_{GS}-V_{Th})V_{DS}$$

where θ is the mobility reduction coefficient, μ_0 is the low-field mobility, V_{Th} is the threshold voltage, and C_{ox} = 1.28×10^{-8} F/cm^2 is the back-gate capacitance from SiO_2 thickness of 270 nm.

If the contact resistance is independent of the gate voltage, then the Y-function can be defined as:

$$Y = \frac{I_{DS}}{\sqrt{g_m}} = \left(\frac{\mu_0 C_{ox} V_{DS} W}{L}\right)^{0.5} (V_{GS} - V_{Th})$$

From $\theta \approx \mu_0 C_{ox} R_c W/L$, the contact resistance R_c can be obtained. As a result, the contact resistance decreased from 318 kΩ for the pristine device, to 34.9 kΩ and 15.6 kΩ for PMMA, and PBVE-coated devices, respectively.

The carrier concentration of the pristine WSe_2 device was extracted from the linear fitting of the output curve at zero-gate voltage and low drain voltage region using the following equation:[2]

$$\rho = \left(\frac{dI_{DS}}{dV_{DS}}\right)^{-1} \frac{tW}{L}, \qquad N_a = \frac{1}{e\rho\mu}$$

where ρ is the conductivity, N_a is the hole carrier concentration, e = 1.602×10^{-19} C is the electron unit charge, μ is the hole mobility, and t is the channel thickness. In the case of PMMA and PBVE-coated samples, the carrier concentrations were obtained from the threshold voltage shift using the following equation.[3]

$$n = \frac{C_{ox} \Delta V_{Th}}{e}$$

where n is the variance of the carrier concentration on a two-dimensional scale (cm^{-2}), ΔV_{Th} is the threshold voltage shift from the pristine sample. From the forementioned equations, the hole carrier concentrations were calculated to be approximately 1.25×10^{15} cm^{-3} (= 1.25× 10^{9} cm^{-2}), 2.72×10^{17} cm^{-3} (= 3.80×10^{11} cm^{-2}), and 4.90×10^{17} cm^{-3} (= 6.38×10^{11} cm^{-2}) for pristine, PMMA-coated and PBVE-coated FET devices, respectively.

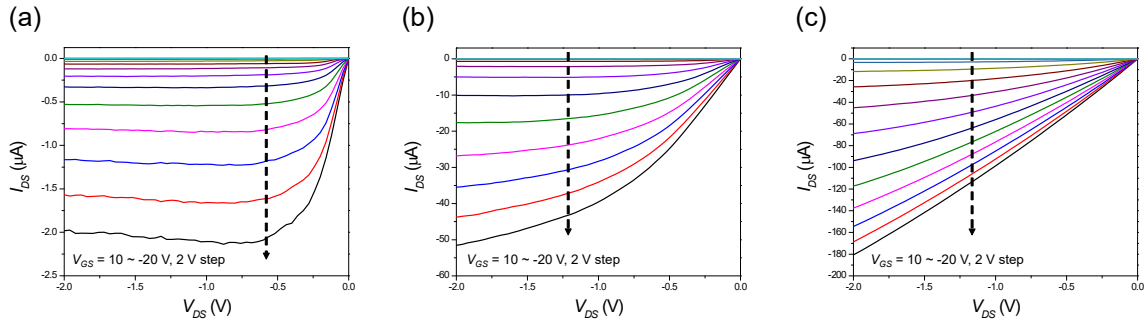

Fig. S5 Output characteristics of the typical WSe_2 FET with (a) pristine, (b) PMMA-coated, and (c) PBVE-coated devices at various gate voltages.

Supplementary Note 2) Low-frequency noise characteristics of the WSe_2/n^+-Si JFETs.

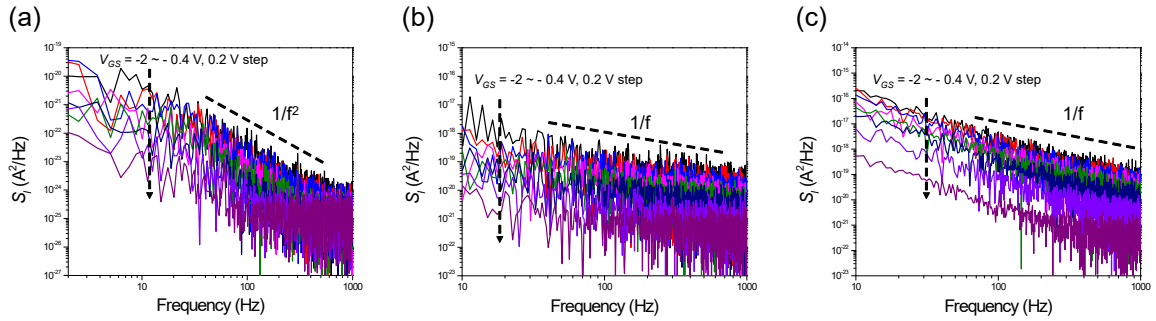

Fig. S6 Low-frequency noise characteristics of (a) pristine, (b) PMMA-coated, and (c) PBVE-coated JFETs measured at a drain voltage of −1 V (gate voltages range from −2 V to −0.4 V with 0.2 V steps).

Low-frequency noise behavior can be explained the following empirical equation:[4]

$$\frac{S_I}{{I_{DS}}^2} = \frac{A}{f^{\beta}}$$

where S_I is the current power spectral density, I_{DS} is the average drain current, A is the noise amplitude, f is the frequency, and β is the scaling exponent factor. In the case of PMMA- and PBVE-coated devices, the power spectral density showed the factor β close to unity, which follows 1/f noise, also called the flicker noise. This result indicates that the polymer coating treatment provides additional interface trap density between the polymers and WSe_2 channel, and is consistent with the mobility degradation after polymer doping. On the contrary, the pristine sample showed β values close to two properties, corresponding to the noise characteristics of the generation-recombination (G-R) process. It has been suggested that TMDs, such as $MoTe_2$, are sensitive to ambient conditions, and several oxygen atoms may affect the WSe_2 channel layer as defect sites.[5] This phenomenon has been observed in MoS_2 devices under low-temperature conditions with low carrier concentrations.[6] It can be

considered that our pristine WSe_2 JFET showed G-R noise at room temperature conditions owing to the low concentration of the pristine WSe_2 flake and nearly nonexistent channel/dielectric interface noise.

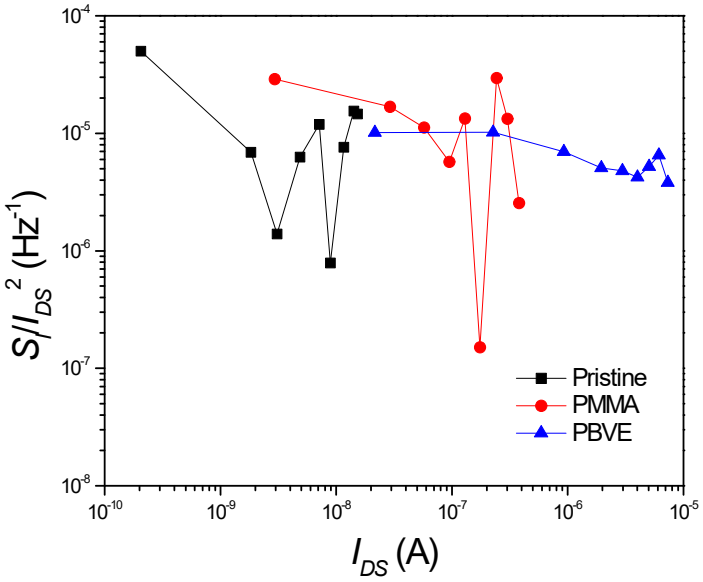

Fig. S7 Normalized noise power spectral densities of the pristine, PMMA, and PBVE-coated WSe_2 JFET devices.

Because our polymer doping affects not only the channel area, but also the contact resistance, we must consider the influence of contact resistance. The noise caused by the contact resistance was different from the channel noise. For example, the normalized power spectral density gradually decreases as the drain current increases owing to the channel noise.[7] Conversely, the normalized power spectral density gradually increases with contact noise.[8] However, such tendencies owing to the contact resistance were not observed in Fig. S7. This result indicates that the low-frequency noise which originating from the contact resistance can be ignored.

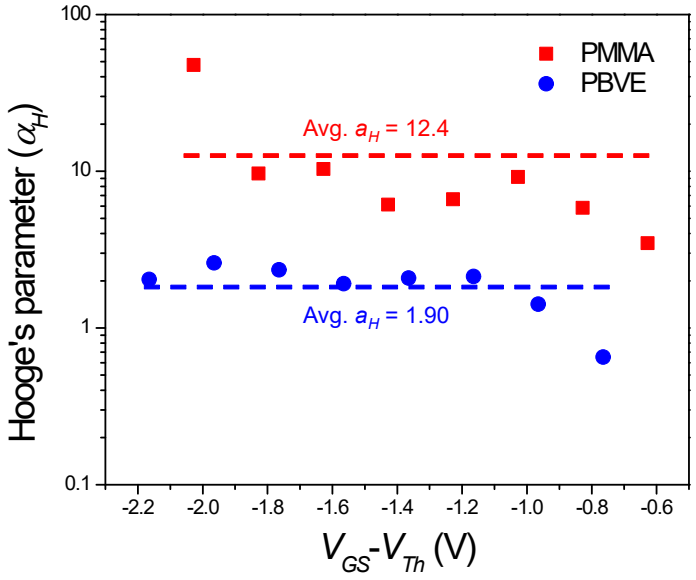

Fig. S8 The Hooge's parameter extracted from the 1/f noise characteristics as a function of gate voltage for PMMA and PBVE-coated WSe_2 JFET devices.

The 1/f noise characteristics can be analyzed by the two main perspectives. One is the Hooge mobility fluctuation (HMF) model, and the other is the carrier number fluctuation (CNF) model. The HMF model originate from random mobility fluctuation via lattice scattering, whereas the CNF model is responsible for the capture and release of carriers at interface and gate oxide trap states. Although typical 2D MOSFETs are generally explained by the CNF model, we applied the HMF model to our doped WSe_2 devices. The first reason is because of the device structure. MESFETs and JFETs are not consist of gate oxide layer. The HMF model was also applied to ZnO MESFET in previous research.[9] The other reason originates from thickness of the WSe_2 channel layer. Previous research showed that MoS_2 transistors follow CNF model in strong-accumulation or single and few-layer thickness of the

channel.[10] While HMF model can be applied to the MoS_2 transistors in relatively thick channel or weak-accumulation state. In the case of our research, the WSe_2 JFET devices cannot be strongly accumulated and consist of relatively thick WSe_2 flakes. Because of the reasons above, the HMF model is reasonable for our doped WSe_2 JFETs. The HMF model of the 1/f noise can be expressed by the equation in the saturation region:[9]

$$S_I = \frac{e\mu(V_{GS} - V_{Th})I_{DS}\alpha_H}{L^2 \quad f}$$

where, α_H is the dimensionless Hooge's parameter. The α_H was first suggested as an universal constant having a value of 2×10^{-3}.[11] However, it was quickly discovered that the α_H have dependency of fabrication process and material quality.[12] Nevertheless, the α_H can be used as indicator for evaluating the performance of the devices. In organic transistors, the α_H is reported to be high values about 10.[13,14] The α_H values of PMMA and PBVE-coated devices are presented in Fig. S8. The PBVE-coated JFET device showed the average α_H of 1.90. However, the PMMA-coated device represented higher α_H value than that of PBVE-coated device, of 12.4. The result indicates that PMMA coting provide stronger surface scattering than that of PBVE coating, and this is consistent with the mobility values above.

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