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Supporting Information for

Nanoristors: Highly Uniform, Sub-500-Millivolt, Large-Scale, and Robust Molybdenum Disulfide Nanograined Memristors

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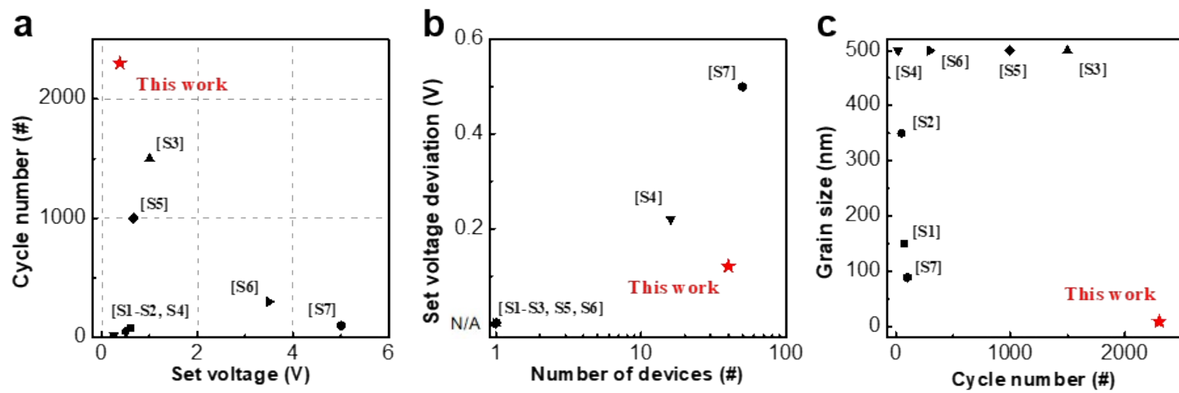

Fig. S1 Performance comparison of the proposed device with previous work. (a) Plot of cycle number versus set voltage, and (b) plot of set voltage deviation versus number of devices. (c) Plot of grain size versus cycle numbers.

Table S1. Comparison of memristor performance with previous research.

Structure	Set (V)	Reset (V)	Endurance cycles (pulse)	Retention time(s)	Fabrication Methods	Uniformity (set/reset)(V)	Scale	Year	Ref.
Ag/ MoS_2 (PECVD)/Au	-0.38	0.28	~2.2×10^3 (~5.3×10^5)	>2.5×10^4	PECVD	±0.12/±0.04	Large-area (40 devices)	2023	This work
Pd/WS_2/Pt	0.60	-0.20	75	3.5×10^3	liquid dispersion	N/A	Flake (1 device)	2019	Ref [S1]
ITO/BP@PS/ITO	- 0.50	2 .00	50	10^4	liquid dispersion	N/A	Large-area (1 device)	2020	Ref [S2]
MoS_2/NbS_2/NbO_x	1.00	-1.00	1.5×10^3	3.6×10^4	CVD	N/A	Flake (1 device)	2020	Ref [S3]
Cu/MoS_2/Au	0.25	-0.15	20	1.8×10^4	MOCVD	±0.22/±0.14	Large-area (16 devices)	2019	Ref [S4]
Ag/1T-MoS_2/Ag	0.66	-0.98	10^3	N/A	exfoliation	N/A	Flake (1 device)	2019	Ref [S5]
Au/Ti/Gr/h-BN/Gr/Au	3.50	-1.00	3×10^2	N/A	CVD	N/A	Large-area	2019	Ref [S6]
Al/MoS_2-MoO_x/Al (unipolar)	-5.00	-0.50	10^2	10^4	colloidal synthesis	±0.5/±0.3	Large-area (50 devices)	2018	Ref [S7]

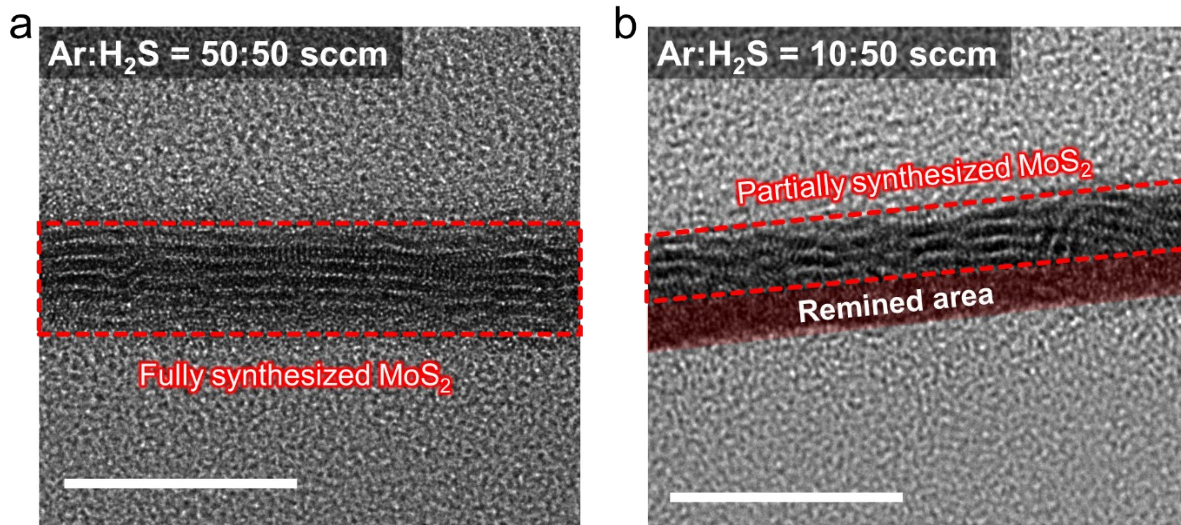

Fig. S2 HRTEM cross-section view of the MoS_2 prepared at the condition of (a) Ar:H_2S = 50:50 sccm, (b) Ar:H_2S = 10:50 sccm. (scale bar = 10 nm)

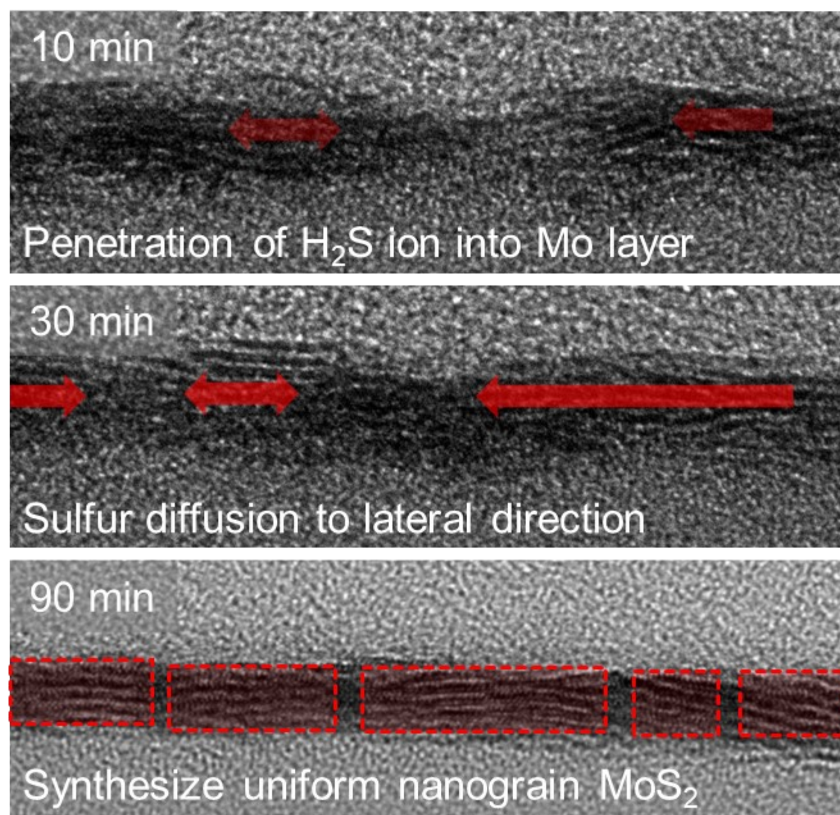

Fig. S3 HR-TEM cross-section view images of the MoS_2 synthesized for (a) 10 min, (b) 30 min, and (c) 90 min.

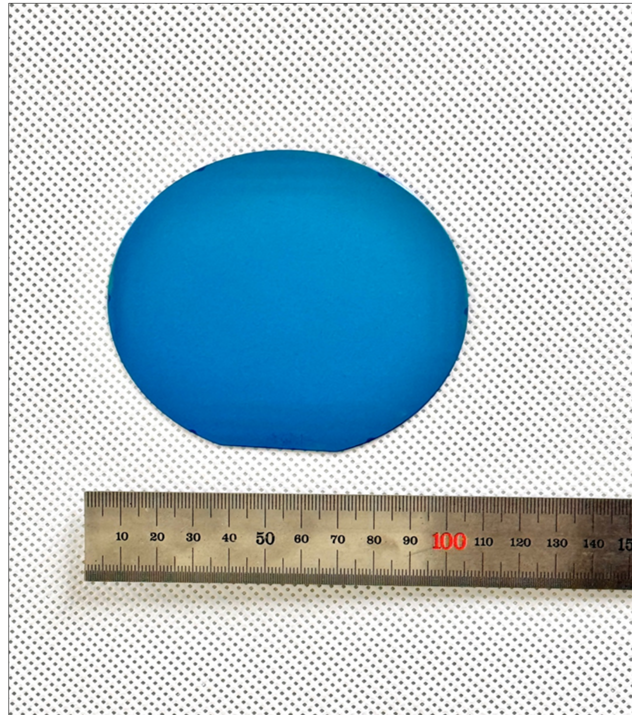

Fig. S4 Image of 4-inch scale PECVD grown MoS_2 layer synthesized on the SiO_2/Si wafer.

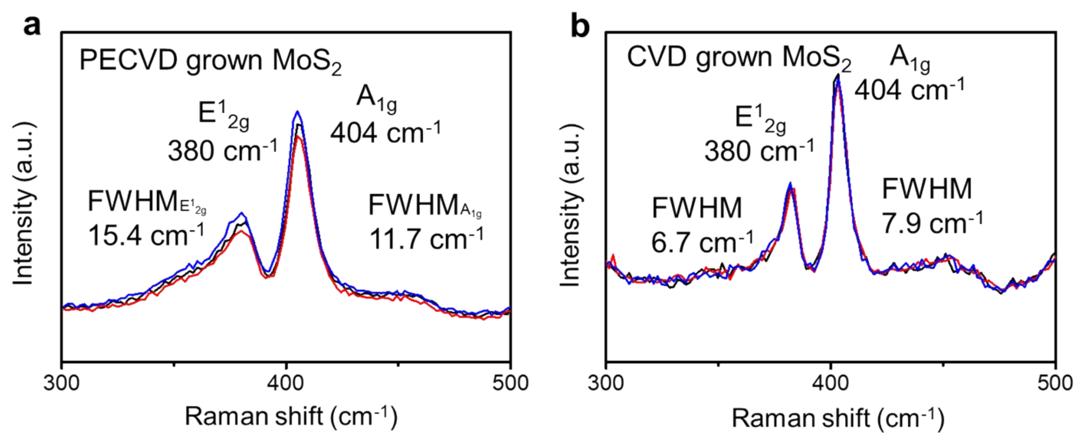

Fig. S5 Raman spectra of (a) the PECVD-grown MoS_2 and (b) CVD-grown MoS_2.

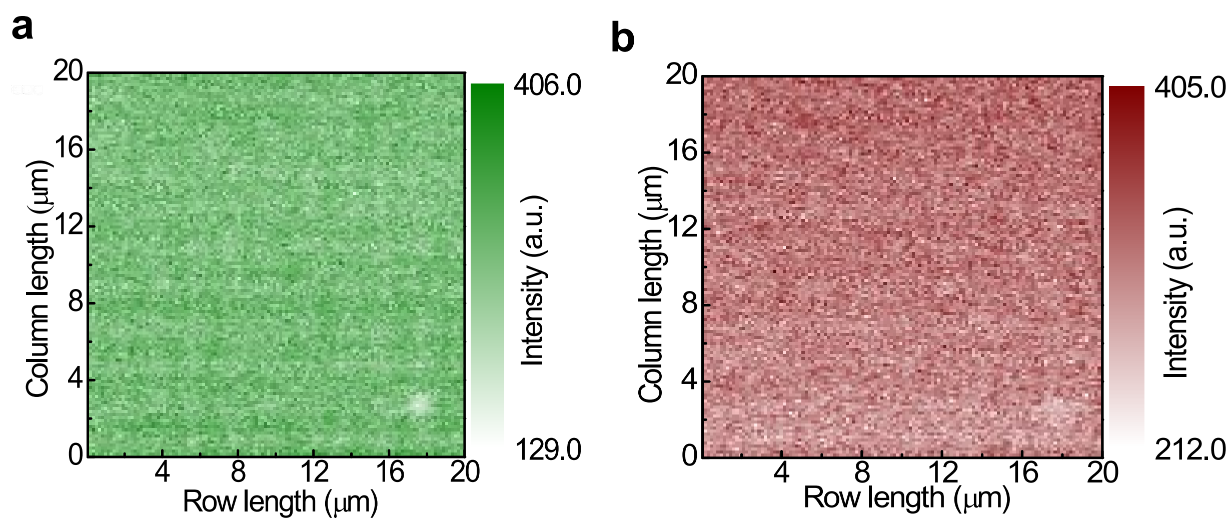

Fig. S6 Raman mapping image of MoS_2 layer (20 μm × 20 μm size). (a) A_{1g} and (b) E^1_{2g} mode.

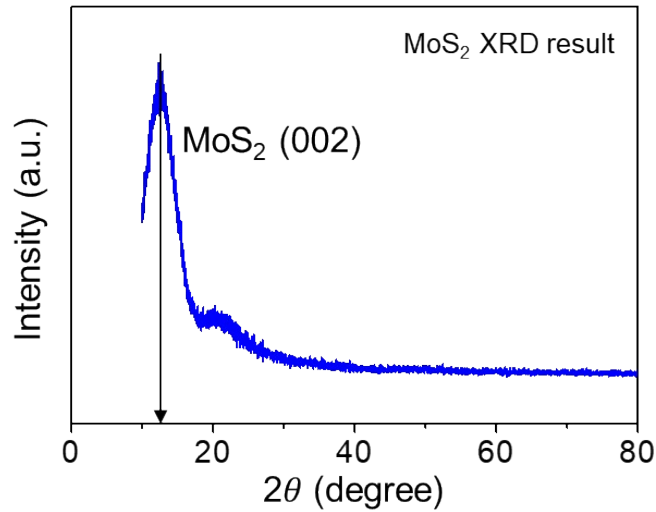

Fig. S7 XRD result of the PECVD grown nanograin MoS_2 which the grain size is estimated as 4.0 nm scale.

The grain size of nanograin MoS_2 is calculated with the Scherrer formula:

$$D_p = \frac{0.94\,\lambda}{\beta \cos\theta}$$

Where D_p is average crystalline size, β is line broadening in radians, θ = Bragg angle, λ = X-ray wavelength. In this case, we calculated the grain size using the peak at 13.1 degree which is closely related to MoS_2 crystal. The full width at Half Maximum (FWHM) is inserted in β, and λ is 0.16418. Consequently, the grain size is estimated as 4.00 nm, showing a significantly matched value with the TEM result.

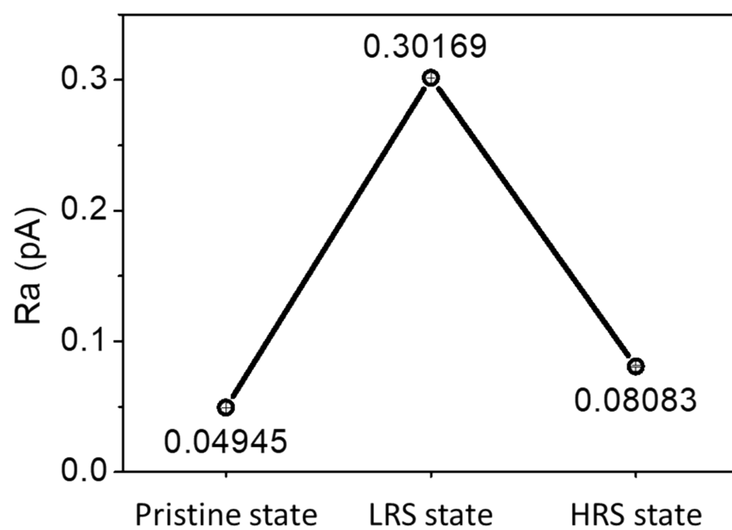

Fig. S8 The roughness average (Ra) of a measured current value for the pristine state, LRS state, and HRS state.

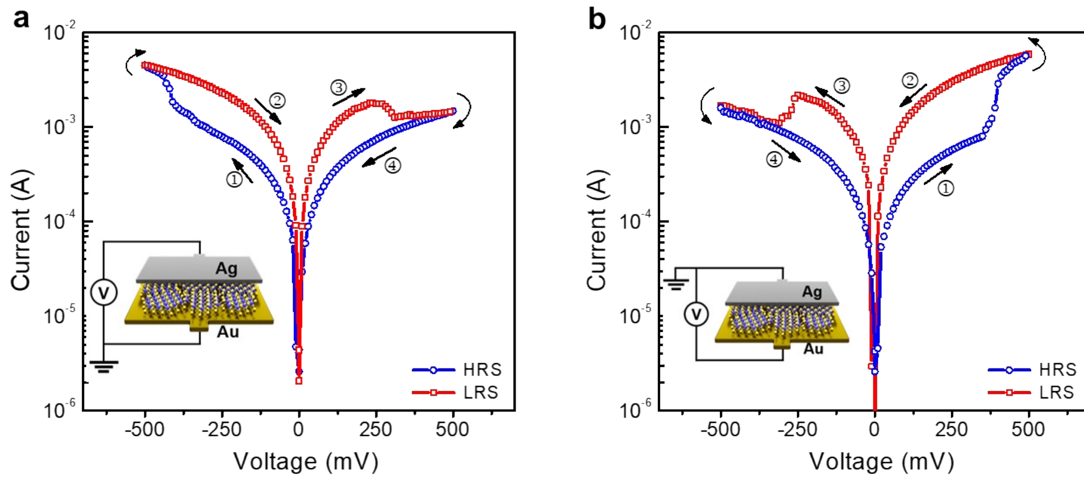

Fig. S9 Switching polarity control by swapping the applied voltage. (a) Au electrode set as ground, and (b) silver electrode set as ground.

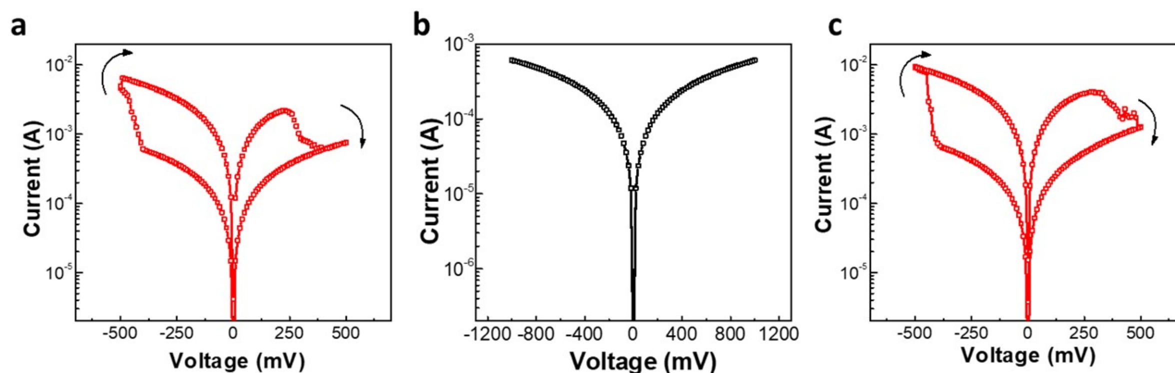

Fig. S10 Characterization of the MoS_2 nanoristor device with various conditions. (a) 20 times sweeping voltage from -0.5 V to 0.5 V of the MoS_2 nanoristor in the vacuum state. (b) 10 times sweeping voltage from -1 V to 1 V of the Au/Ti/MoS_2/Au/Ti vertical structure. (c) Current behavior of the nanoristor which is fabricated on PI-substrate (sweeping voltage range: -0.5 V to 0.5 V)

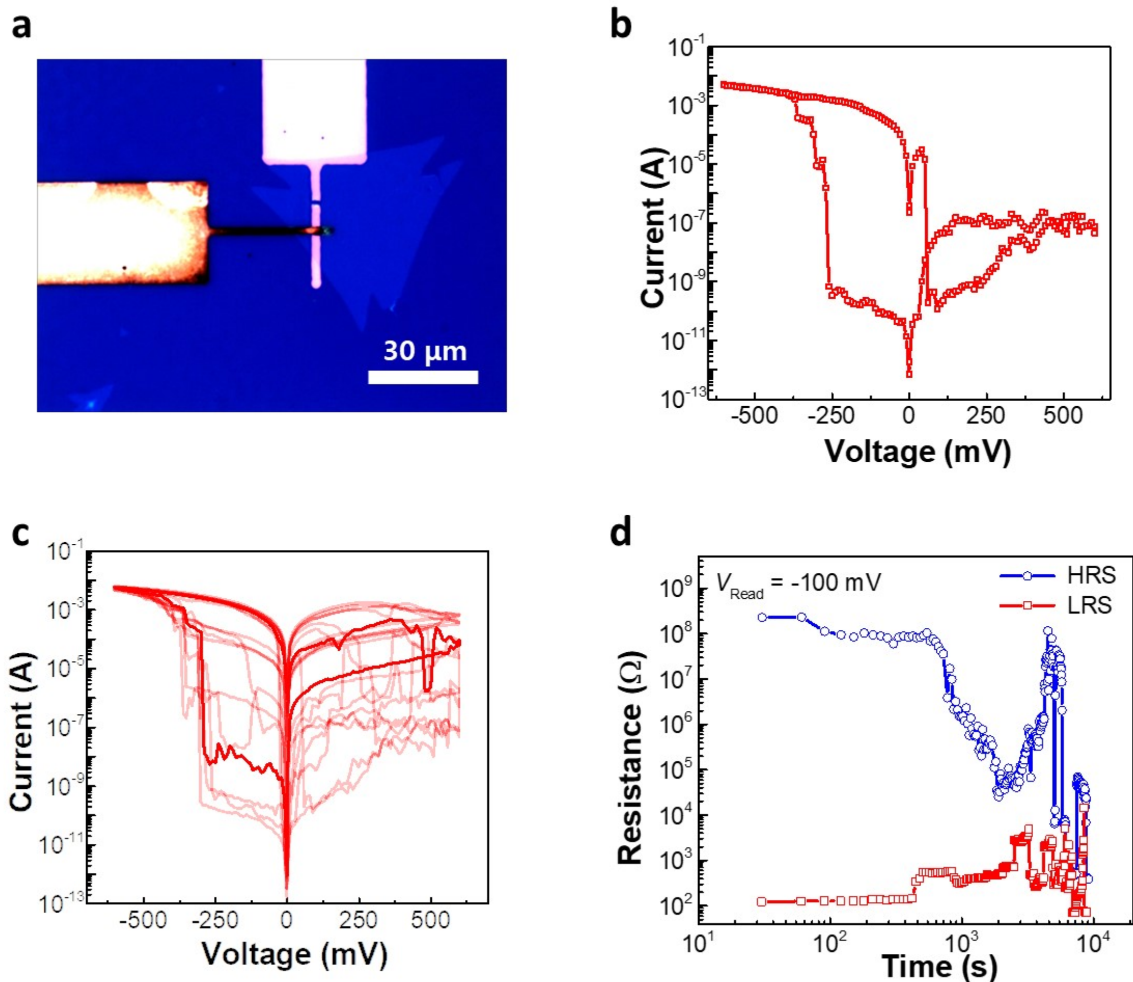

Fig. S11 (a) Optical image of memristor based on CVD-grown MoS_2. (Scale bar: 30 µm). (b) Typical *I*-*V* curve of CVD-grown MoS_2 memristor. (c) Bipolar switching curve of CVD-grown memristor with 10 times cumulative sweep. (d) Measured retention about 10^4 retention time at -100 mV read voltage.

To compare with the proposed nanograin MoS_2 memristor device, single crystalline MoS_2 was synthesized by chemical vapor deposition (CVD) process. CVD-grown MoS_2 (micrometer-sized grains) was transferred on patterned Au/Ti (50 nm/5 nm) bottom electrode (BEs) and top electrode (TEs) patterned of Ag (50 nm) was subsequently patterned by lift-off process mentioned in experimental section. The fabricated triangle shaped CVD-grown MoS_2 memristor device has a line width of 3 µm, shown in Fig. S5(a), S5(b) and S5(c) show a

bipolar switching and 10 times sweep I-V curve of CVD-grown MoS_2 with set voltage (V_{set}) = -260 mV. However, the CVD-grown MoS_2 memristor exhibit unstable device performance with unclear reset voltage (V_{reset}) and poor repeatability in comparison to the proposed nanoristor device. Furthermore, the retention characteristics also showed instability in which the resistance state was not stably maintained in the CVD-grown MoS_2 memristor (Fig. S5d). Based on the above results, it is concluded that larger grain size and lack of defect sites in the CVD-grown MoS_2 resulted in the unstable memristive operation.

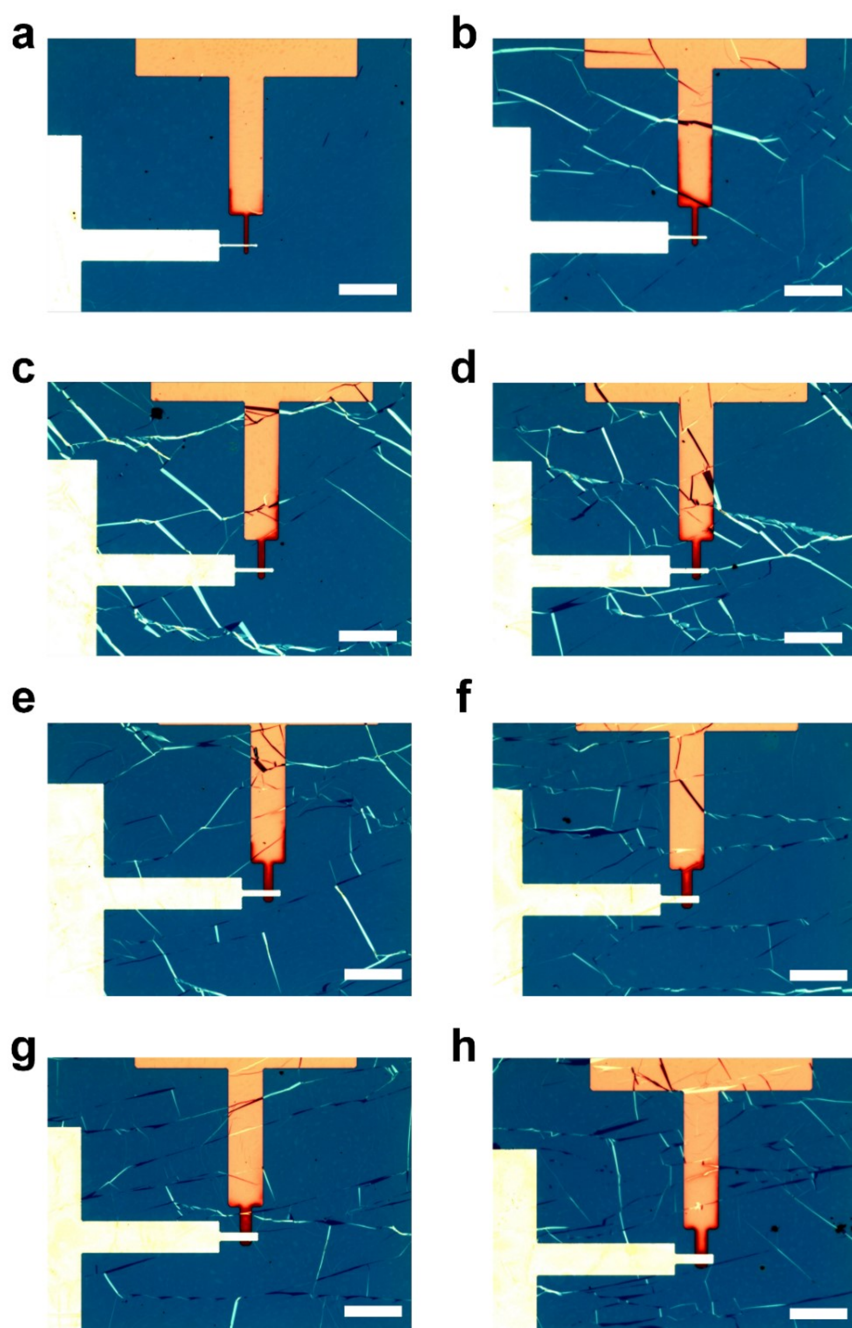

Fig. S12 Optical image of Nanoristors depending on metal line width of electrodes (Scale bar: 50 µm). (a) 3 µm, (b) 4 µm, (c) 5 µm, (d) 6 µm, (e) 7 µm, (f) 8 µm, (g) 9 µm, and (h) 10 µm.

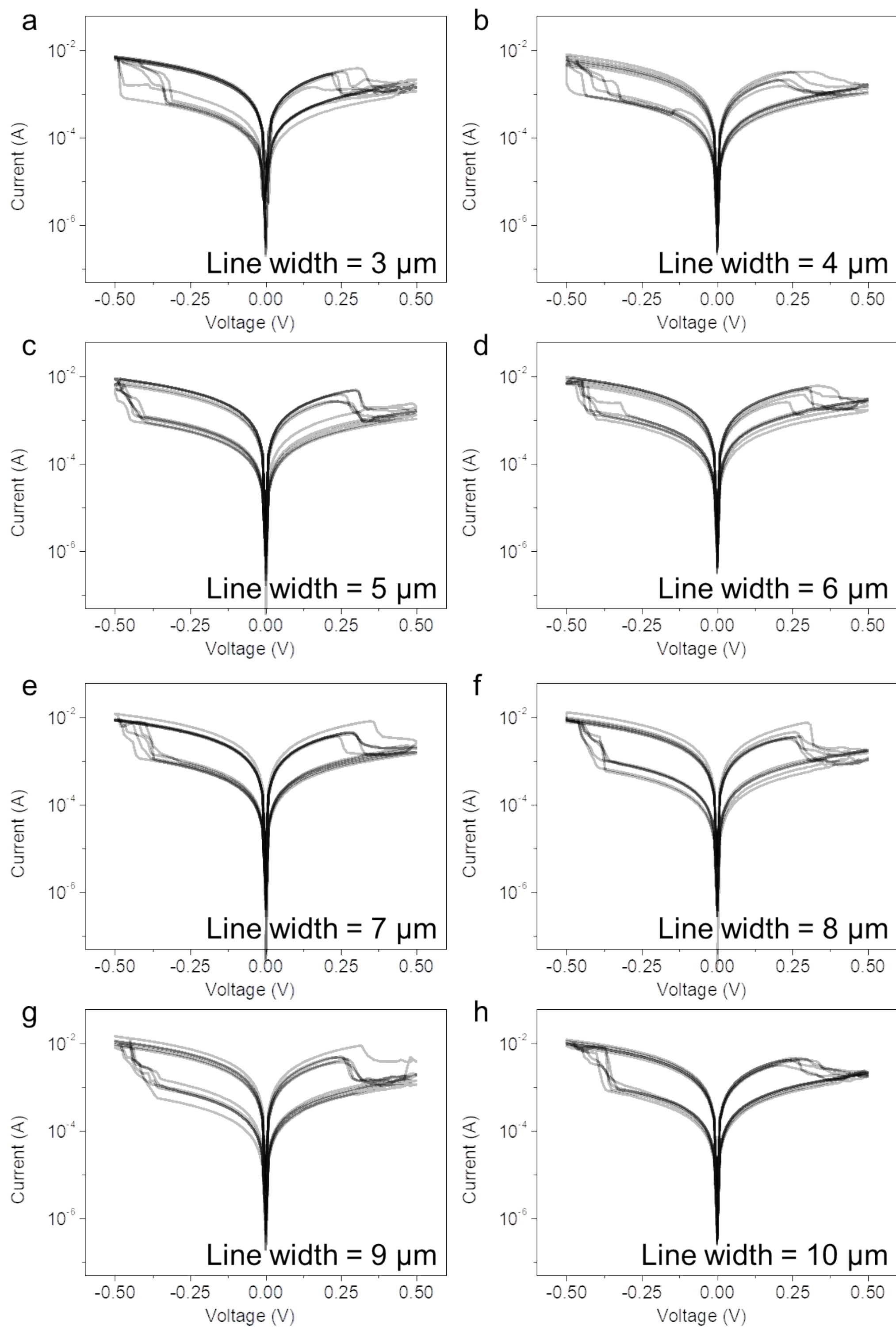

Fig. S13 5 cycles I-V curves along to width of the electrode. (a) 3 μm, (b) 4 μm, (c) 5 μm, (d) 6 μm, (e) 7 μm, (f) 8 μm, (g) 9 μm, and (h) 10 μm.

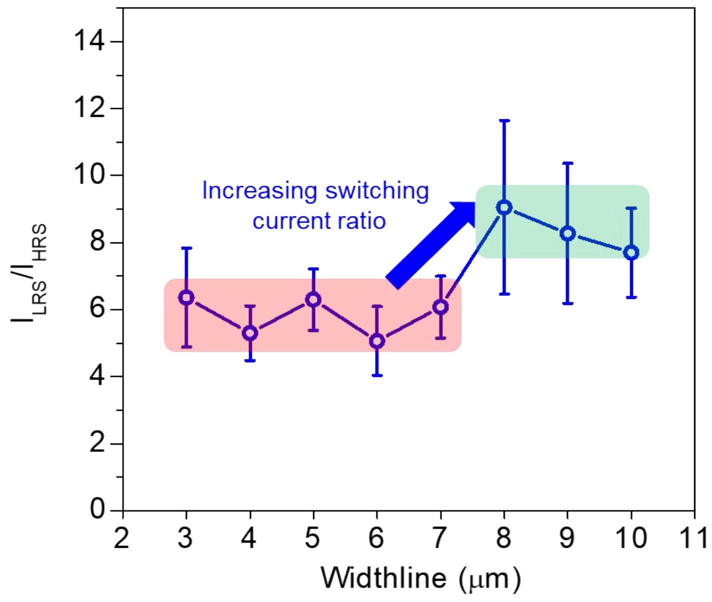

Fig. S14 The switching current ratio (I_{LRS}/I_{HRS}) as a function of electrode linewidth (3 to 10 μm).

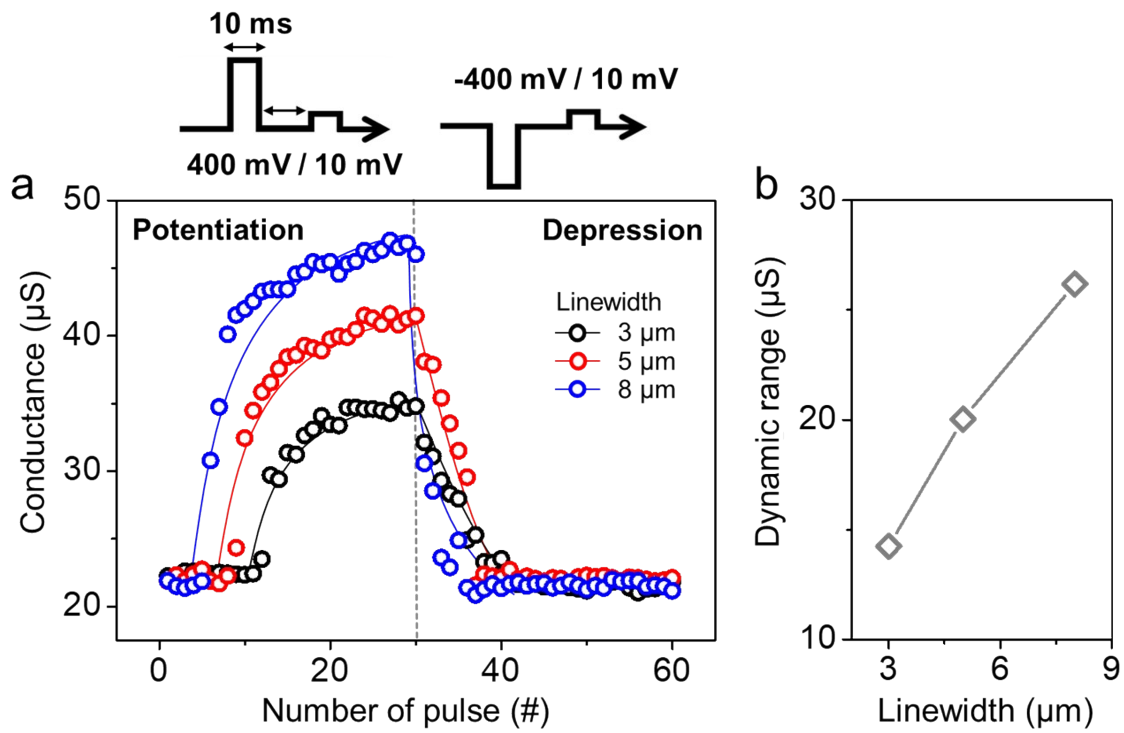

Fig. S15 (a) The result of conductance updates for the nanoristor with varying the electrodes linewidth (3, 5, and 8 μm). (b) Extracted dynamic range from the LTP/LTD curves measured under various electrode dimension conditions.

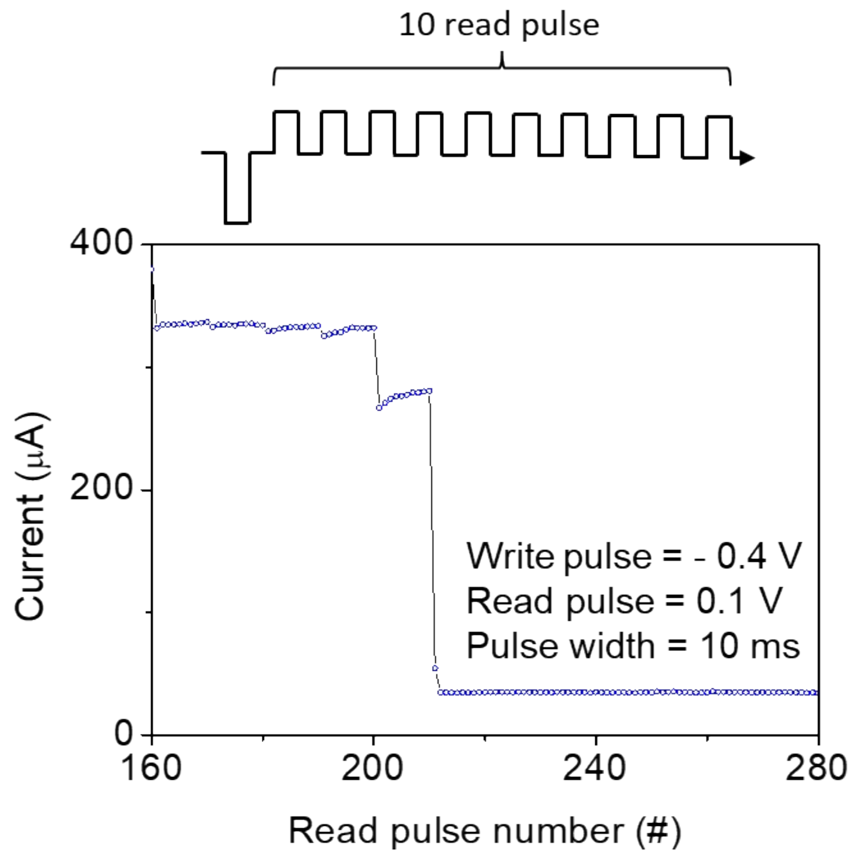

Fig. S16 Read-disturb immunity characteristics during the depression process.

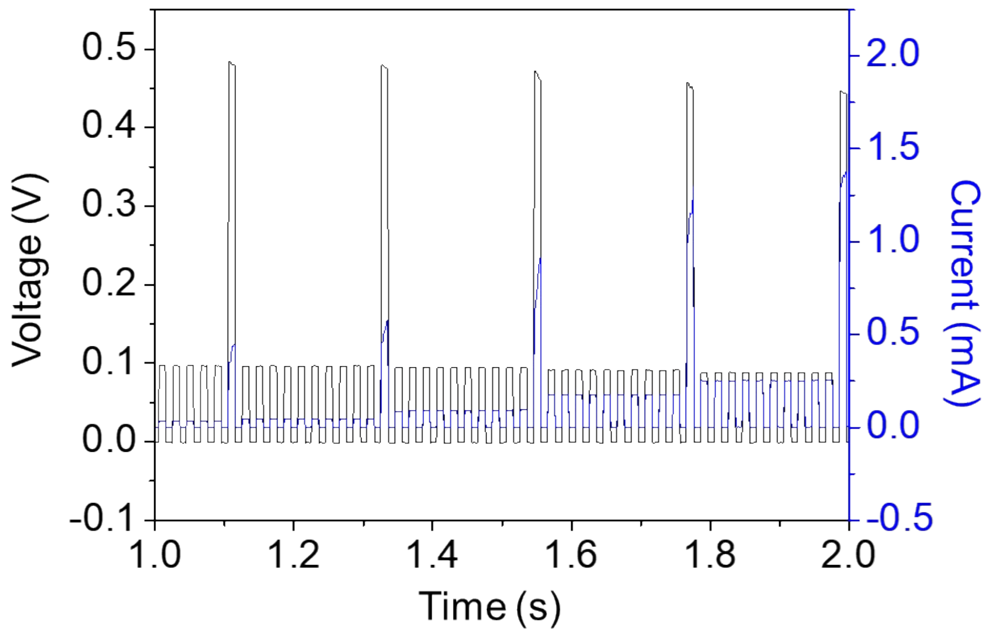

Fig. S17 *I-V* curve of the nanoristor operated in pulse programming mode.

The energy consumption during the programming and erasing can be estimated with the following equation:

$$E = V \times I \times T_{pulse\ width}$$

Here, E demote the energy consumption of the nanoristor during the programming and erasing process. V, I, and $T_{pulse\ width}$ means applied voltage, drain current, and pulse width, respectively. The read and write energy consumption of the nanoristor is estimated as 44.4 nJ for reading and 2.10 μJ for writing.

Supplementary information 1. The ANN simulation process

For the device-to-system simulation, we designed a two-perceptron artificial neural network (ANN) system for face recognition. The ANN with two crossbar architectures consists of 1024 input neuron layers, 20 middle neuron layers, and 3 output neuron layers, as shown in Fig. S18(a). In the face recognition system, an image sensor detects a human face and the detected pixels are converted into presynaptic spikes (V_{pre}) with delayed pulse timing to encode the analog information of pixel intensities (Fig. S18(b)).

In the input neuron layer, the input neurons consist of a waveform generator connecting the image sensor and a CMOS inverter. The 1024 input neurons are connected to pixels in the face image to emit V_{Pre}. As shown in Fig. S18(a), the presynaptic spikes (V_{pre}) emitted from the input neurons trigger the MoS_2 nanoristor-based synapse devices connected with the postsynaptic neurons to induce postsynaptic currents (I_{post}) based on the conductance of MoS_2 nanoristor. The I_{post} are integrated at a leaky integrator in the postsynaptic neuron. When the output voltage of the leaky integrator by the accumulated I_{post} is higher than a threshold voltage (V_{th}), the postsynaptic neuron utilizes a feedback network to fire a postsynaptic spike (V_{post}) through the waveform generator. Subsequently, the synaptic weights between the input neuron and the middle neurons can be updated using the correlation of the presynaptic and postsynaptic spikes by the STDP learning rule. This process clusters similar human images. Furthermore, the V_{Pre} emitted from the input neurons also trigger MoS_2 nanoristors between the middle and output neurons, integrating I_{Post} at the leaky integrators in the output neurons. The corresponding target value determined by a specific person’s label to classify a human’s face image is given for each training process as follows: the corresponding target value is loaded to the lower V_{th} at the comparator of the corresponding target output neuron and into the higher V_{th} at the other output neurons. Then, the target output neuron with the low V_{th} and

other output neurons with the high V_{th} emit the V_{pot} for the potentiation process and the V_{dep} for the depression process into MoS_2 nanoristors between the middle and the output neurons, respectively. If an output neuron generates a V_{post}, it also sends inhibitory signals to other neurons in the output layer in order to prevent the other neurons from firing during the refractory time. This lateral inhibition enables to prevent all neurons from learning in a similar image. It also promotes competitive learning that corresponds to a winner-takes-all mechanism.

The delayed timing of the presynaptic spike (t_{pre}) is encoded from 0 to 20 μs proportional to the intensity of the image pixel (Fig. S18(b)). In the input neuron, a specific voltage can be applied to MoS_2 nanoristors through the CMOS inverter. The V_{dd} of PMOS in the CMOS inverter corresponds to a reading voltage (V_{Read}) of -0.1 V, while V_{ss} of NMOS corresponds to the V_{post} emitted by the following neuron. The applied voltage to MoS_2 nanoristors-based synapse device (V_{syn}) depends on the timing difference ($\Delta t = t_{pre} - t_{pst}$) of the V_{pe} and V_{pst} via CMOS inverter. Hence, the correlation between V_{pre} and V_{post} induces either the potentiation process ($\Delta t > 0$) or the depression process ($\Delta t < 0$) of MoS_2 nanoristors.

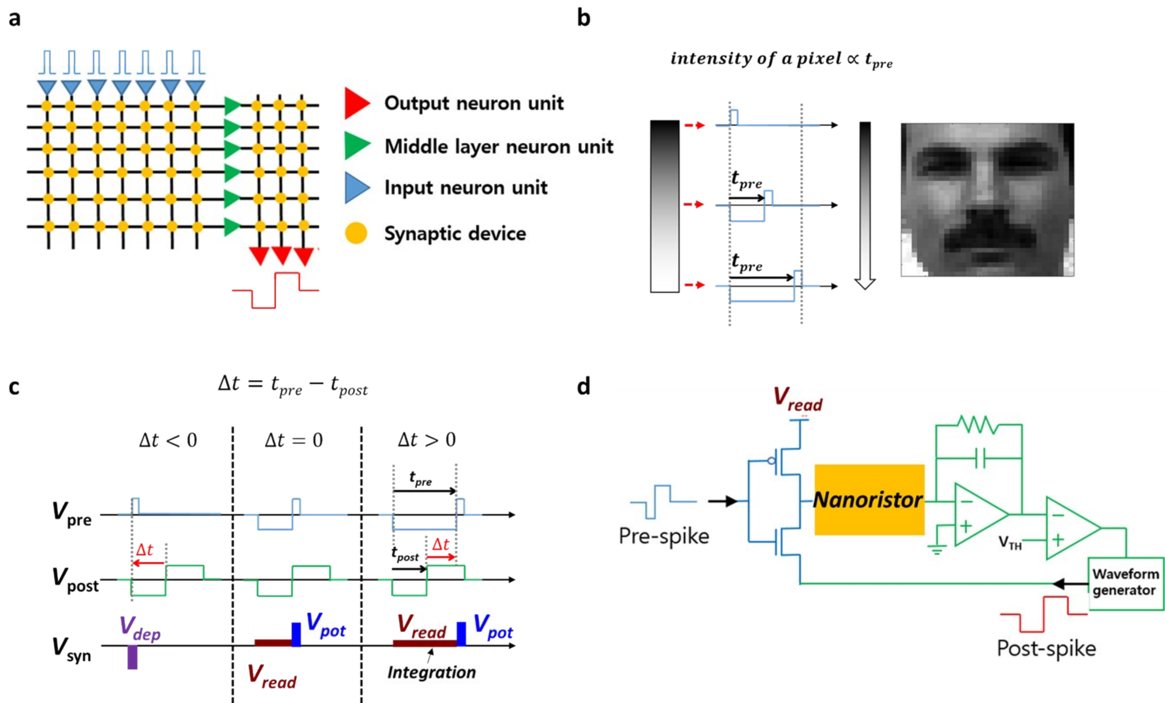

Fig. S18 Device-to-system simulation for the face classification. (a) Two-crossbar array architecture for two-perceptron ANN. (b) The timing of the pre-spike encoded by the intensity of the input pixel. (c) The designed overlapping pulse scheme to implement the simplified STDP scheme. (d) Circuit diagram of the neuron circuit.

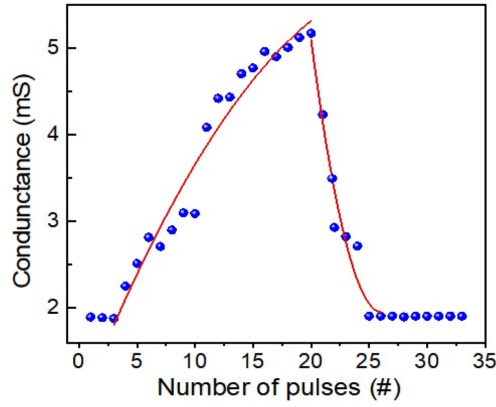

Fig. S19 Synaptic plasticity of MoS_2 nanoristor and its fitting curve

In the device-to-system simulation, we mathematically modeled the conductance modulation of MoS_2 nanoristors as a function of the number of pulses to update the synaptic weights according to the experimentally measured synaptic plasticity of MoS_2 nanoristors shown in Figure 5a (Figure S13). The conductance modulation (ΔG) results from the simplified STDP model, indicating that ΔG relies only on the present conductance (G_{present}). The following equation can be derived from the fitted curve using experimental data:

$$\Delta G = \left[\left(G_{HGS_p}{}^{a_p} - G_{LGS_p}{}^{a_p}\right) \cdot \left\{\left(G_{present} \cdot 10^{3 \cdot a_p} - G_{LGS_p}{}^{a_p}\right) / \left(G_{HGS_p}{}^{a_p} - G_{LGS_p}{}^{a_p}\right) + 1/19\right\} + G_{LGS_p}{}^{a_p}\right] \ldots G_{present}$$

(in potentiation)

$$\Delta G = \left[\left(G_{HGS_d}{}^{a_d} - G_{LGS_d}{}^{a_d}\right) \cdot \left\{\left(G_{present} \cdot 10^{3 \cdot a_d} - G_{LGS_d}{}^{a_d}\right) / \left(G_{HGS_d}{}^{a_d} - G_{LGS_d}{}^{a_d}\right) - 1/19 \ldots G_{present}\right.\right.$$

(in depression)

where G_{HGSp} is the highest conductance state in the potentiation, G_{LGSp} is the lowest conductance state in the potentiation, G_{present} is the present conductance state, a_{p} is the degree of deflection of the fitted curve from the measured data in the potentiation, and G_{LRSd},

G_{HRSd}, a_d are applied to the case of depression. Table S2 provides the parameters used in this device-to-system simulation.

Table S2. Summarized fitting parameters.

	G_{LGSp}	G_{HGSp}	a_p	G_{LRSd}	G_{HRSd}	a_d
value	517	191	1.2	517	191	-4.8

To simulate the leaky integrator, the integrated I_{post} was modeled using the following equation:

$$\tau \frac{dX}{dt} + X = I_{Post},$$

where the state variable (X) is the output voltage of the integrator, and τ is a leak-time constant (= 100 μs).

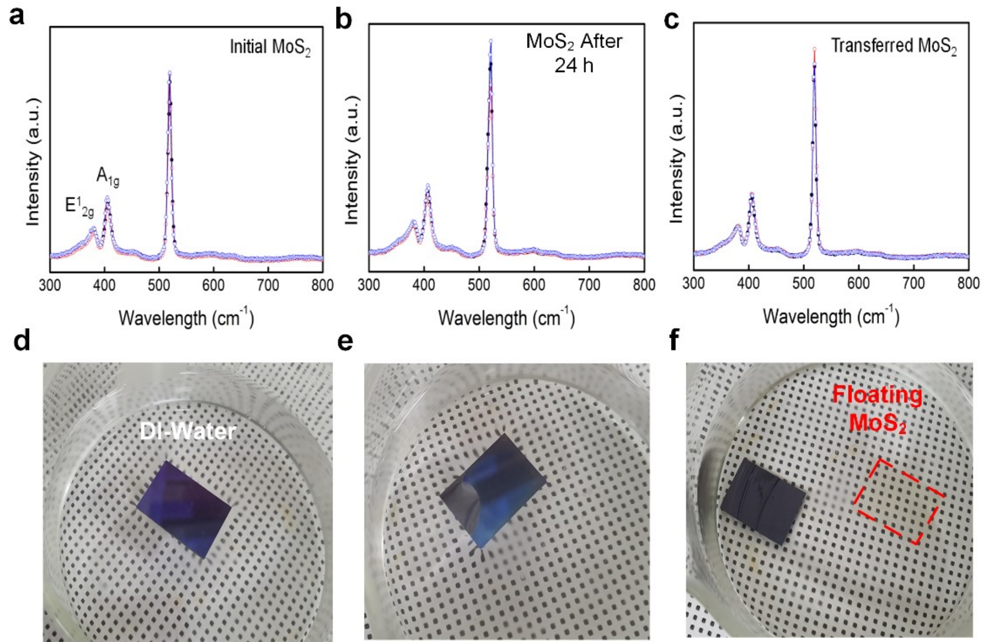

Fig. S20 (a) initial MoS_2 layer, (b) MoS_2 layer aged for 24 hours, and (c) transferred MoS_2 layer onto SiO_2/Si wafer. Images of MoS_2 layer transfer process which show (d) dipping the MoS_2/SiO_2/Si sample in the DI-water, (e) separated MoS_2 layer from SiO_2/Si wafer, and (f) floating MoS_2 layer.

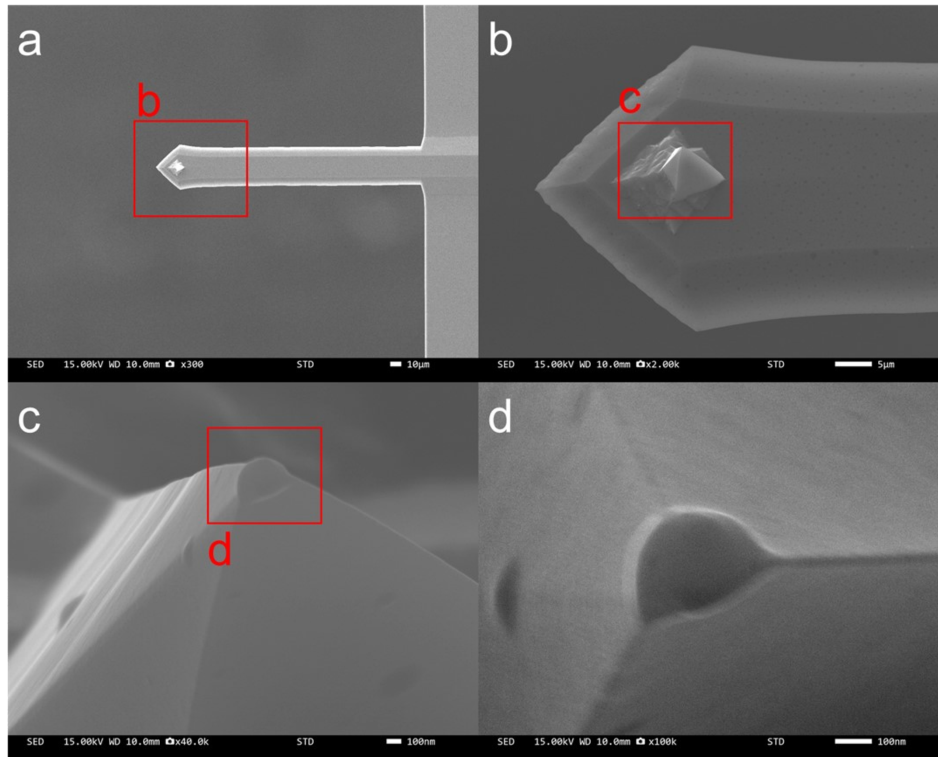

Fig. S21 SEM images of the cantilever tip used in CAFM measurement with a magnification of (a) × 300, (a) × 2,000, (a) × 40,000, and (a) × 100,000.

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