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The dopant (n- and p-type), band gap, size, stress-dependent field electron emission induced from silicon nanowires

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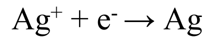
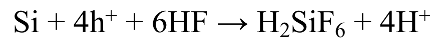
1.1 Detailed process and machnism of synthesis of SiNWs

Various methods have been advanced to synthesize Si nanostructures in a top-down or bottom-up approach[1-3]. Among them, catalyst-induced etching (CIE) is wet-chemical method, which is a particularly fascinating and promising approach, because of its good cost-efficiency, economical, and ease for massive production. Various Si nanostructures including Si nanowires (SiNWs), porous SiNWs, Si nanopores, have been successfully synthesized through CIE method, with their size and morphological features well controlled[4]. Tremendous efforts have been devoted to realization of various Si nanostructures for various applications such as, energy storage, harvesting, optoelectronics, and sensors. In addition, Si nanostructures have been used for electron field emission applications. For example, Jihun Oh et al. [5] studied $SiNW_S$ with 18.2%-efficient silicon solar cells achieved through control of carrier recombination. Keying Guo et al. [6] investigated the biosensor using porous Si NSs. Song et al. [7] fabricated the one-dimensional Si Ns for Li-ion batteries and observed that the one-dim. NSs have many advantages because geometry accommodates the large volume change of the Si during cycling and enables facile electron transport during all stages of operation. Various efforts have been made on novel strategies for enhancing the performances of various devices based on such SiNWs. In particular, SiNWs synthesized by CIE gives unique advantage in terms of fabrication of advanced devices at a low cost. Therefore, depth understanding on the CIE approach could be helpful to understand the advanced realization of Si nanostructure-based high-performance devices. The CIE approaches have been categorized in two-way, 1- one step CIE and 2- two step CIE approach. One-step chemical dissolution process in an aqueous HF solution containing the metal salt in this method. The etching process is a direct process which involves the immersion of substrates in an etchant solution of $AgNO_3$/HF. The SiNWs can be fabricated on large areas, which can cover the whole Si wafer. On the other hand, the two-step process gained an

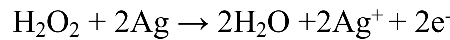
increasing interest in the last years due to its simplicity and the high crystalline quality of the obtained SiNWs, resulting from etching of the single crystalline Si material. SiNWs with lengths ranging from a few micrometers to several tens of micrometers can be obtained using either a two-step process. The detailed mechanism of the two step CIE approach discussed here. The two-step CIE method is adopted to grow Si nanostructures, the second step involves the synthesis of Si nanostructures through immersing in $AgNO_3$/HF for a few minutes and further it is followed by electroless etching in solution. The chemical reactions involved in fabrication of Si nanostructures during CIE approach are[1,2,3]



$$Ag^+ + e^- \rightarrow Ag$$



$$Si + 4h^+ + 6HF \rightarrow H_2SiF_6 + 4H^+$$



$$H_2O_2 + 2Ag \rightarrow 2H_2O + 2Ag^+ + 2e^-$$

The mechanism of CIE depends on the creation and transport of electron and holes, which can be obtained by redox reaction that occurred at interface of silver nanoparticles(AgNPs) and electrolyte solution. In this approach the Si wafers are etched in the presence of HF and H_2O_2 which acts as oxidizing agents. There is ejection of electrons from Si wafer which create hole. When AgNPs accepts electron from Si wafer, they behave as seed nuclei which turned into nano-porous structure. Since the procedure involves various steps: (a) elimination of the oxide layer from Si with HF solution, (b) deposition of AgNPs, (c) etching of the manufactured sample and then immersed in HNO_3 to remove residual AgNPs from beneath, and (d) finally leaving Si nanostructures. Here, the galvanic displacement of Si by Ag+ throughout Ag+ leads to Ag reduction on Si surface establishing many local electrochemical cells in which AgNPs act as active cathode and Si surface act as active anode. Through this approach the Si nanostructures can be fabricated on large areas, which control the length and diameter. It is thus important to investigate the impact of length, diameter and hence ratio of length to diameter i.e aspect ratio on an electron field emissions properties of Si nanostructures.

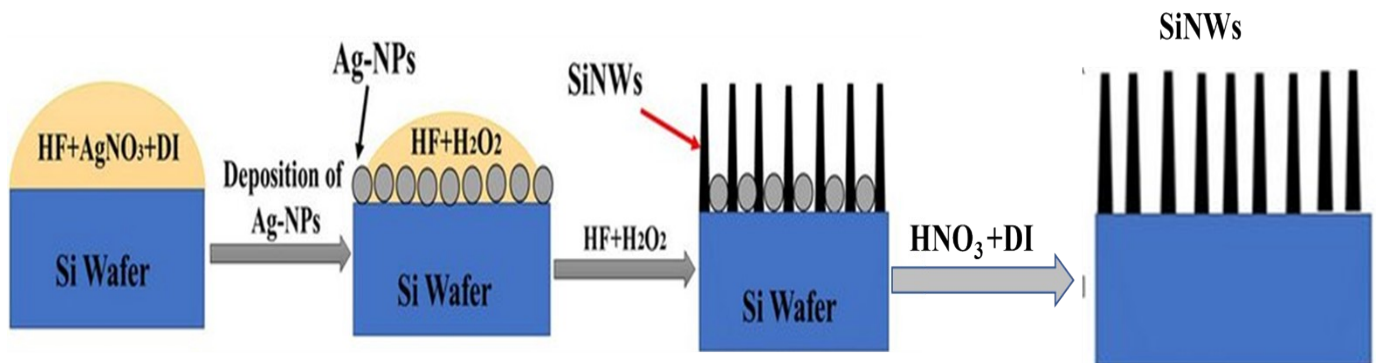


Fig. S1 Schematic diagram of the SiNWs fabrication process by using CIE technique

2.0 Results and discussion

2.1 Microstructural analysis

Fig.2(d-e) shows the XRD spectra, recorded by using Cu (Kα) radiation (λ = 0.154nm) of SiNWs. The peaks assigned to Si phase for reflection planes (004) were observed at 2θ=68.89° , 69.04° , 68.93° and 69.15° assigned the plane (400) for samples n_{30}, n_{50}, p_{30} and p_{50}, respectively. No extra peaks related to any impurities were observed within the detection limit of the instrument, which confirms that the as-synthesized products are pure SiNWs. The FWHM values has been estimated using Gaussian fit, which is summarized in Table S1 for all samples respectively. Estimated values of lattice constant of SiNWs for all samples is summarized in Table S1. The average crystalline size, micro strain (ε) and dislocation density(δ), lattice stress present in the sample, were estimated by the Scherrer formula using XRD patterns [8-9].

$$D = \frac{k\,\lambda}{\beta \cos\theta} \quad \text{and} \quad \varepsilon = \frac{\beta_{hkl}}{4 \tan\theta}$$

$$\delta = \left(\frac{\beta \cos\theta}{k\,\lambda}\right)^2 = \frac{1}{D^2} \quad \text{and} \quad \sigma = Y\frac{a - a_0}{2a_0\gamma}$$

Here β is the full-width at half maximum (FWHM), D is crystalline size, k is shape factor $\gamma = 0.28$, Y= 160GPa, a_0 =0.5410 nm is lattice constant of bulk Si and a is lattice constant of SiNWs. Average crystalline size(D), micro strain (ε) and dislocation density(δ), lattice stress of SiNWs are summarized in Table S1. The calculate values of macrostrain for all samples are positive, indicates the tensile strain in SiNWs lattice. The both n-type and p-type samples with etching time of 50 minutes shows the maximum strain, which is related to various factor including impurity/defect emergence, lattice constant, mismatch, and the thermal extinction coefficient between the Si substrate and grown SiNWs. In addition, the calculated values of internal stress of SiNWs are summarized in Table S1. Lattice Constant of a SiNWs describes the spacing of the atoms in the crystal of that material. Here p-type exhibited higher lattice constant than n-type SiNWs, interspacing is larger for p-type than n-type SiNWs, as clearly seen in Fig. 7(in main file). According to the sign of the positive (negative) values of the stress σ, the NWs samples can have a tensile or compressive strain, dependent on the lattice constant of the SiNWs. The magnitude and sign of internal stresses in SiNWs depend on a number of factors, most of which are associated with the conditions and method of synthesized, as well as with the nature of their growth. Thus, during heteroepitaxial growth, when the NWs and the substrate are different, the appearance of internal stresses is mainly caused by the mismatch of the constants of their crystal lattices.

The mismatch ratio of the SiNWs samples n_{30}, p_{30}, n_{50}, and p_{50} against the Si substrate have been estimated through following expression[10].

$$\text{Lattice mismatch Ratio} = \frac{a_{substrate} - a_{nanowires}}{a_{substrate}} \times 100\%$$

where $a_{substrate}$ and $a_{nanowires}$ are lattice parameter of Si substrate (a = 4.510 Å) [13] and SiNWs, respectively. After the CIE process, n_{30} samples exhibits the lowest mismatch ratio between the substrate and the NWs. It can be observed that sample p_{50} have the maximum mismatch ratio in that order. After the increasing etching time from 30 minute to 50 minutes, the lattice mismatch ratio increased because stress increases. The calculated mismatch ratio were 0.66%, 0.72%, 0.75%, and 0.77% for n_{30}, p_{30}, n_{50}, and p_{50} of SiNWs, respectively. Here it was observed that the lattice mismatch below 1% for all samples because of grown NWs onto Si(100) substrate(which confirm the synthesized NWs onto Si). The lattice mismatch between SiNWs and substrate lead to defect densities. Maximum mismatch observed for p_{50} sample because of higher stress present in this sample. Further it would be interesting to correlate the size, stress, lattice mismatch with different parameters of EFE of grown Si NWs. Moreover, the misfit strain is given as.

$$\text{Misfit strain} = \frac{a_{substrate} - a_{nanowires}}{a_{substrate}}$$

Thus, through the above-mentioned equations, it can be seen that lattice mismatch, misfit strain, and stress are in a directly proportional relationship with each other. Therefore, the stress was increased owing to a increases in the lattice mismatch due to variation in etching time and different dopant. If the lattice constants of samples are different, the mismatching positions of the atoms in the crystal at the boundaries can cause strain, leading to cracks or dislocations that propagate through the Si structure. The lattice mismatch between SiNWs and substrate lead to higher defect densities for p_{50} sample(also confirm from Urbach energy).

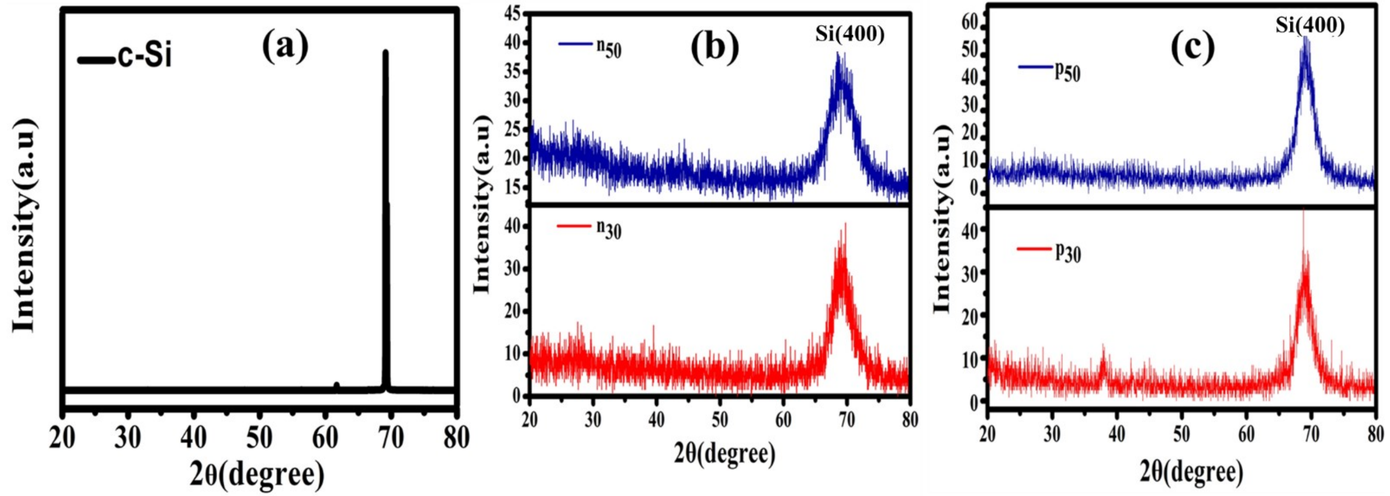


Fig. S2 XRD pattern (a) bulk Si(100), (b) SiNWs grown onto n-type Si(100), (c) SiNWs grown onto p-Si(100)

Table S1 Microstructural parameters of SiNWs

Samples	2^{θ}	FWHM	a(nm)	D(nm)	δ(nm^{-2})	ε	Stress(GPa)	Mismatch (%)
n_{30}	68.89	2.125	0.5446	4.74	0.044508	0.013521	1.901	0.66
p_{30}	68.93	2.341	0.5449	4.30	0.054083	0.014884	2.059	0.72
n_{50}	69.04	2.271	0.5451	4.44	0.050735	0.014407	2.165	0.75
p_{50}	69.15	2.433	0.5452	4.14	0.058377	0.015405	2.218	0.77

2.2 XPS analysis

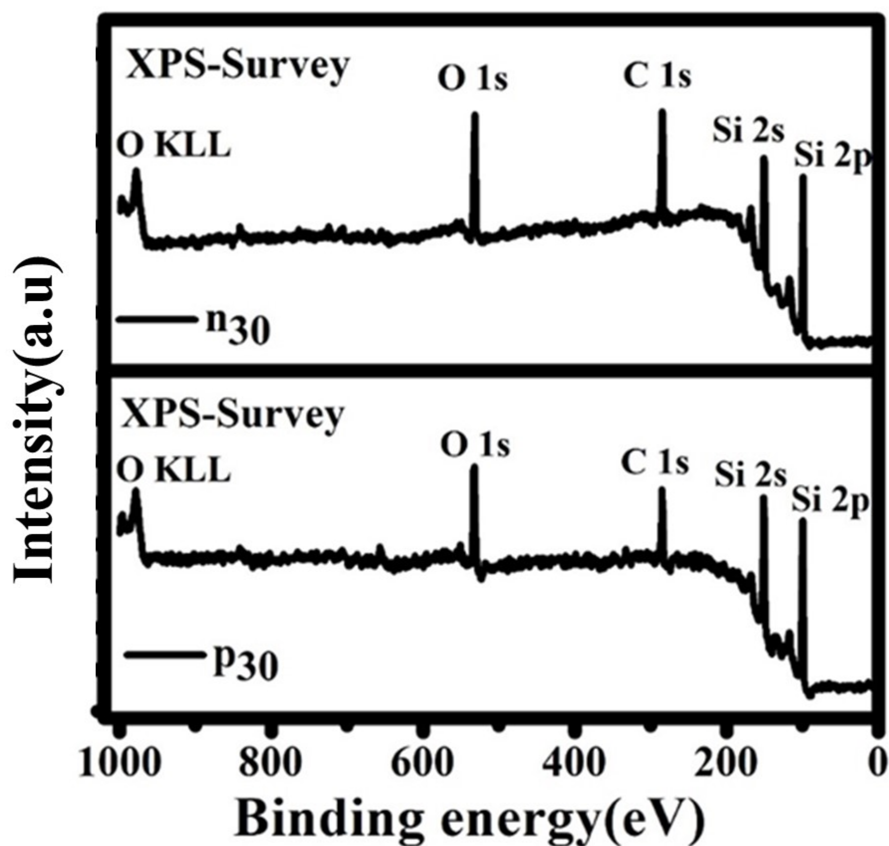


Fig. S3, survey spectra of SiNWs

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