

## Supporting Information

### Enhancing simulation feasibility for multi-layer 2D MoS<sub>2</sub> RRAM devices: reliability performance learnings from passive network model

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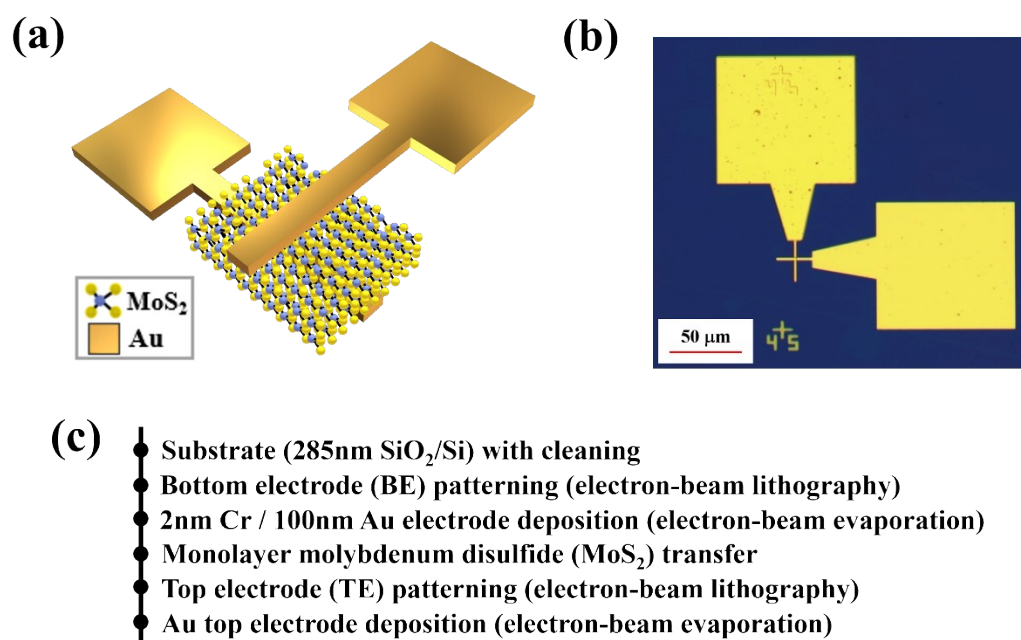
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## Supplementary Figures & Table

### Device structure and fabrication process

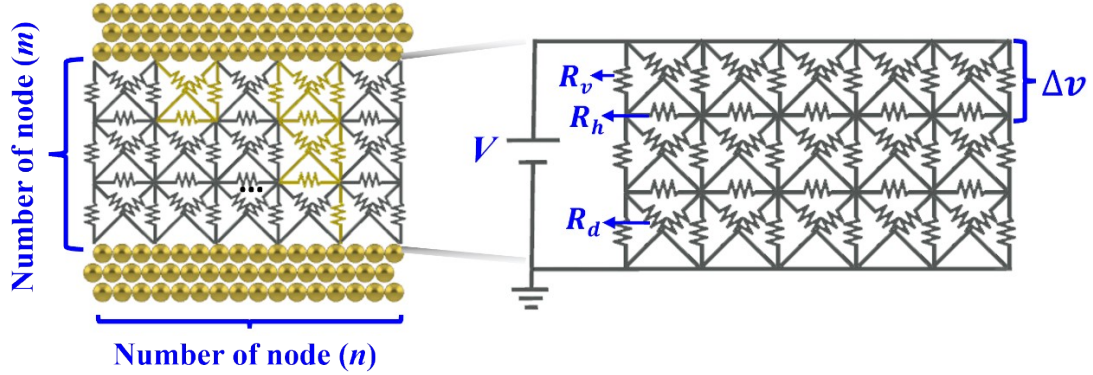


**Figure S1.** (a) A schematic and (b) an optical image depicting a metal-2D material-metal sandwich structure designed for crossbar devices. The scale bar shows 20 μm. The resistive switching layer is composed of monolayer MoS<sub>2</sub><sup>S1</sup>. (c) Workflow for MoS<sub>2</sub>-based non-volatile resistive switching (NVRs) crossbar devices.

Figures S1a and S1b show the schematic and optical images of the MoS<sub>2</sub>-based RRAM devices. The MoS<sub>2</sub> films, synthesized using a sulfurization method, were produced in three different thicknesses by adjusting the Mo precursor thickness. Based on the MoS<sub>2</sub> film thickness, they were categorized as T1, T2, and T3. Atomic Force Microscopy (AFM) cross-sectional height profile analysis confirmed that the thicknesses of T1, T2, and T3 were 1, 1.3, and 2.5 nm, respectively<sup>S1</sup>. This demonstrates that the MoS<sub>2</sub> films varied from a monolayer to tri-layer structure.

The fabrication process, illustrated in Figure S1c, involved growing MoS<sub>2</sub> films on sapphire substrates at 550 °C using a one-step sulfurization process. The grown MoS<sub>2</sub> films were transferred onto SiO<sub>2</sub>/Si substrates with pre-patterned Au bottom electrodes using a water-assisted transfer method. The top electrodes (TE) were patterned and deposited using the same process as the bottom electrodes (BE). The TE were deposited using an e-beam evaporator at three different deposition rates: 0.5 Å/s (low), 1.5 Å/s (medium), and 2.5 Å/s (high).

## Modeling Methodology



**Figure S2.** Schematic of the PNM. The PNM consists of nodes connected by resistors arranged in an  $n \times m$  matrix. Each node is connected to adjacent nodes through vertical resistors  $R_v$ , horizontal resistors  $R_h$ , and diagonal resistors  $R_d$ . When a voltage  $V$  is applied between the TE and BE, the voltage  $\Delta v$  at each node is calculated using Kirchoff's law <sup>S2</sup>.

**Table S1.** Measured Values and Modeling Parameters for PNM Simulation

	Measured		Modeling
$V_{SET}$	1.75 V	$v_{off}$	1.75/m
$V_{RESET}$	-0.82 V	$v_{on}$	-0.82/m
T1 (thickness)	1 nm	m (number of node)	4
T2 (thickness)	1.3 nm	m (number of node)	6
T3 (thickness)	2.5 nm	m (number of node)	10
Low deposition rate (TE deposition rate)	0.5 Å/s	Low defect (Top/Bottom defect)	30%/1%
Medium deposition rate (TE deposition rate)	1.5 Å/s	Medium defect (Top/Bottom defect)	40%/2%
High deposition rate (TE deposition rate)	2.5 Å/s	Medium defect (Top/Bottom defect)	50%/3%
A1 (LRS equation)	-3.25	$R_v, R_h$	$\frac{n * R(V)}{m * 0.414}$
B1 (LRS equation)	4.21	$R_d (= \sqrt{2} R_v)$	$\frac{n * R(V)}{m * 0.414} * \sqrt{2}$
A2 (HRS equation)	7.07E-06		
B2 (HRS equation)	6.53		
C2 (HRS equation)	-6.67		

In this study, parameters were set for passive network modeling (PNM) simulations by considering process parameters such as deposition rates and MoS<sub>2</sub> thickness conditions, as well as threshold voltages and conduction mechanisms derived from DC measurements. Table S1 shows the modeling parameter values based on the measurements of MoS<sub>2</sub>-based RRAM devices. The specific values that transition the state of each individual resistor in PNM are defined as  $V_{on}$  and  $V_{off}$ , and are derived from equation (1) below.

$$v_{off} = \frac{V_{SET}}{m}, v_{on} = \frac{V_{RESET}}{m} \#(1)$$

where  $m$  represents the number of nodes in the vertical direction. This equation is derived under the assumption that each resistance value is uniformly distributed and that the total voltage is equally divided among the nodes. Therefore, the  $V_{SET}$  and  $V_{RESET}$  voltages are divided by the number of nodes  $m$ .

Additionally, PNM can set each individual resistance value based on the conduction mechanisms of HRS and LRS derived from DC measurements. Assuming that each resistance is uniformly distributed, the vertical resistance  $R_v$  and horizontal resistance  $R_h$  values are the same, and the diagonal resistance  $R_d$  is defined as  $\sqrt{2} \times R_v$  based on its length. By setting isotropic resistance in this way, an equipotential is formed horizontally within the circuit, making the voltage across each individual  $R_h$  small. As a result,  $R_h$  does not transition from the initial HRU state to the LRU state, and its role in the actual current flow becomes negligible. Therefore, when the  $R_h$  component is not considered, the output angle  $R_{total}$  according to the input value  $R_v$  can be set as follows:

$$R_{total} = \frac{m(R_d || R_d || R_v)}{n} = \frac{m(\sqrt{2}R_v || \sqrt{2}R_v || R_v)}{n} = \frac{m \times 0.414 \times R_v}{n} \#(2)$$

In the above equation,  $R_{total}$  varies depending on the conduction mechanism. Specifically, in the HRS state, it is expressed as a voltage function for Schottky emission (equations 3 and 4), whereas in the LRS state, it is expressed as a voltage function for Ohmic behavior (equation 5). Using these equations, each individual resistance is defined accordingly <sup>S3</sup>.

$$J \propto A * T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{\frac{qE}{4\pi\epsilon_0\epsilon_r}}\right)}{kT}\right] \#(3)$$

$$R(V) = \frac{V}{A_2 \cdot \exp(B_2 \cdot \sqrt{V} + C_2)} \#(4)$$

$$R(V) = A_1 V + B_1. \#(5)$$

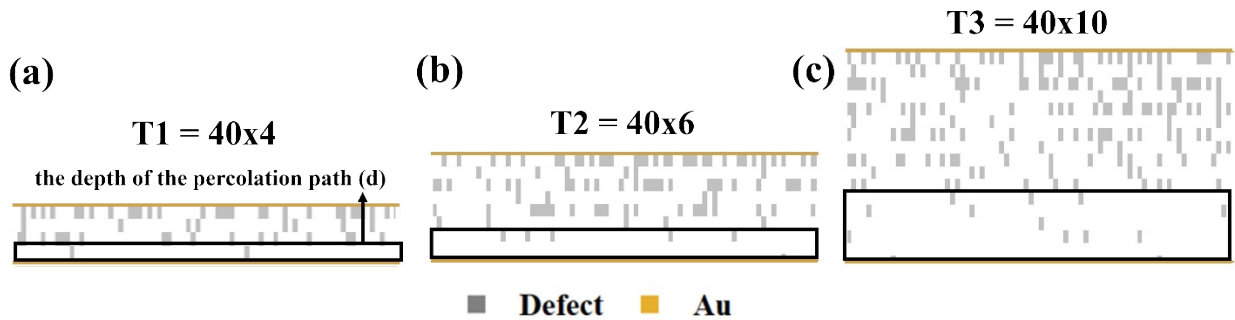
In the PNM model, a 2D mesh with a width  $\times$  thickness of  $40 \times m$  is used as the simulation region. Here, the value of thickness  $m$  varies between 4 and 6, considering the process parameters, and mimics the monolayer to tri-layer of the MoS<sub>2</sub> RRAM device. The process parameters for the TE deposition rate affect the defect occurrence probability. As the deposition rate increases, more defects occur, and thus the defect probability was adjusted to reflect these conditions. The rationale for incorporating the TE deposition rate and defect probability in the PNM model, as detailed in Table 1, is further explained in the model validation section of the main article.

## Model Assumptions

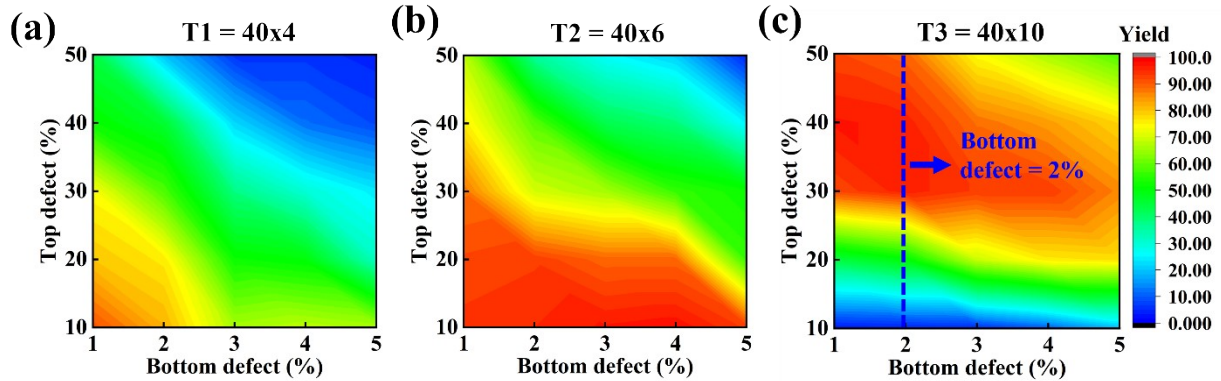
The simulation is conducted based on the following assumptions and rules:

- 1) In PNM, regions with Au ions in sulfur vacancies are modeled as LRU.
- 2) Due to the initial TE deposition process, the probability of LRU occurrence gradually decreases from TE to BE.
- 3) Each individual resistance has its unique resistance value and threshold voltage, and the mean and variance of these parameters are used to model the cycle-to-cycle variation and device-to-device variation of RRAM.
- 4) During the set process, HRU is converted to LRU only when another adjacent LRU is present.
- 5) During the reset process, some individual resistances do not switch due to a certain probability, which can lead to reset failure.

## Model validation and discussion



**Figure S3.** Resistance images for different thicknesses under identical defect probabilities (TE/BE defects = 30%/1%). These images show the resistance states in the pristine condition before voltage is applied. Gray units indicate that the individual resistance is in a low-resistance state, while white units indicate a high-resistance state. Figures (a), (b), and (c) show the simulation results for regions of  $40 \times 4$ ,  $40 \times 6$ , and  $40 \times 10$ , respectively. Despite the ratio of LRUs to the total number of individual resistances being the same, it can be observed that the penetration length for potential filament formation increases with thickness.



**Figure S4.** Simulation results of yield based on variation defect probability for different simulation regions: (a) 40×4, (b) 40×6, and (c) 40×10. It is noted that the yield wouldn't keep increasing when the top defect % decreases. It fits the observation from the experiments, when MoS<sub>2</sub> with good crystallinity and few defect is applied in the device, the yield would be low due to devices that cannot SET initially<sup>S4</sup>.

#### Reference:

- S1. Huang Y, Gu Y, Mohan S, Dolocan A, Ignacio ND, Kutagulla S, Matthews K, Londoño-Calderon A, Chang YF, Chen YC, Warner JH, *Advanced Functional Materials*, 2024, **34**(15), 2214250.
- S2. Robitaille PM, *Progr. Phys.*, 2009, **4**, 3-13.
- S3. Lim EW, Ismail R, *Electronics*, 2015, **4**, 586-613.
- S4. X. Wu, Y. Gu, R. Ge, M. I. Serna, Y. Huang, J. C. Lee and D. Akinwande, *npj 2D Materials and Applications*, 2022, **6**, 31.