

Electronic Supplementary Material

Thermally tunable anti-ambipolar heterojunction devices

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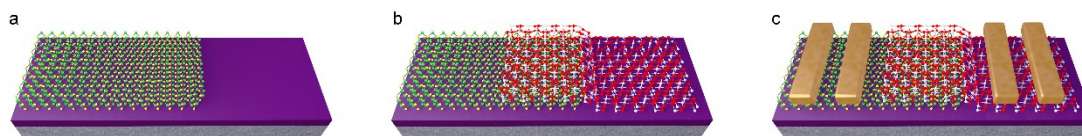


Fig.S1 Preparation process diagram of anti-ambipolar heterojunction devices (a) Transfer few-layers $\text{As}_{0.4}\text{P}_{0.6}$ onto SiO_2 (285 nm)-Si substrate. (b) Transfer few-layers PdSe_2 onto $\text{As}_{0.4}\text{P}_{0.6}$. (c) fabricate Cr/Au electrodes onto the heterojunction.

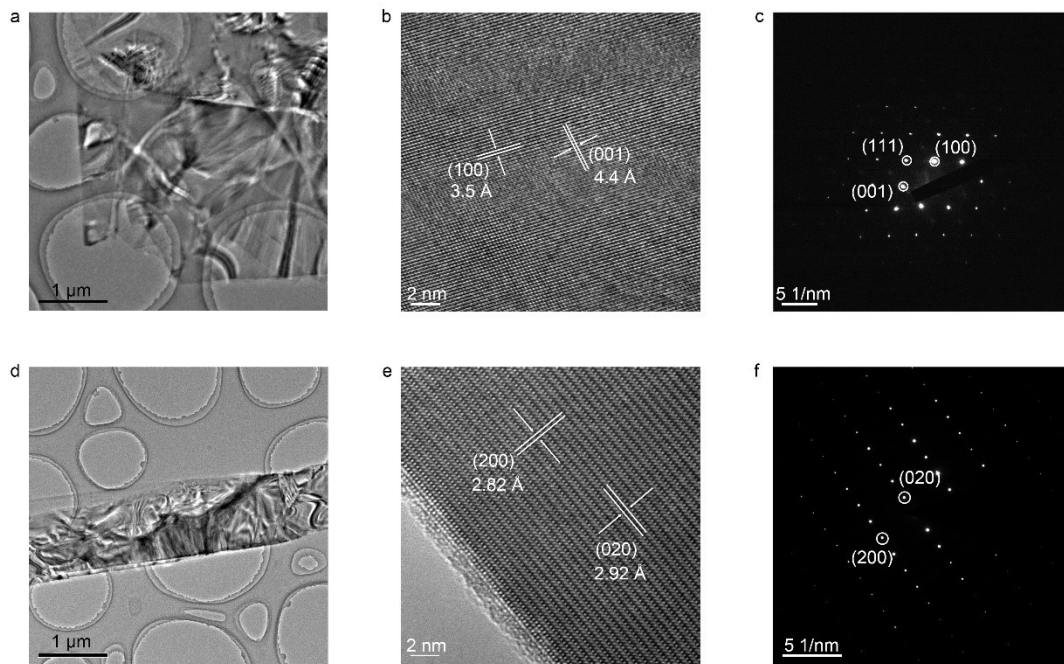


Fig.S2 (a-c) The transmission electron microscopy image of few-layers $\text{As}_{0.4}\text{P}_{0.6}$. (d-f) the transmission electron microscopy image of few-layers PdSe_2

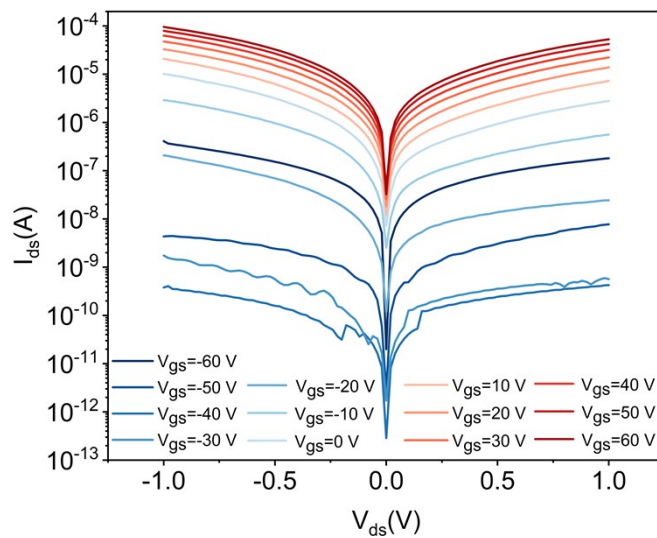


Fig.S3 The output characteristic curve of PdSe_2 at room temperature under different gate voltage (from -60 V- 60 V)

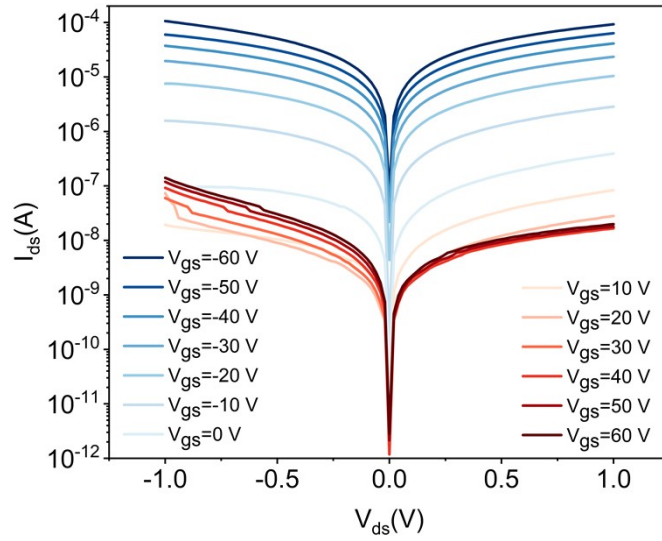


Fig.S4 The output characteristic curve of $\text{As}_{0.4}\text{P}_{0.6}$ at room temperature under different gate voltage (from -60 V- 60 V)

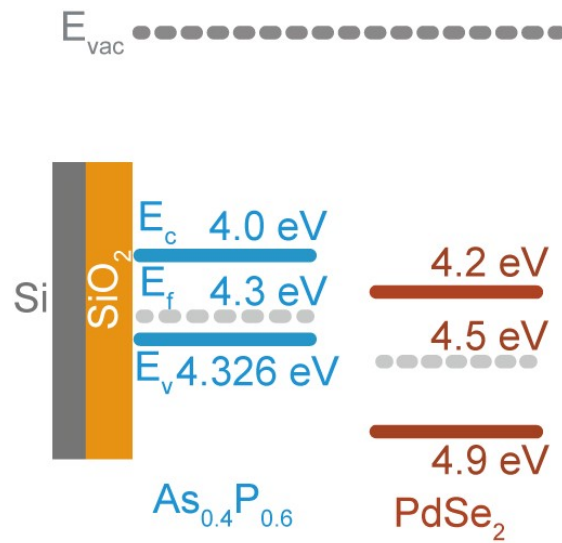


Fig.S5 Band diagram of the $\text{As}_{0.4}\text{P}_{0.6}/\text{PdSe}_2$ heterojunction before contact.