ARTICLE

Phosphorus-based heterojunction tunnel field-effect transistor: from atomic insights to circuit renovations

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Effects of altering BP layers

Changes in the number of BP layers affect the device's performance. As the number of BP layers decreases, the device width alters, the effective mass of electrons increases, the bandgap widens, and both electron mobility and affinity for the TFET's source region decrease, which is expected to exhibit a narrower bandgap (monolayer BP has a 1.53 eV bandgap, 240 % greater than that of 10-layer BP).[1,2] In fact, decreasing layers from 10-layer leads to a diminishment in the current mechanism. Fig. S1(a) shows the transfer characteristics of the DL-HTFET with differing layers of BP in the source region. In the OFF state, the reduction of BP layers leads to a reduction in device width. As a result, the energy band experiences more downward pull due to the boost gate effect on the channel, enhanced electron concentration in the InP layer acts as a source of electrons, and the potential barrier height slightly decreases, which in turn results in higher electron concentration in the OFF-state and accelerated drain current saturation (see Fig. S1(b)). In the ON-state, a higher electron effective mass and lower electron mobility, together with a smaller device width, result in a decrease in drain current as the number of BP layers decreases.

Increasing the number of BP layers reduces electron concentration in the InP layer along with the potential barrier height rise, which results in less electron concentration in OFF-state and less leakage current. The slightly larger value of Φ_{int} leads to less intraband tunneling probability and the dominance of thermionic emission as a more robust current mechanism, which drops SS_{avg} a bit. However, due to less effective mass, higher electron mobility, and wider device width, more ON-state current is observed.

Two key points must be considered in here:

1- More downsizing the device width introduces quantum sizing constraints that are better to solve with fully quantum Schrödinger-Poisson for the device and have analog/RF analysis limitations that are important in this manuscript discussion and 7T SRAM design parameters extraction inability, such as C_{gs} and C_{gd} extraction, device atom numbers issue and fabrication challenges.[3]

2- According to eqn (S1) and Fig. S2, n is the number of layers, which predict E_G for few-layer BP,[4] increasing the number of layers from 10-layer does not increase E_G significantly. Thereby, not a bright boost in the performance is achieved. Moreover, increasing the device width is incompatible with transistor scaling.

$$E_G = 0.39 + \frac{1.62}{n^{1.4}} \quad \text{(S1)}$$

In accordance with the mentioned reasons, we employ all phosphorus-based materials along with applicable dimensions that contribute to a feasible structure that aligns with excellent TFET structural specifications, material requirements, and previous reports.

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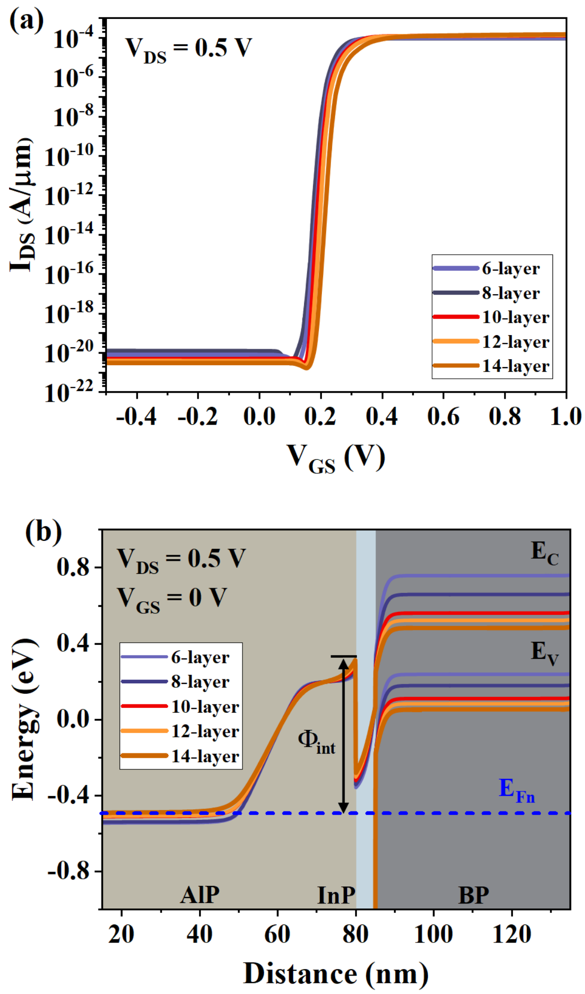


Fig. S1 (a) Transfer characteristics, and (b) energy band diagram of the DL-HTFET with Lpocket = 5 nm for different values of BP layers.

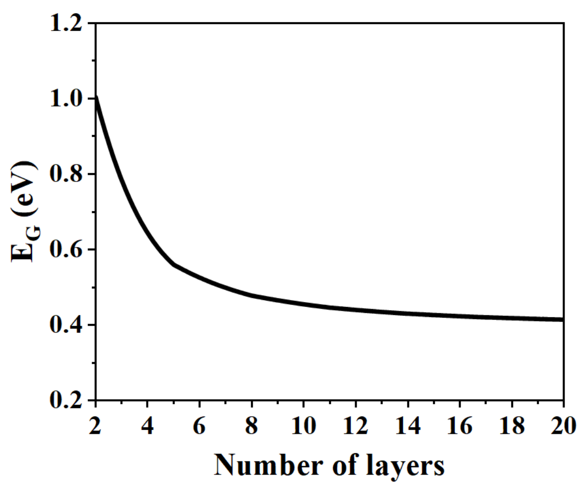


Fig. S2 Variation of the EG with the thickness of few-layer BP.

hybrid methodology

The overall methodology consists of three steps as depict in Fig. S3:

1- Computation of semiconductor materials (10-layer BP, InP, AlP) electrical parameters by employing Quantum Wise ATK (Atomistic Tool Kit), which is a software pack particularly focused on quantum mechanical calculations to simulate materials at the atomic scale, using density functional theory (DFT) method Heyd–Scuseria–Ernzerhof (HSE06) functional, which is a robust method for calculating the band energy in semiconductor materials. Here, the required electrical material parameters relevant to BTBT including: bandgap, electron/hole effective mass, electron/hole mobility, static dielectric constant and affinity are aimed.

2- The device structure geometry is defined and achieved electrical parameters from previous step then utilized as materials parameters in ATLAS by SILVACO device simulator, which solves Poisson's equation self-consistently along with the carrier current continuity equations and is considered the nonlocal band-to-band tunneling model along with other TFET device simulation models. Due to some limitations, analog/RF parameters extraction such as distinct Cgs and Cgd, numbers of proposed device atoms, trap analysis and gate leakage, semi-classical technique is used in this step. It should note the TFET device current mechanism is based on BTBT, and Wentzel–Kramer–Brillouin (WKB) approximation is used. Furthermore, a calibrated must be done between simulation and experimental data of TFET I-V curve, displaying agreement between the physical models employed and experimental data. DC and AC analysis are performed to extract IDS, Cgd and Cgs as functions of VGS and VDS for next step.

3- 2D lookup tables are implemented in a text file and export as ".tbl" file format. Then import ".tbl" file by defining a Verilog-A model into the CADENCE Virtuoso tool, which is software platform for analog, mixed-signal, and RF integrated circuit (IC) design and support Verilog-A language. Here, IDS curve replotted based on VGS sweep at VDS = 0.5 V and behavior of current must be fit with previous step data from SILVACO. It is assumed that the p-type DL-HTFET has symmetric IDS–VGS properties corresponding to its n-channel counterparts. This method provides an easy and accurate way of compact modeling for emerging devices and has been verified against conventional BSIM modeling. Finally, the 7T-SRAM configuration is designed and circuit parameters are extracted using DC and transient analysis.

Output characteristics of the DL-HTFET

Fig. S4(a-d) shows the output characteristics for different gate voltages of the DL-HTFET. The drain current increases with V_{GS} due to boosted tunneling mechanisms and a reduced thermionic barrier. It is important to note that tunneling mechanisms mainly depend on gate voltage, not drain voltage. In fact, the drain voltage affects the thermionic barrier. Therefore, when the drain voltage is increased, the drain current rises until it ultimately saturates. As intraband and interband tunneling reach their maximum values and the thermionic barrier decreases, increasing gate voltage does not influence the drain current, as seen in Fig. S4(c) and (d). However, as the pocket length increases, a nonlinear drain current is observed at lower V_{GS}, which has a higher value for wider pocket length. This behavior is similar to that in MOSFETs, where the role of thermionic emission becomes more pronounced with increased pocket length and a thinner barrier width. Additionally, for $V_{DS} < 0$ V, a negligible increase in drain current is observed, which contributes to the robustness of the device against ambipolarity.

Analysis of Si DL-TFET

Fig. S6 shows the cross-sectional view of the Si DL-TFET, which has exactly the same structural parameters as the proposed DL-HTFET. Fig. S7 depicts the transfer characteristics and gate leakage of the Si device. The ON-state current is 1.15×10^{-6} A μm^{-1} and 1.29×10^{-5} A μm^{-1} at V_{GS} of 0.5 and 1 V, respectively, while the OFF-state current is equal to 7.69×10^{-14} A μm^{-1} for $V_{GS} = 0$ V. The ON-state currents are 108.69 and 9.68 times higher at $V_{GS} = 0.5$ V and 1 V, respectively, and the OFF-state current is 4.75×10^{-8} times lower for the DL-HTFET compared to the Si DL-TFET. The gate leakage current is also 153.8 times greater for the Si DL-TFET, resulting in extreme static power consumption. The Si DL-TFET achieved $SS_{avg} = 47.14$ mV dec^{-1}, which is 824.31% higher than that of the DL-HTFET with a 5 nm pocket length.

According to Fig. S8, under OFF-state conditions, the width of the barrier for tunneling electrons from the valence band maximum to the conduction band minimum is high. As the V_{GS} increases up to 0.5 V, the width of the tunneling barrier decreases, allowing a more significant number of majority carriers to tunnel. In fact, interband tunneling is the primary mechanism of current flow, and based on the WKB approximation, the current is inversely proportional to the width of the tunneling barrier. Hence, the drain current increases as V_{GS} increases and the barrier width decreases. The merit parameters of the Si DL-TFET are provided in Table S1 and compared with those of the proposed DL-HTFET with various pocket lengths and recent TFET works.

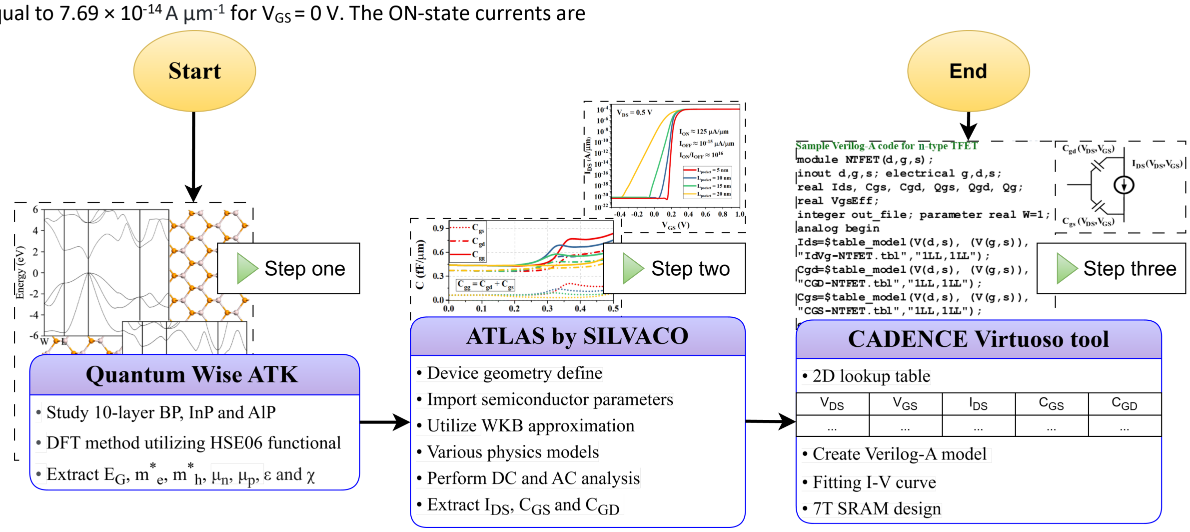


Fig. S3 Flowchart representation of the hybrid methodology.

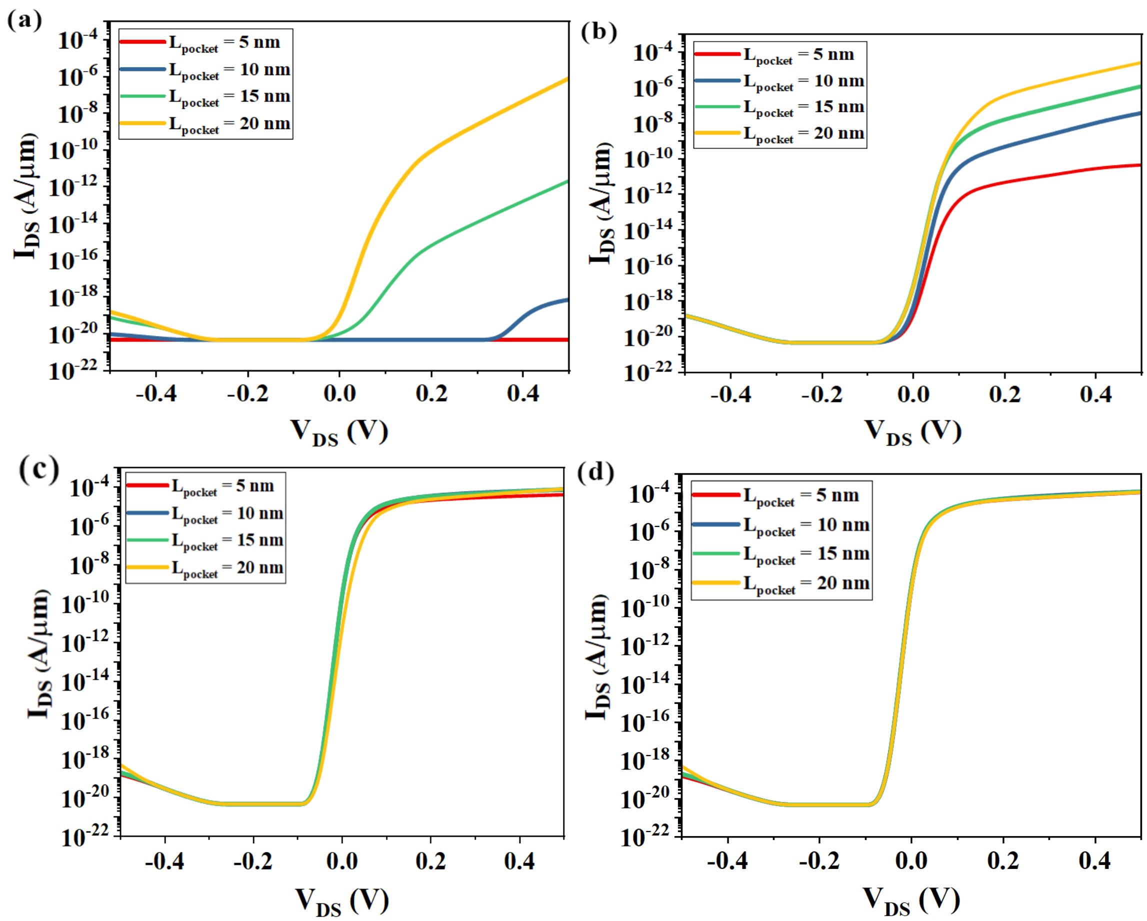
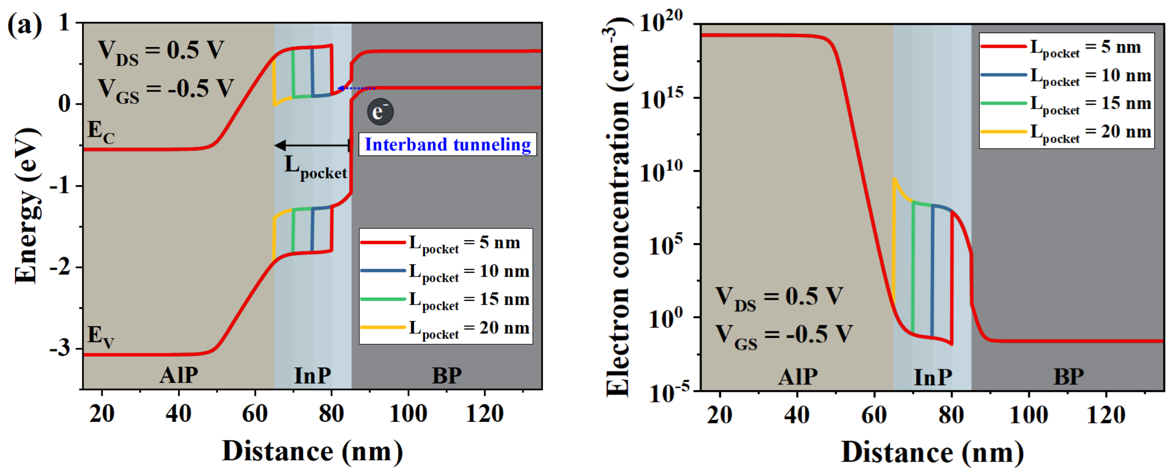


Fig. S4 Output characteristics of the DL-HTFET device at (a) V_{GS} = 0.1 V, (b) V_{GS} = 0.2 V, (c) V_{GS} = 0.3 V, and (d) V_{GS} = 0.4 V along with V_{GS} = 0.5 V which have almost same values and overlay.



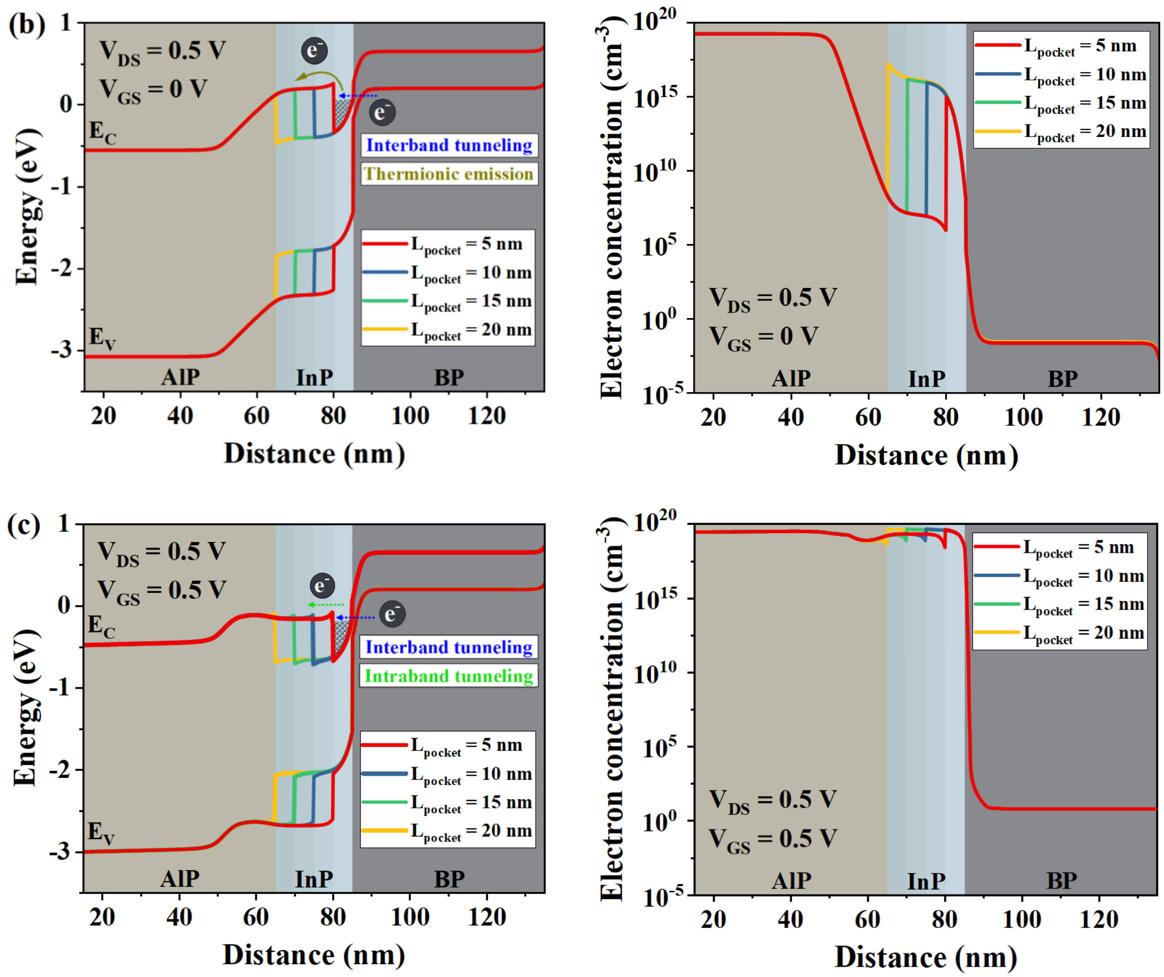


Fig. S5 Energy band diagram and electron concentration, respectively, (a) at V_{GS} = -0.5 V, (b) at V_{GS} = 0 V, and (c) at V_{GS} = 0.5 V taken horizontally across the DL-HTFET at a distance of 1 nm from the semiconductor surface for various pocket lengths.

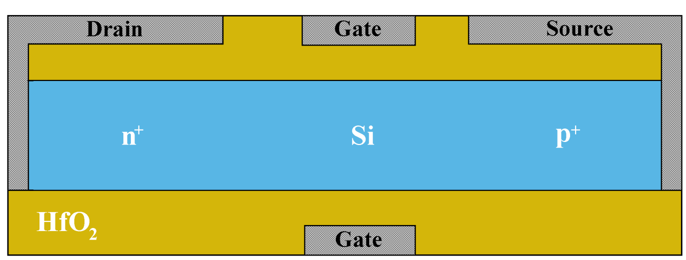


Fig. S6 Cross-section view of the DL-HTFET device.

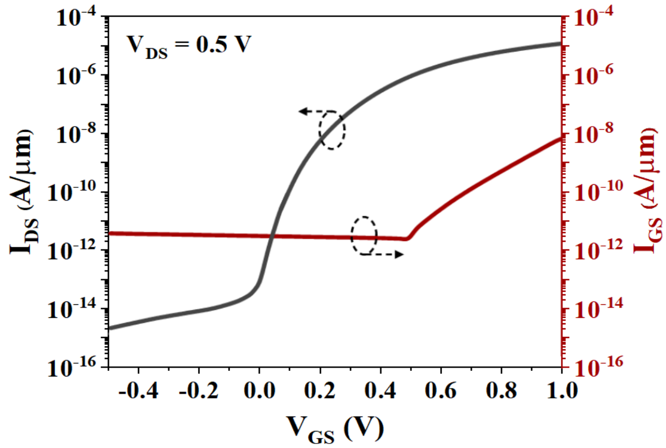


Fig. S7 Transfer characteristics along with gate current leakage of the Si DL-TFET.

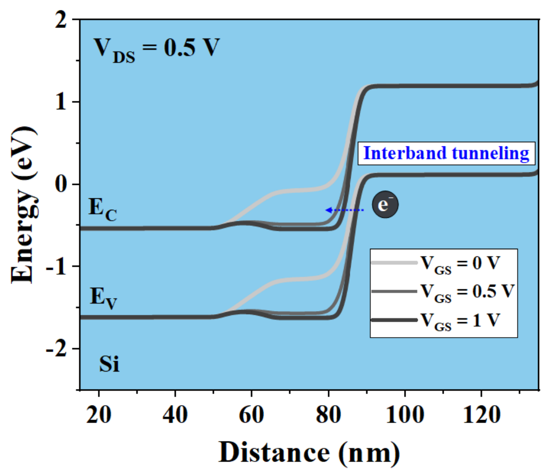


Fig. S8 Energy band diagram taken horizontally across the Si DL-TFET at a distance of 1 nm from the semiconductor surface.

Table S1. Comparison of the performance metrics of the simulated devices along with previous TFET works at V_{DS} = 0.5 V.

Device structure	L_g (nm)	I_{ON} (μA μm^{-1})	I_{ON}/I_{OFF}	SS (mV dec^{-1})	g_m (μS μm^{-1})	f_T (GHz)	GBP (GHz)	TFP (THz V^{-1})
DL-HTFET (L_{pocket} = 5 nm)	20	125	10^{16}	5.10	1470	457	56.18	16.91
DL-HTFET (L_{pocket} = 10 nm)	20	125	10^{16}	11.92	1392	424	51.12	11.97
DL-HTFET (L_{pocket} = 15 nm)	20	125	10^{16}	18.23	1267	399	47.33	9.91
DL-HTFET (L_{pocket} = 20 nm)	20	125	10^{16}	32.21	710	336	28.56	5.81
Si DL-TFET	20	12.9	10^{9}	47.14	33	13	1.42	0.17
MoS_2 TE-TFET[5]	10	4.61	10^{13}	11.6	3	1	0.766	-
CP-ITSM-DLTFET[6]	20	31.8	10^{13}	23.4	370	90	32.3	1.3
JL-SiNT-TFET[7]	20	1.1	10^{10}	20.1	6	242	24.2	-
GaSb/Si V-TFET-WP[8]	25	20.1	10^{11}	26	66	46	7	0.5
GeSn-HJDGTM-VTFET[9]	40	200	10^{12}	12.3	790	-	-	-
$In_{0.75}Ga_{0.25}N$-GEDL-TFET[10]	50	80.2	10^{13}	7.9	339	119	-	-
T-channel GaAs JTFET[11]	70	61.5	10^{11}	18.1	147	32	3.5	0.3

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