Supplementary Information

Supplementary files:

- .stl of the designs:
  - Alignment structure
  - Coverslip with 3 channels and 1 mm walls
  - Coverslip with 3 channels and 500 µm walls
  - Coverslip with 3 channels and 200 µm walls
  - Glass resin imaging window
  - Glass glass imaging window
  - Sacrificial channel with hydrosoluble film
  - Reagent storage with paper pads
  - Reagent storage with hydrosoluble film
  - Valve with PDMS membrane
  - Diode valve with steel ball and O-ring
  - Support for Nafion membrane
  - Chip with microfabricated filter

- Movie file:
  - Movie S1: DIC channel microscopic video of bacteria culture in the glass-glass chip.
  - Movie S2: GFP channel microscopic video of bacteria culture in the glass-glass chip.
  - Movie S3: Time-lapse of the resuspension of inks in the paper pad-based storage chip.
  - Movie S4: Time-lapse of the resuspension of ink in the hydrosoluble film-based storage chip.
  - Movie S5: Time-lapse of the cell capture in the microfabricated filtre chip.

Supplementary Table 1: 3D printing parameters

029J+, DWS Systems		
Parameter	**Value**	**Remarks**
Resin	DS 3000	Transparent, biocompatible
Slice height	50 µm	
Contour numbers	3	Number of laser path at the contour of the object
Hatching (0-400 µm)	70 µm	Distance between two laser paths inside the object
Hatching (400-1000 µm)	50 µm	
Hatching (>1000 µm)	30 µm	
Laser speed (0-400 µm)	180 mm/s	
Laser speed (400-1000 µm)	2800 mm/s	
Laser speed (>1000 µm)	5000 mm/s	
Z compensation	0 µm	Deactivate the automatic compensation of the laser over-penetration for overhanging structures
Indentation	0 µm	The centre of the laser spot is located exactly at the contour of the object (no shift into the object to compensate the laser spot)
Form 3, Formlabs		
Resin	Clear V4	Transparent
Slice height	25 and 50 µm	Only accessible parameter, all the others are fixed

Supplementary Table 2: X-ray tomography values

Chip	**Tube voltage**	**Source current**	**Voxel size**
Coverslip with 3 channels	80 kV	125 µA	10.0 µm
Glass-resin imaging window	80 kV	79 µA	6.6 µm
Glass-glass imaging window	80 kV	80 µA	7.0 µm
Reagent storage with paper pads	60 kV	130 µA	11.5 µm
Valve with PDMS membrane	80 kV	129 µA	8.7 µm
Diode valve	80 kV	129 µA	10.0 µm
Microfabricated filter	80 kV	130 µA	7.5 µm

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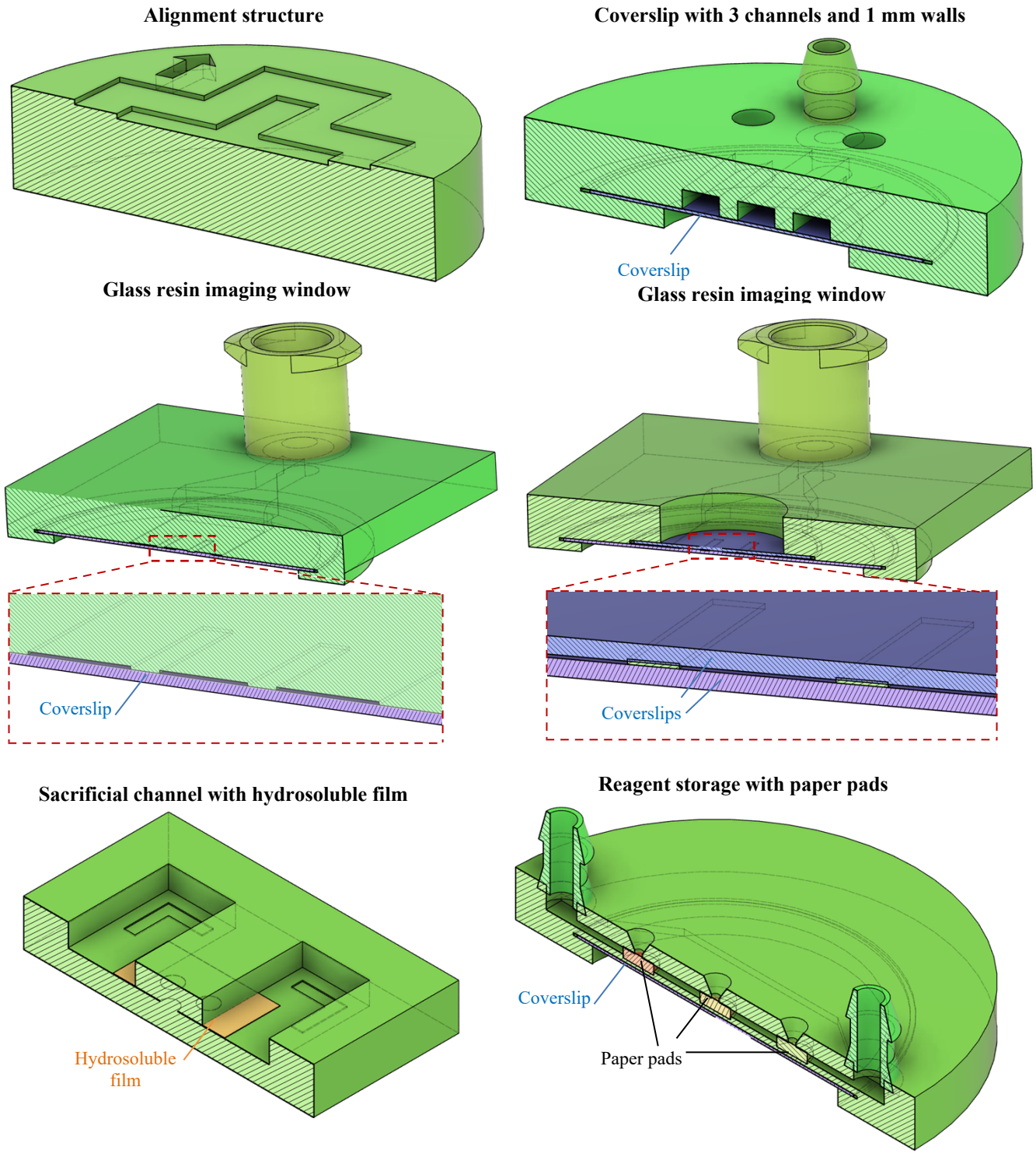

Fig. S1 Cross section images of the designs.

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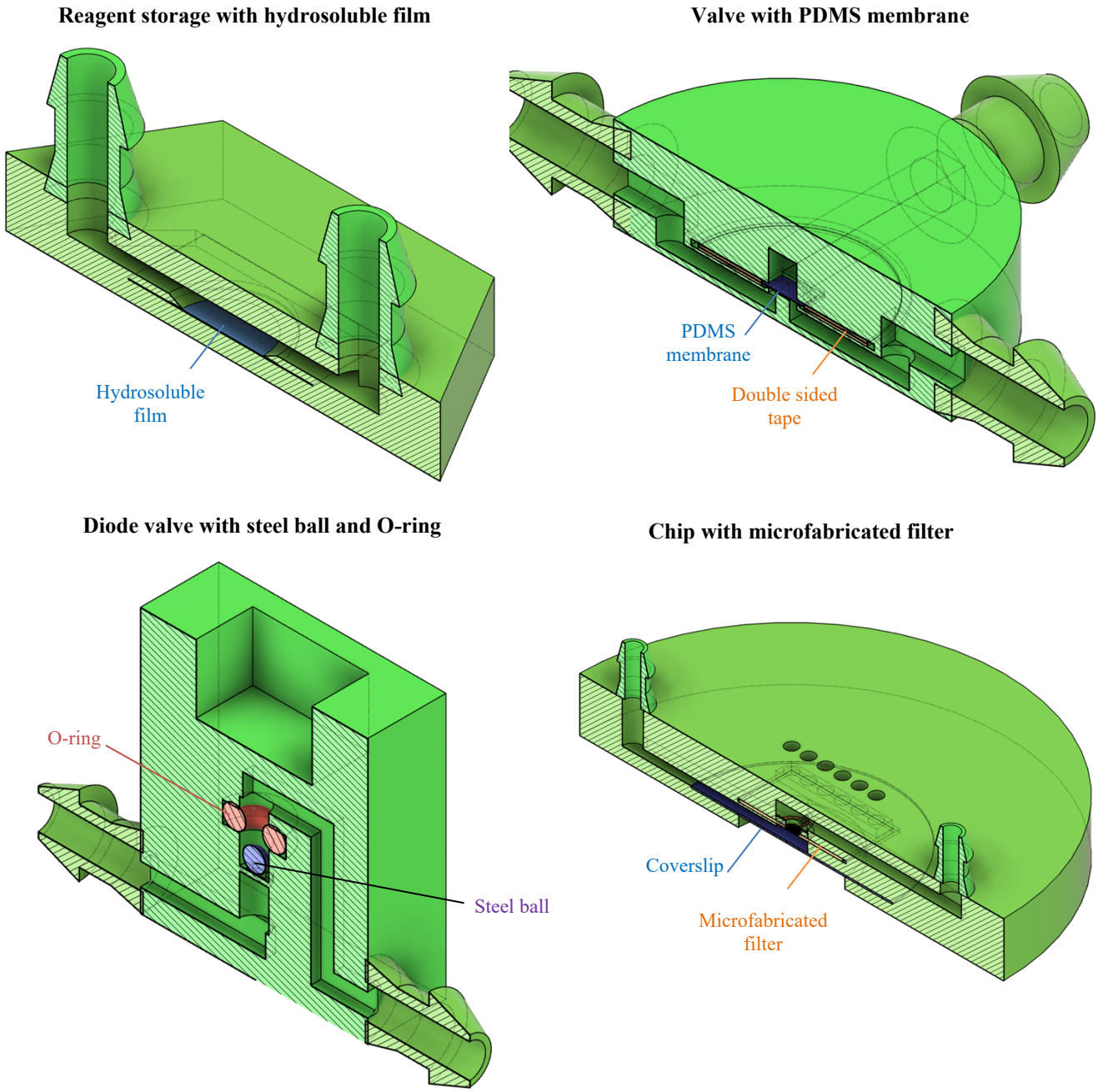

Fig. S2 Cross section images of the designs.

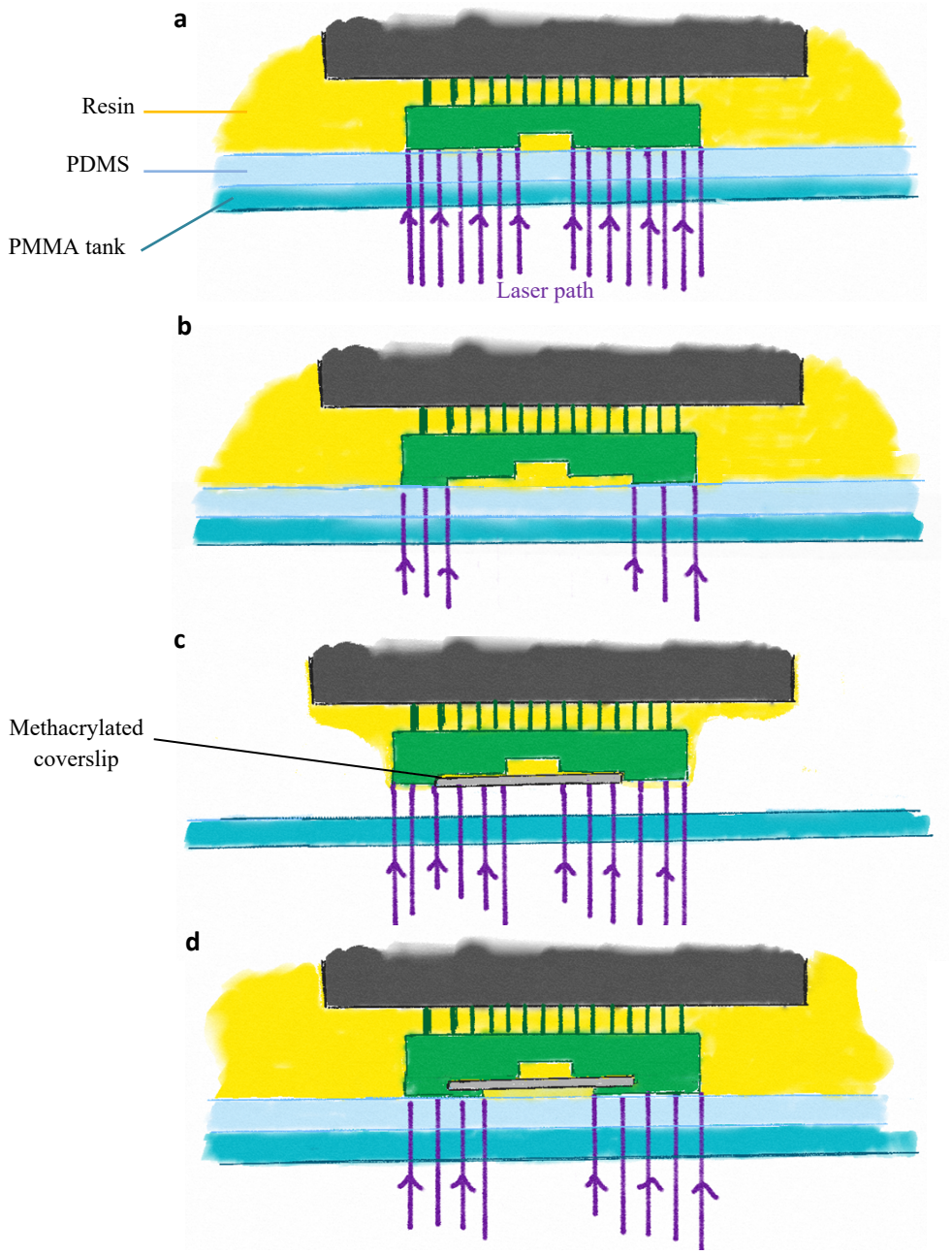

Fig.S3. a) Printing of the pre-pause channel. b) Printing of the slot for the coverslip. c) Partial cleaning of the part, positioning of a methacrylated coverslip, tank change for an empty tank without resin and PDMS (used only to protect the light source from dripping resin drops) and illumination of the liquid resin above the coverslip. d) Tank change to a classical tank with resin and PDMS and printing of the post-pause layers.

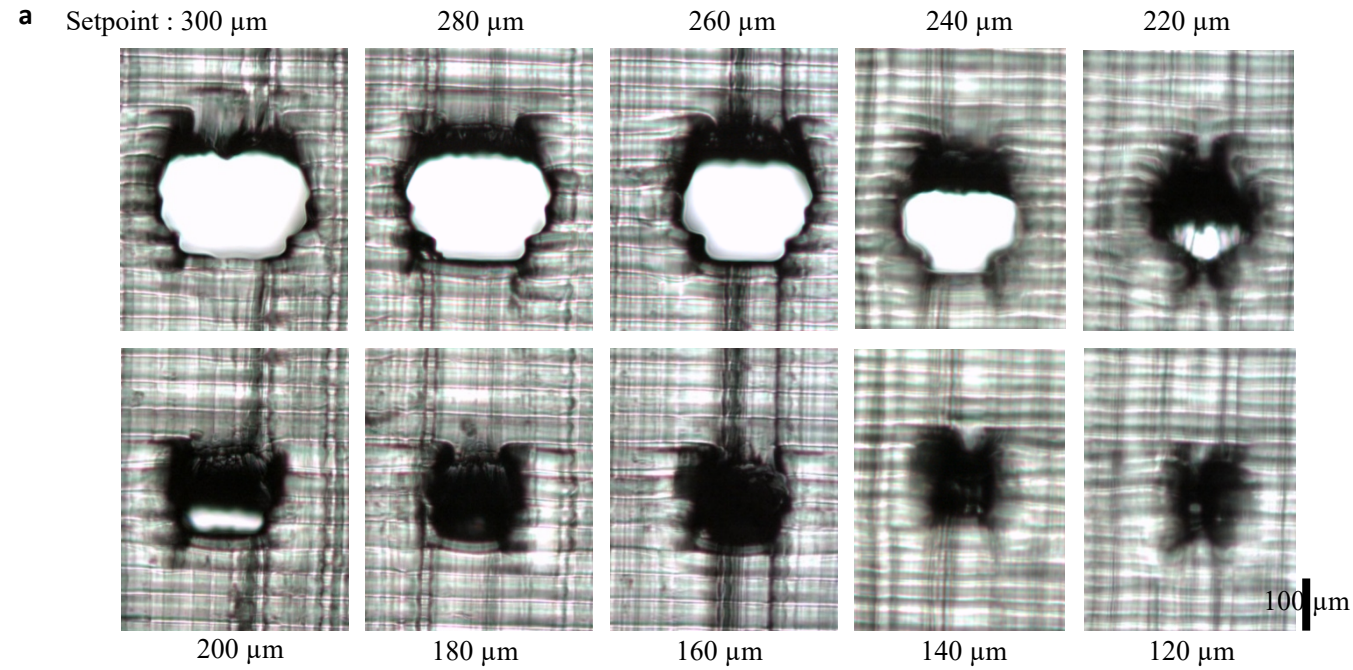

Fig.S4. a) Pictures of horizontal holes (circular section) of different diameters printed using the DS3000 resin and the 029J+ DWS printer. Pictures were made with an Olympus inverted microscope. b) Effective dimensions for the height and width of the holes compared to the setpoints, measured on three different prints. Error bars are standard deviation.

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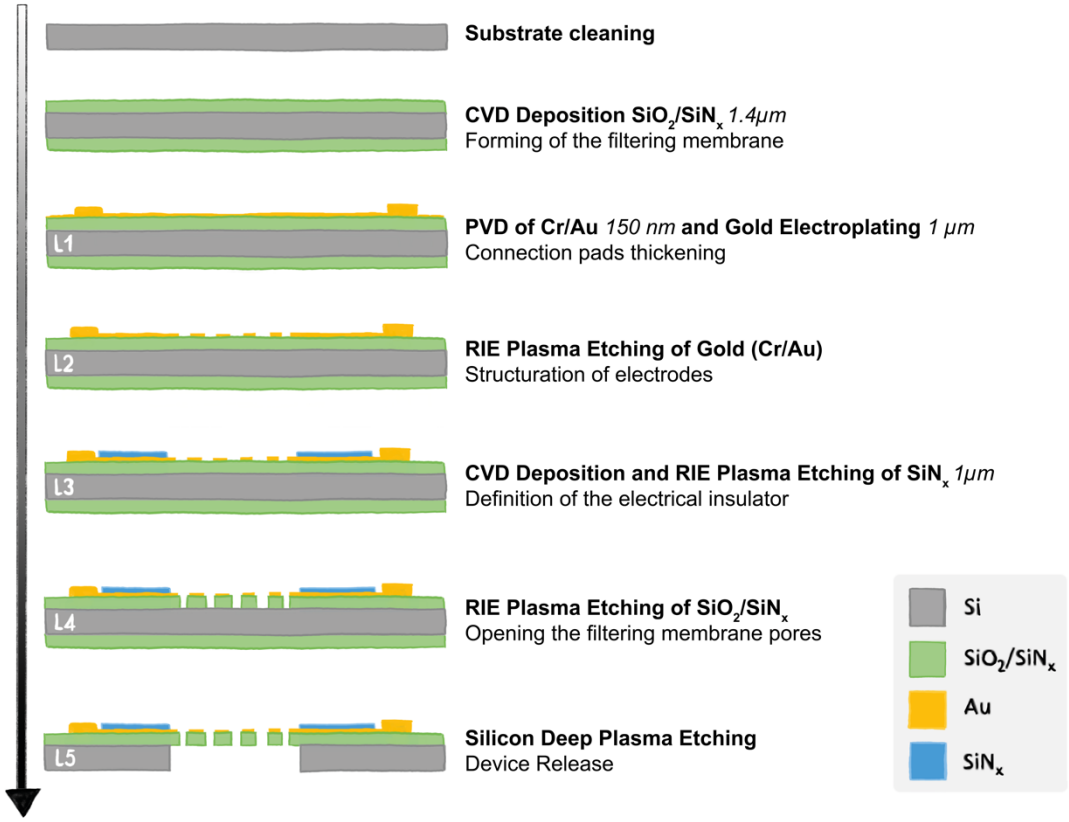
SI document 1: detailed protocol for fabrication of silicon-based filters



Photolithography. Every photolithography step mentioned in the fabrication process uses the AZ15NXT negative resist and lead to a resist thickness of 9 µm. A hexamethyldisilazane (HMDS) deposit is performed on the wafer to ensure the adhesion of the resist on oxidized surfaces. The wafer is coated with a spinning machine (speed: 2000 rpm/min, acceleration: 4000 rpm/min^2, time: 30 seconds). The annealing is done at 110°C for 2 minutes. UV exposure is performed with a dose of 300 mJ/cm^2 in vacuum contact. Post-exposure curing is performed at 120°C for 1 min and the resist is developed in MFCD26 for 15 minutes. Following the pattern transfer step, the resist is stripped from the wafer in NF52 developer heated at 80°C for 5 minutes followed by an O_2 plasma (time: 5 min, power: 400 W, O_2 flow rate: 1000 mL/min) to remove potential resist leftovers.

1. **Substrate cleaning**. A 4-inch silicon wafer is first cleaned in a piranha solution (50% H_2SO_4 + 50% H_2O_2). Deoxidation is then performed in a 5% HF solution.

2. **Chemical vapor deposition**. Thermal oxidation is performed at 1070 °C on the substrate to obtain an 800nm SiO2 layer. A 600nm SiNx film is then deposited at 750°C by LPCVD. These deposits are made on both sides of the wafer at the same time.

3. **Physical Vapor Deposition** followed by **Electroplating of contact pads (L1)**. A seed layer consisting of a bilayer of Chromium and Gold of respectively 50nm and 100nm is deposited by thermal evaporation on the wafer. The previously described photolithography step is performed, followed by the electrolytic growth of 1 µm of gold and the removal of the resist.

4. **RIE Plasma etching of seed layer for electrode definition (L2)**. As previously described, the wafer is spin coated with an AZ15NXT negative resist, exposed to UV and developed. The Cr/Au seed layer of 150 nm is then etched with argon plasma (Ar, 30 cm^3/min) at a sample temperature of 20°C for 3 minutes with a RF power of 100 W and an ICP power of 600 W with a reactor residual pressure of 0,67 mT. This etching step induces gold sputtering over the resist. The resist stripping is therefore done within a NF52 solution for 5 minutes with the wafer placed upside down in an ultrasonic bath followed by the O_2 plasma cleaning step.

5. **CVD Deposition and RIE Plasma etching of Si_3N_4 (L3)**. A 1µm layer of Si_3N_4 is deposited through a PECVD technique on the wafer at 300°C in 10 minutes. The deposition is followed by the photolithography process. Finally, etching of the deposited Si_3N_4 layer is done through RIE plasma etching, using trifluoromethane (CHF_3, 20 cm^3/min), nitrogen (N_2, 10 cm^3/min), argon (Ar, 100 cm^3/min) and dioxygen (O_2, 10 cm^3/min). The process step takes 8 min for etching the 1µm layer at a temperature of 20°C and with a RF power of 35 W and ICP power of 300 W with a reactor residual pressure of 25 mT.

6. **Opening the pores of the filtering membrane (L4)**. Following the photolithography step, RIE etching of the bilayer membrane (SiO_2/SiN_x) is performed using trifluoromethane (CHF_3, 20 cm^3/min) and argon (Ar, 50 cm^3/min) to etch 0.6 µm silicon nitride and 0.8 µm silicon dioxide successively. The plasma etching takes 10 minutes at a sample temperature of 15°C and with a RF power of 90 W to generate the plasma and an ICP power of 300 W with a reactor residual pressure of 7,1 mT.

7. **Etching of the silicon substrate and release of the devices (L5)**. The etching of the silicon substrate is done in two steps. The first step consists of the wafer thinning through plasma etching using an isotropic etching recipe, trimming the wafer from 550 µm to 250 µm (SF_6 at 700 sccm, 20°C, RF Power: 2800 W, BIAS Power: 85 W, time: 37.5 minutes). This step is followed by a light O2 plasma to remove the SF_6 hydrophobic layer before the photolithography step which is performed on the backside of the wafer with a pattern alignment on the front side. A thermal paste is used to bind the wafer to be etched to a second silicon wafer on which the etching will stop, thus avoiding damaging the equipment's chuck while keeping a good thermalization of the exposed resist. The silicon etching process then follows a trip-pulsated Bosch etching process for 40 minutes.

Gas	Flow rate	Time	RF Plasma	LF Polarization
SF_6	700 sccm	3 s	2300 W	85 W
C_4F_8	350 sccm	3.5 s		
O_2	200 sccm	2 s		

A light O_2 plasma allows to remove the SF_6 hydrophobic layer and is followed by both the resist and thermal paste removal within a piranha solution (50% H_2SO_4 + 50% H_2O_2) heated at 120°C for 15 minutes. The devices are then rinsed with DI water and stored.

SI document 2: electrode characterization

Mutliplexer

Following the Print Pause Print integration of the micro-fabricated membranes, a multiplexer shown in figure 1 was designed and fabricated in order to individually route the 6 electrodes pairs to an impedance analyzer (HIOKI IM3570). The multiplexer will act as an intermediary in between the impedance analyzer on one side and the micro-fabricated device on the other, hence its characterization is essential and will be discussed here.

The multiplexer was mounted on top of the 3D printed chip with the contact pins sliding inside in order to take electrical contacts on the micro-fabricated device. The circuit board is perforated with two holes in order to access to the fluidic connector from the top side while the optical access is granted from the bottom this of the printed chip. Finally, the multiplexer is controlled and synchronized to optical imaging through an Arduino Uno board. The multiplexer circuit design is available upon request.

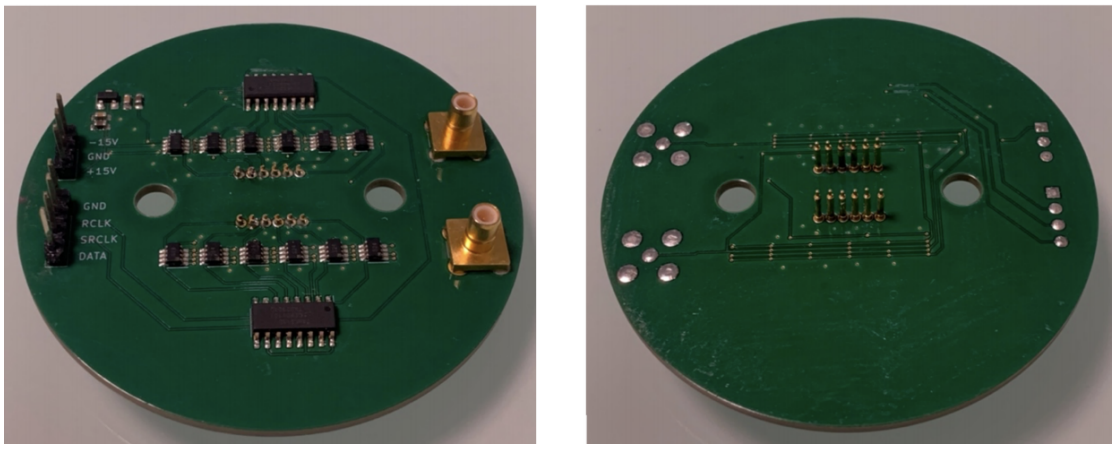


Figure 1: Printed Circuit Board (PCB) of a multiplexer. The top side (a) exhibits the electrical components together with two holes for the fluidic connections to go through, two coaxial connections on the right side, and the data and power pins on the left side. In the center, the 12 spring-loaded pins are going through the PCB on the top side (a) and on the bottom side (b).

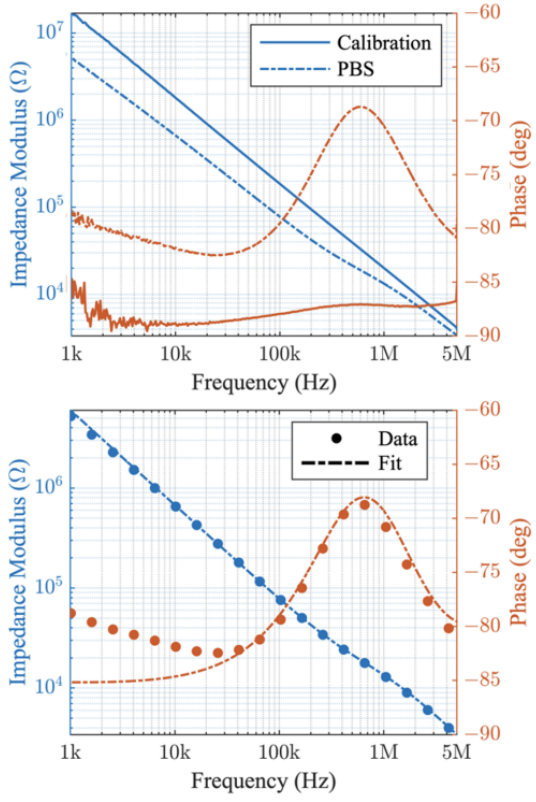
The multiplexer was characterized on its own and showed a total contribution of 250 Ω for each contact pin pair. Moreover, this contribution is stable across the frequency range of interest (1 kHz to 5 MHz) and act as an offset on upcoming impedance spectra.

Micro-fabricated Device

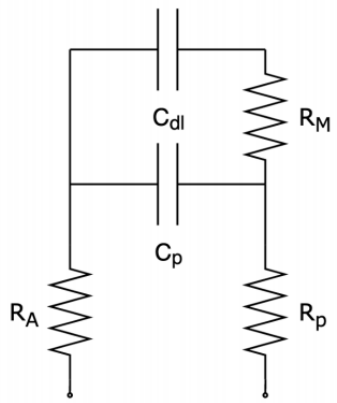
Electrical characterization of the integrated devices is shown in figure 2a through impedance spectra in air ("Calibration") and an electrolytic solution (Phosphate Buffer Saline "PBS"). These spectra are then fitted with an equivalent electrical circuit shown in figure 2b in order to quantify and interpret the physical effects leading to the observed impedance spectra. Here, the resistance R_A takes into account the multiplexer resistance together with the access lines on the micro-fabricated device leading the contact pads to the sensing electrodes on the filtering membrane. $R_P$considers the parasitic resistance brought by the impedance analyzer.R_M and C_{dl} characterize respectively the inter-electrode resistance and the ionic double layer capacitance (reported here as a constant phase element). Finally, C_p represents the capacitive effects induced in-between electrodes and the supporting silicon substrate through the electrically insulating filtering membrane.

Following curve fitting, values of each electrical component can be extracted. We can note that, following this extraction, and based on the impedance spectra, the lower frequencies are dominated by a capacitive behavior which is reflected through the double layer capacitance. Increasing in frequency, a first cut-off frequency is reached at around 200 kHz were the system transitions towards a resistive regime which characterizes the inter-electrode medium through R_M. However, the phase does not reach a fully resistive regime (0°) but plunges back, toward a capacitive regime at a second cut-off frequency of around 1 MHz. However, the region of interest for our application is the resistive regime. Indeed, this resistive regime must be attained in its entirety (the phase is near 0°) and spread over a wide range of frequency in order to study the electrical dispersion of the biological material present in-between the sensing electrodes. Thus, both the double layer and the parasitic capacitances reduce the window of observation in terms of bandwidth and sensitivity, hence, further electrode optimization is required.

Indeed, based on these preliminary characterizations, the geometry of electrodes can be adjusted in order to reduce the double layer capacitance, which would lower the first cut-off frequency. A change in substrate, from silicon to silicon dioxide, a perfect electrical insulator would remove the parasitic capacitance effects, thus spanning the window of observation up to 5 MHz.



(a)



	C_{dl} [$S.s^n$]	C_p	R_M
E1	35.10^{-12}	9.2 pF	29 kΩ
E2	35.10^{-12}	7.5 pF	30 kΩ
E3	35.10^{-12}	9.2 pF	30 kΩ

(b)

Figure 2: (a) Impedance spectra with the modulus in blue and the phase in red of the first electrode pair (E1) in air versus in PBS. (b) shows the equivalent electrical circuit composed of three resistors and two capacitances to describe the experimental data, (a) the fitting results of the electrical model compared to the experimental impedance spectra and table (b) reports the fitting values for each electrode impedance with n=0.92 for the constant phase element.