Supplementary Information for "Universal Skyrmion Logic Gates and Circuits Based on Antiferromagnetically Coupled Skyrmions Without Topological Hall Effect"

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S1. Modified Lindau-Lifshitz-Gilbert Equation of Motion with Spin-Orbit Torque (SOT) Dynamics

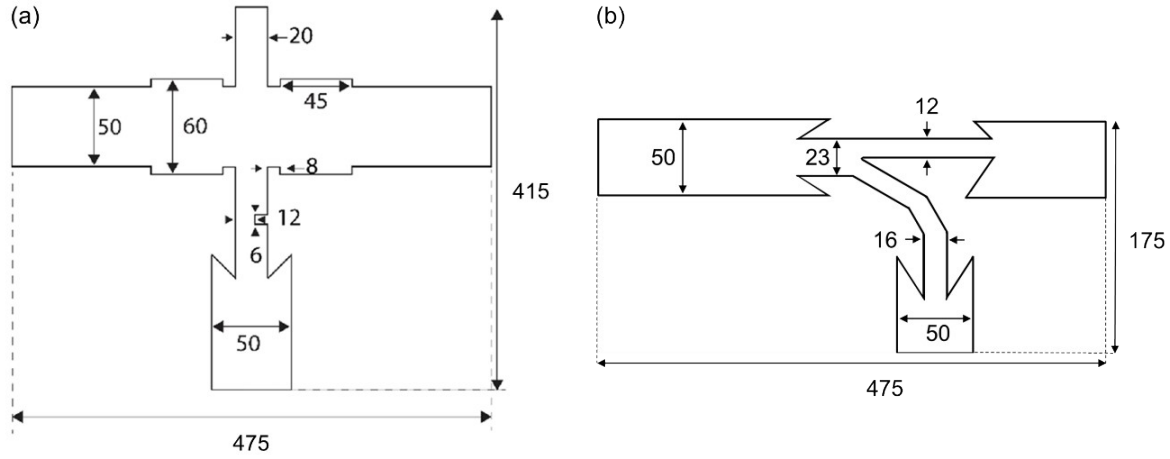
A SOT-driven current in the SAF structure is utilized for dynamic simulations of the SAF skyrmion. The spin Hall angle is tuned to $\theta_{Hall} = +0.25$, and the current pulse was applied adjacent to the ferromagnetic (FM) layers and the spin current (J_s) was applied perpendicular to them such that the SAF skyrmion could travel in the in-plane direction. The LLG equation incorporating the SOT element is then,

$$\frac{\partial \boldsymbol{m}}{\partial t} = -|\gamma|\boldsymbol{m} \times \left(\boldsymbol{H}_{\boldsymbol{eff}} + a_j(\boldsymbol{m} \times \boldsymbol{p}) + b_j\boldsymbol{p}\right) + \alpha \boldsymbol{m} \times \frac{\partial \boldsymbol{m}}{\partial t},$$

where the perfectors a_j and b_j represent the damping-like torque and the field-like torque field strengths, respectively [1]. $\boldsymbol{p}$ is the polarization unit vector in the direction of the magnetic moments that are injected into each ferromagnetic (FM) layer, and it is given by the equation $\boldsymbol{p} = \text{sign}(\theta_{Hall})\, \boldsymbol{j} \times \boldsymbol{n} = -\hat{y}$, where the current direction $\boldsymbol{j} = +\hat{x}$ and the surface normal of the heavy metal layer $\boldsymbol{n} = +\hat{z}$. This vector points in the direction of the magnetic moments that are injected into the FM layer.

S2. Schematic and Dimensions of the Inverter (NOT) and Duplicator Blocks

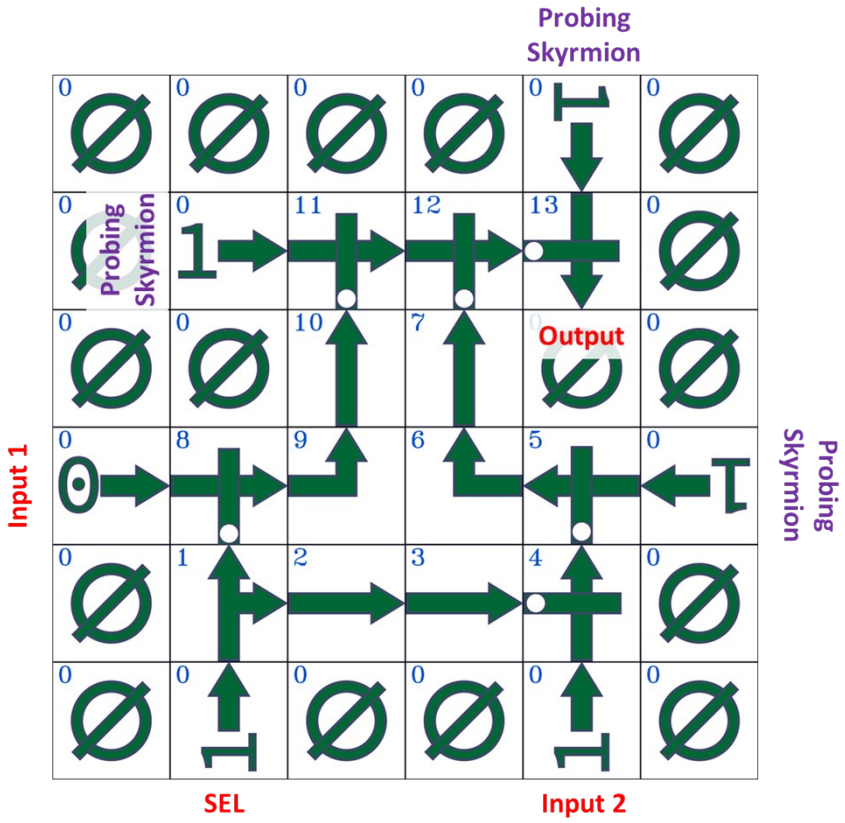
The schematics of the inverter and the duplicator blocks are shown in the figure below. These geometries are imported into the micromagnetic models of a square block geometry (grid size of 600 × 600 × 2) of the SAF multilayer system as images of pixel dimensions 1700 × 1700.



Supplementary Figure S1. Schematics of the simulated logic gate blocks in the SAF multilayers. The dimensions shown for the different parts of the geometries of the inverter block in (a) and the duplicator block in (b) are all in nanometers. Schematic in (a) is adopted from Ref.[2].

S3. MUX logic Circuit Schematic

The schematic shown in Figure S3 represents the MUX circuit constructed from the invertor, duplicator, and transfer blocks. Input 1, 2, and SEL take a single-bit input (1, skyrmion, or 0, no skyrmion). Probing skyrmions are always present during the circuit operation. The numbers on the array of blocks show the order or each block. A video of the timed operation is shown in supplementary video SV11.

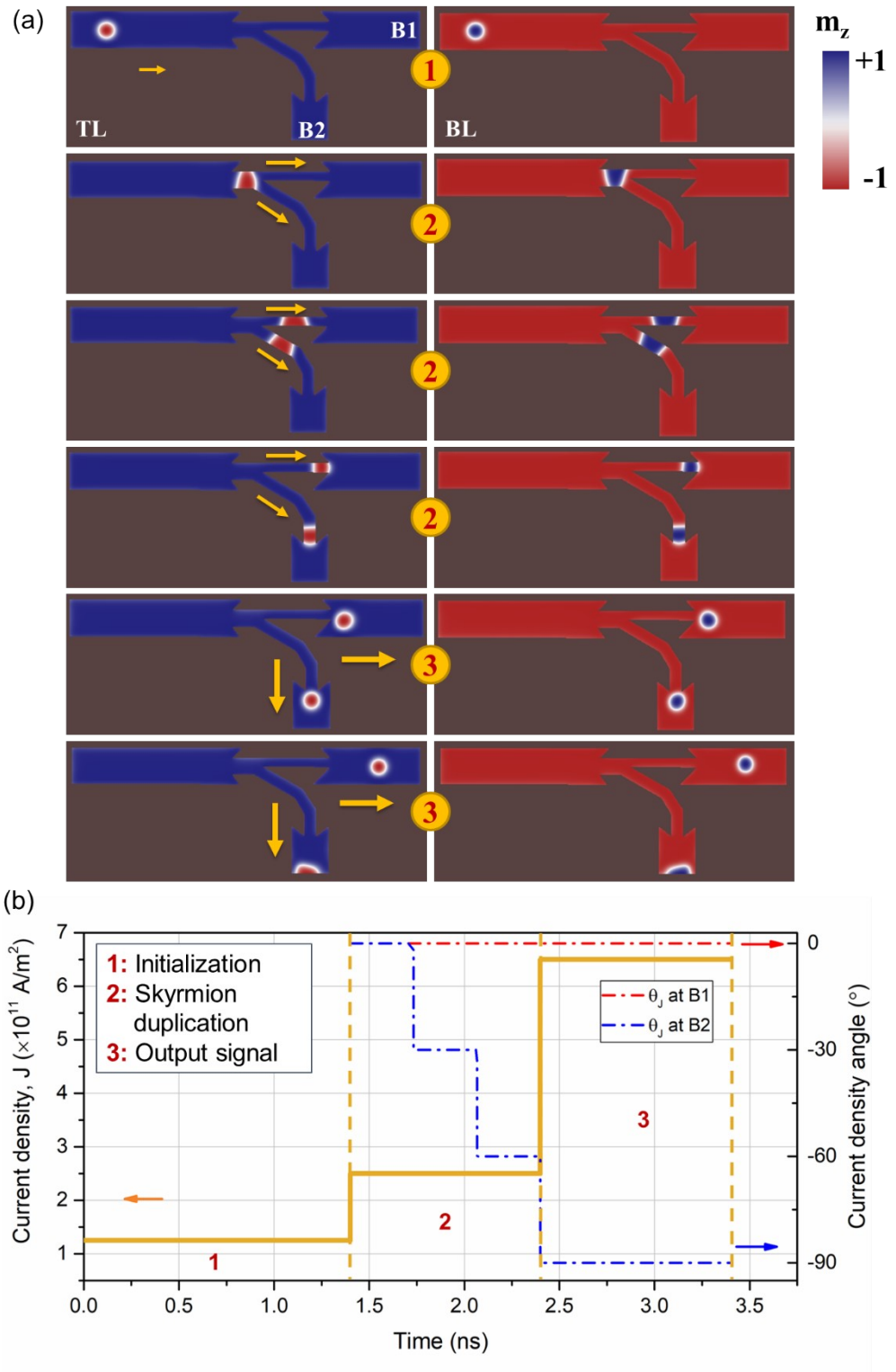


Supplementary Figure S2. MUX equivalent circuit schematic with SAF logic inverter, duplicator, and transfer blocks. The number on each block indicates the order in which the circuit operates.

S4. Duplicator Gate Block Operation and Energy Response

The stages of operation of the duplicator gate are shown in Figure S3, show how the stable SAF skyrmion pair goes through reversible skyrmion-DW conversions without losing their coupling, converting the input SAF skyrmion into two independent SAF skyrmions in the output branches. The SAF skyrmion is driven by current density applied from the left channel to the different branches to guide them to the output on the right side. The current density is mapped in magnitude and angle as plotted in Figure S3(b). We observe that the domain wall edges in the top and bottom interfaces don't exactly match in space, though the magnetic domains are still A-FM coupled. However, this didn't cause any decoupling between the domains, and we recovered the SAF skyrmion with decoupling. The created SAF skyrmion on the right is initially pushed in the horizontal channel with low current $J_e = 1.25\times10^{11}$ A/m^2 until reaching the narrow channel entrance, where two magnitudes of J_e are needed to push the skyrmion and obtain the DW pair. The DW pairs travel through the top and bottom branches, arriving at the end of the narrow channels and getting pinned by the large demagnetization field, creating an energy barrier. The current increased further up to 6.5×10^{11} A/m^2 in the last stage to push out the SAF skyrmions. The output skyrmions face the edge of the branches and are destroyed by the forces from the current and edge charges.

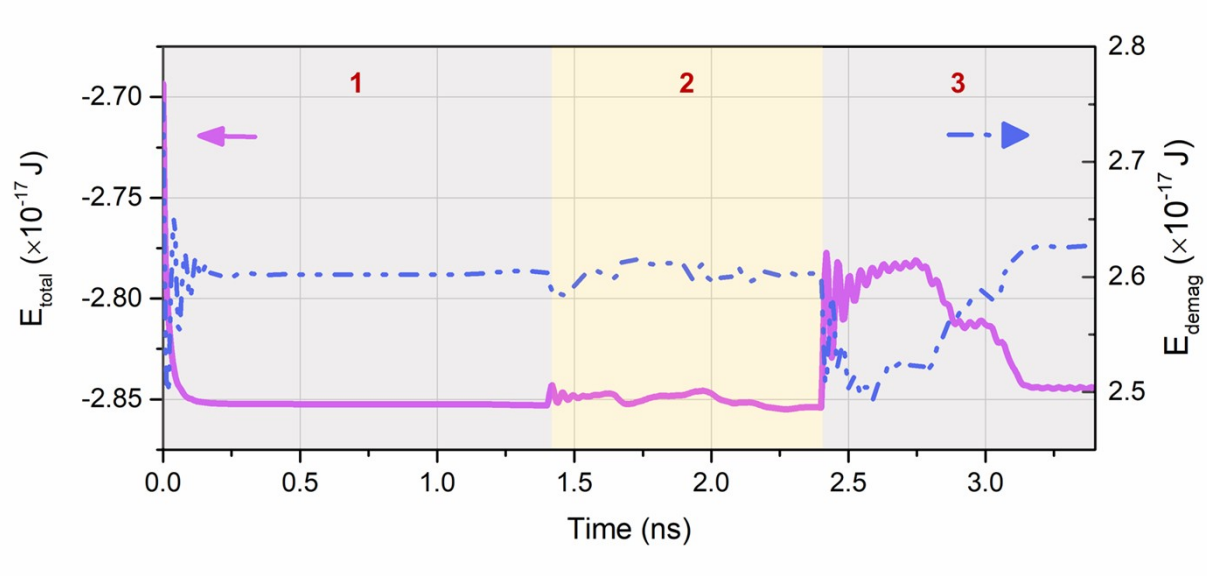
The performance of the SAF duplicator gate compared to the FM shows a faster switching delay time (t_d) obtained at lower currents. Where t_d = 3.4 ns compared to the response of the FM duplicator gate in Figure 5.2 where t_d = 5 ns, keeping in mind that we are still driving with one order of magnitude lower than current densities. Such power savings and high performance and stability shed light on the possible expansion of SAF skyrmion in more complex gates.



Supplementary Figure S3. Duplicator gate operation in the SAF system. (a) The different stages shown for SAF-paired skyrmions are shown with the top layer (TL) and the bottom layer (BL). (b) The applied current density time plot is according to the different stages in the gate operation and the simulated current density angle in the gate's top and bottom branches.

Spin current application shows the same effect on the energies plotted in Figure S4. The stable energy phase is observed in stage 1; however, the disturbance occurs when the skyrmion enters

the narrow channel and while the DW pairs are driven in branches B1 and B2 (refer to Figure S3(a)). The demagnetization energy E_{demag} drops while the total energy E_{total} increases as the DW pairs are pushed out of the channel by applying a large current density, overcoming the magnetostatic energy barrier at these points, shown in the 3rd stage.



Supplementary Figure S4. SAF skyrmion inverter gate (bottom layer) energy terms, $E_{total,}$ and E_{demag}, time response, respectively.

S5. Supplementary Videos and Their Descriptions

Supplementary Video SV1. SAF inverter logic operation. This video shows the operation stages and the time evolution of the inverter gate for logic input 1.

Supplementary Video SV2. SAF NOR logic operation for inputs (0,0). This video shows the operation stages and the time evolution of the NOR logic gate for logic inputs 0 and 0.

Supplementary Video SV3. SAF NOR logic operation for inputs (1,0). This video shows the operation stages and the time evolution of the NOR logic gate for logic inputs 1 and 0.

Supplementary Video SV4. SAF NOR logic operation for inputs (1,1). This video shows the operation stages and the time evolution of the NOR logic gate for logic inputs 1 and 1.

Supplementary Video SV5. SAF OR logic operation for inputs (1,0). This video shows the operation stages and the time evolution of the OR logic gate for logic inputs 1 and 0.

Supplementary Video SV6. SAF OR logic operation for inputs (1,1). This video shows the operation stages and the time evolution of the OR logic gate for logic inputs 1 and 1.

Supplementary Video SV7. SAF AND logic operation for inputs (0,1). This video shows the operation stages and the time evolution of the AND logic gate for logic inputs 0 and 1.

Supplementary Video SV8. SAF AND logic operation for inputs (1,1). This video shows the operation stages and the time evolution of the AND logic gate for logic inputs 1 and 1.

Supplementary Video SV9. SAF NAND logic operation for inputs (0,0). This video shows the operation stages and the time evolution of the NAND logic gate for logic inputs 0 and 0.

Supplementary Video SV10. SAF NAND logic operation for inputs (0,1). This video shows the operation stages and the time evolution of the NAND logic gate for logic inputs 0 and 1.

Supplementary Video SV11. SAF Multiplexer logic operation for inputs (0,1) and S = 1. This video shows the operation stages and the time evolution of the multiplexer logic gate for logic inputs 0 and 1 and select bit input 1.

S6. References

1. Büttner, F. et al. “Field-free deterministic ultrafast creation of magnetic skyrmions by spin– orbit torques”. Nat Nanotechnol 12, 1040–1044 (2017).
2. A. Mousavi Cheghabouri, F. Katmis, and M. C. Onbasli, “Cascadable direct current driven skyrmion logic inverter gate,” Phys Rev B, vol. 105, no. 5, p. 054411, Feb. 2022, doi: 10.1103/PhysRevB.105.054411.