Supplementary Information

Achieving Neuronal Dynamics with Spike Encoding and Spatial-Temporal Summation in Vanadium-based Threshold Switching Memristor for Asynchronous Signal Integration

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Keywords: Threshold Switching Memristor (TSM), Artificial Neuron, Spike Encoder, Spatial Summation, Spatial Temporal Summation

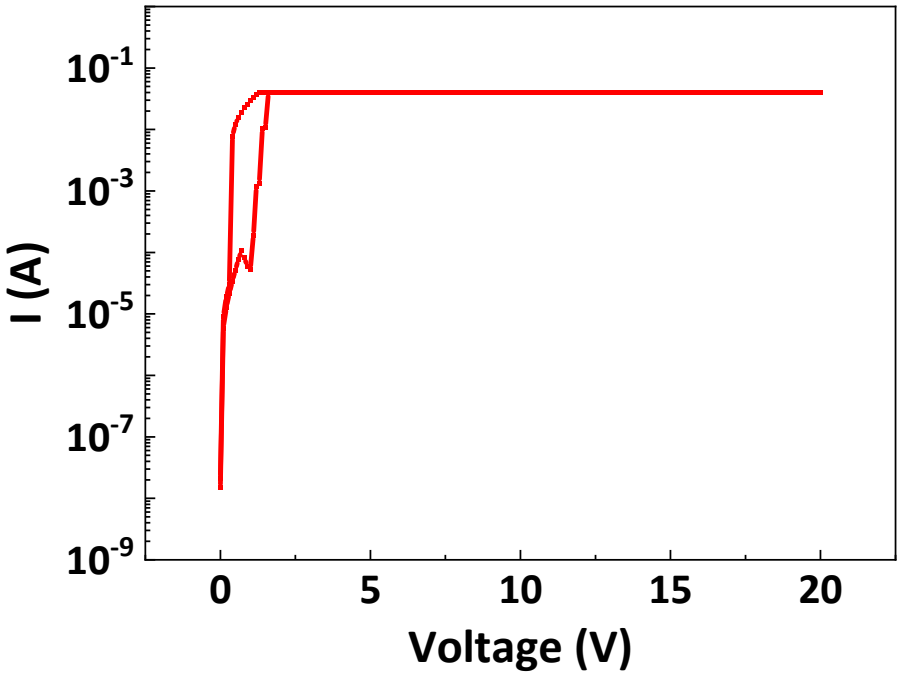

Figure S1. The electroforming process of the Pt/V/AlO_x/Pt threshold switching memristor (TSM) device. The voltage was swept from 0 to 20V and then returned to 0V, with a compliance current limit of 40 mA.

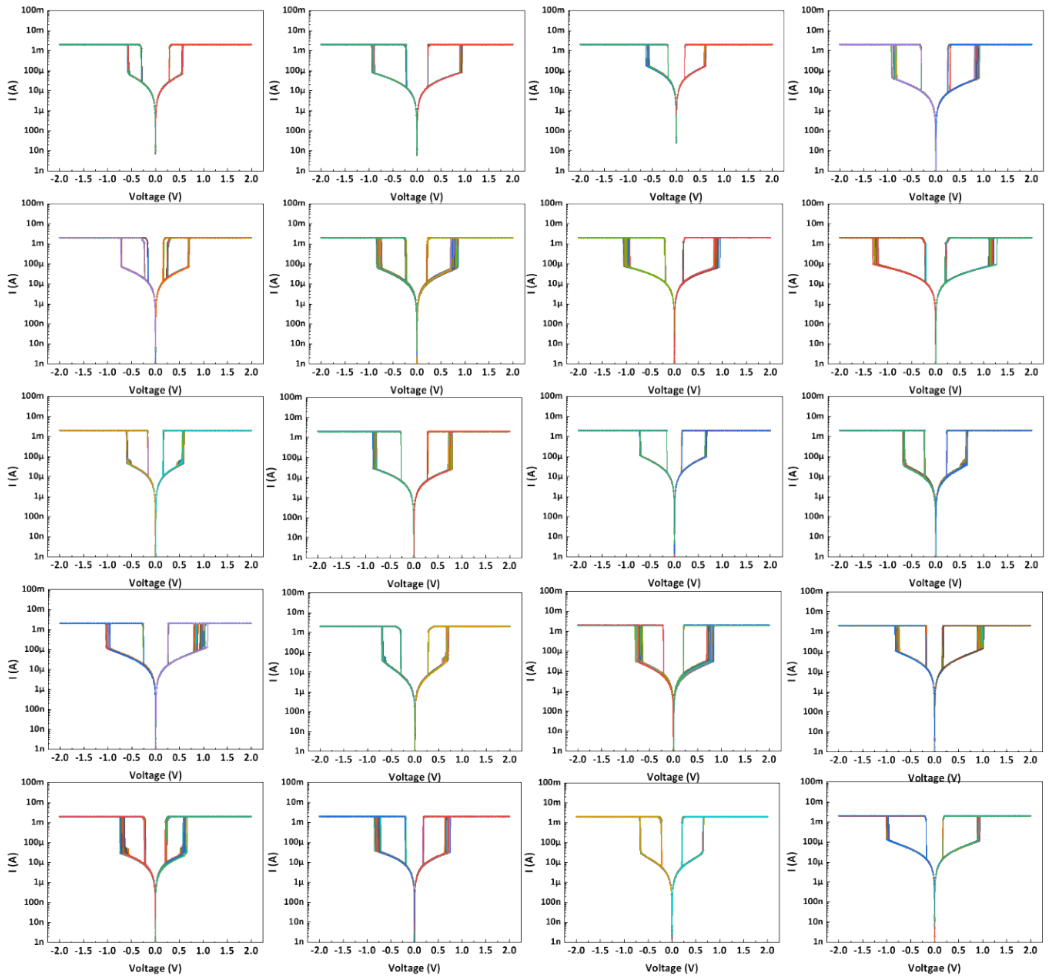

Figure S2. Current-voltage (I-V) characteristics of 20 Pt/V/AlO_x/Pt TSM devices.

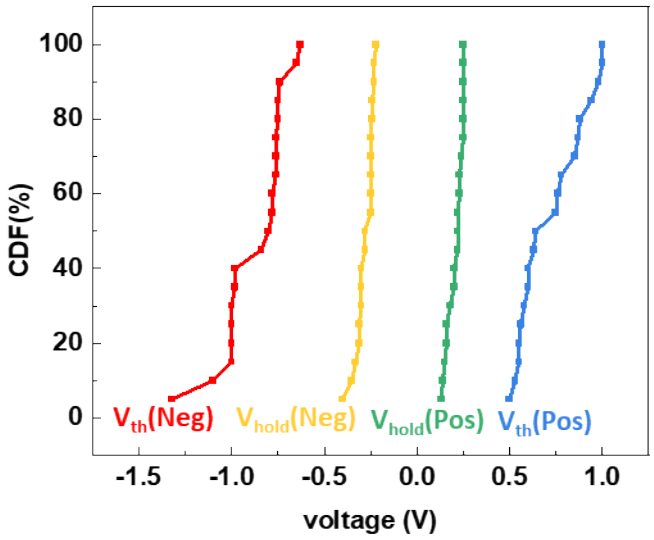

Figure S3. Statistical analysis of device-to-device variability in threshold voltage (V_{th}) and hold voltage (V_{hold}) for 20 Pt/V/AlO_x/Pt TSM devices. The mean values for positive V_{th}, positive V_{hold}, negative V_{hold} and negative V_{th} were 0.728 V, 0.209 V, -0.277 V and -0.856 V, respectively, with corresponding σ/μ values of 23.3%, 19.3%, 16.2% and 19.2%.

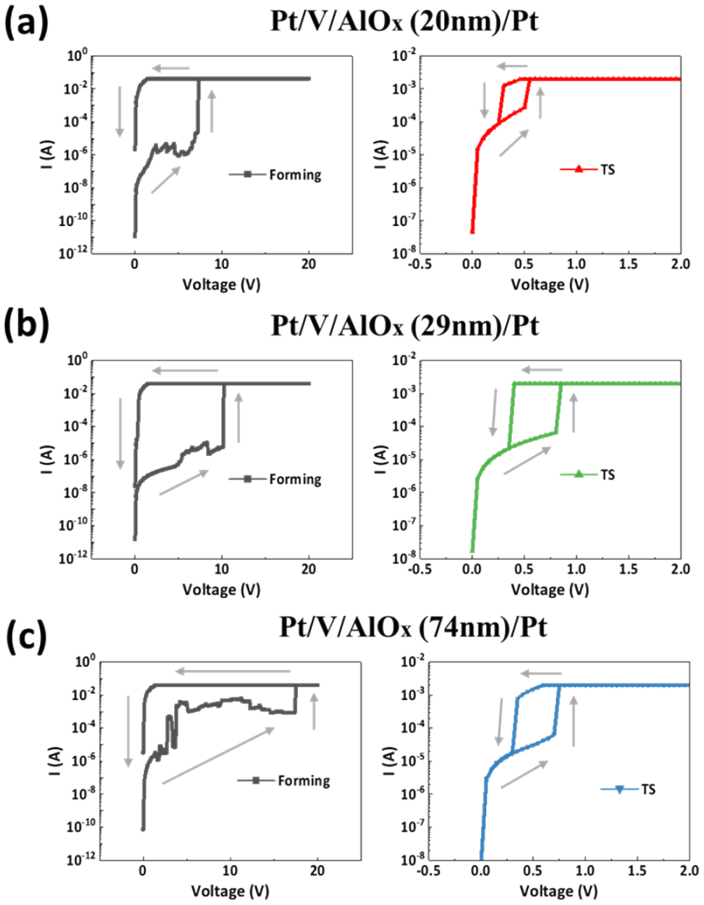

Figure S4. Forming process and threshold switching (TS) characteristics of Pt/V/AlO_x/Pt TSM devices with varying AlO_x thicknesses: (a) Pt/V/AlO_x (20 nm)/Pt, (b) Pt/V/AlO_x (29 nm)/Pt, and (c) Pt/V/AlO_x (74 nm)/Pt. Forming was performed with a 0V~20V~0V voltage sweep (compliance current: 40 mA), followed by TS characterization with a 0V~10V~0V voltage sweep (compliance current: 2 mA).

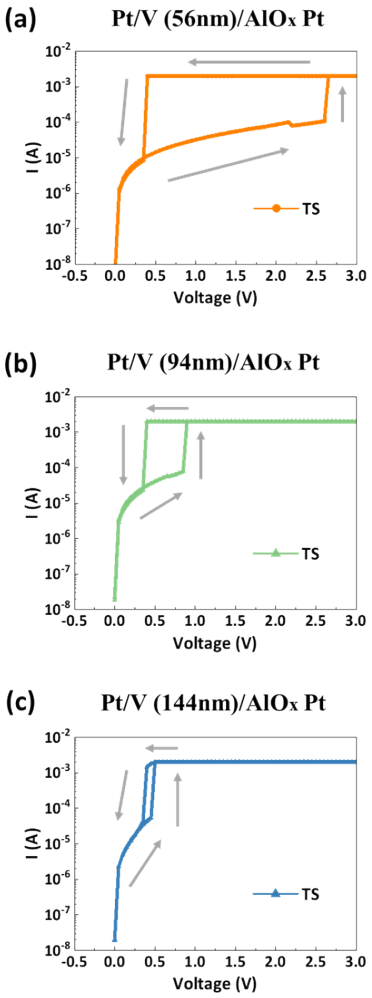

Figure S5. Threshold switching characteristics after the forming process of Pt/V/AlO_x/Pt TSM devices with varying V electrode thicknesses: (a) Pt/V (56 nm)/AlO_x/Pt, (b) Pt/V (94 nm)/AlO_x/Pt, and (c) Pt/V (144 nm)/AlO_x/Pt. Forming: 0V~20V~0 V (CC: 40 mA), followed by TS: 0V~10V~0V (CC: 2 mA).

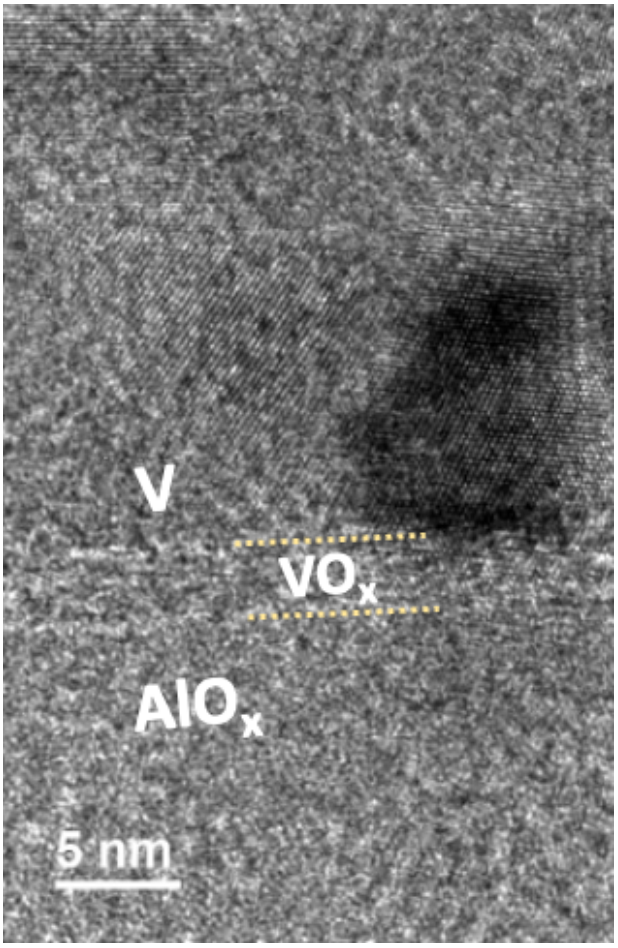

Figure S6. HR-TEM image of the Pt/V/AlO_x/Pt device at the V/AlO_x interface, showing the presence of VO_x following electrical operation.

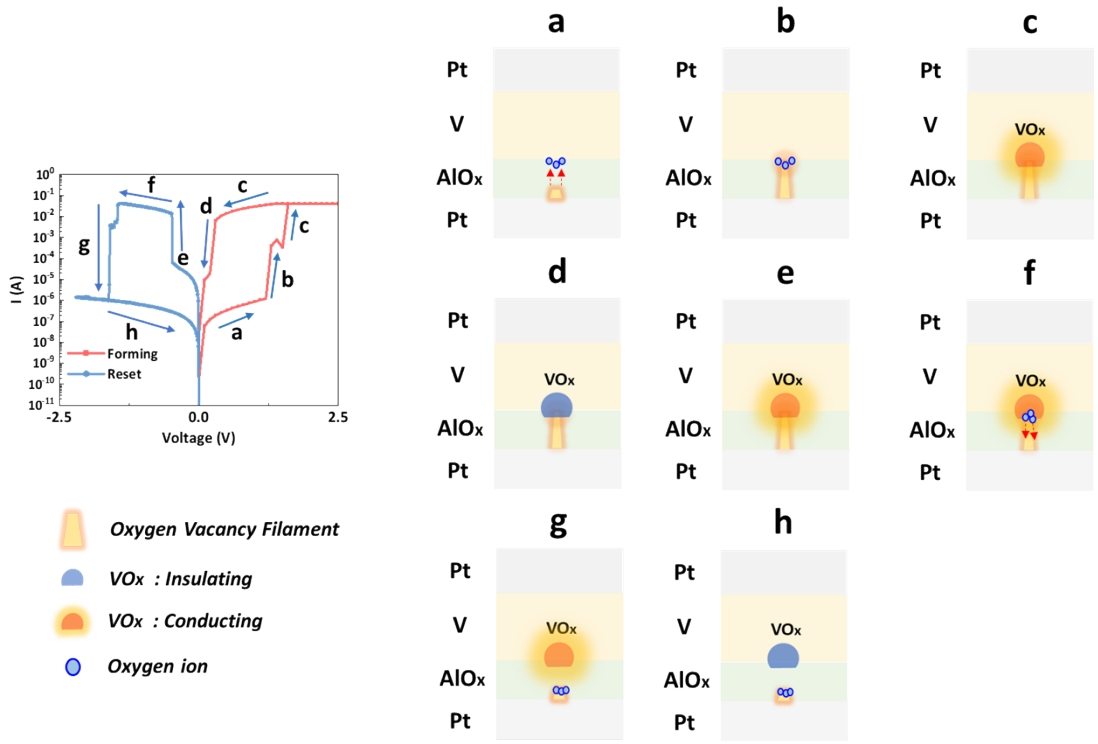

Figure S7. Schematic illustration of the resistive switching (RS) mechanism in the Pt/V/AlO_x/Pt TSM device. The left panel shows the experimentally measured I-V characteristics, while the right panel depicts the corresponding internal processes within the device.

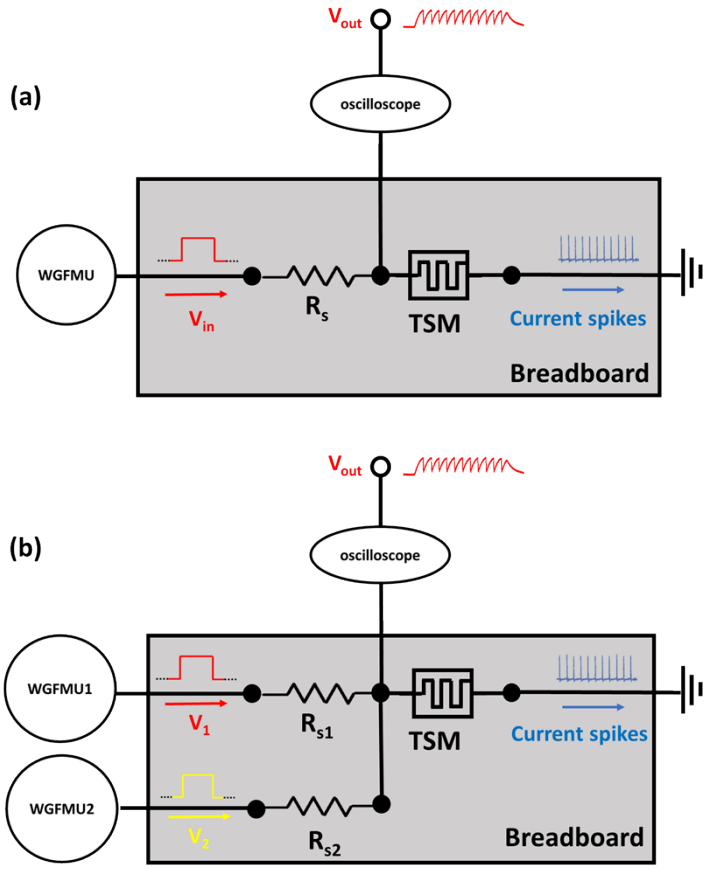

Figure S8. (a) The layout of Figure 4(b) in the real case. (b) The layout of Figure 4(f) in the real case. The pulse input is generated by a waveform generator (WGFMU) and is applied through a series resistor and the TSM device, resulting in a current spike response. The voltage across the TSM device (V_{out}) is monitored using an oscilloscope to capture the voltage dynamics.

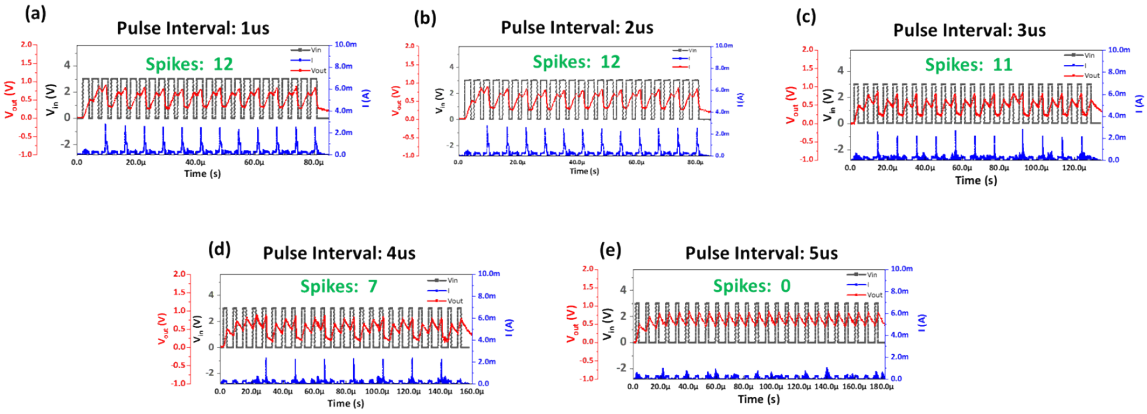

Figure S9. Temporal summation characteristics of the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit in response to 20 input voltage pulses, each with an amplitude of 3V and a pulse width of 2 µs, with varying pulse intervals. The resulting output spike trains are shown for pulse intervals of (a) 1 µs, (b) 2 µs, (c) 3 µs, (d) 4 µs, and (e) 5 µs.

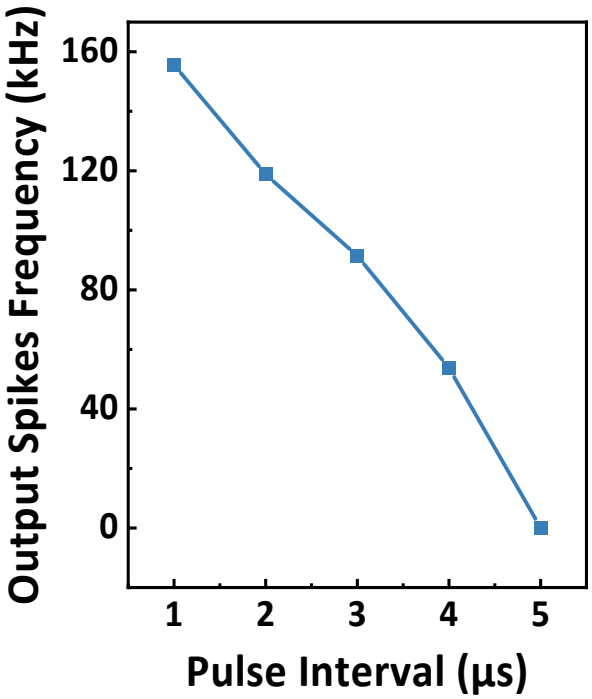

Figure S10. The relationship between the output current spike frequency of the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit and the pulse interval of the input voltage pulse train.

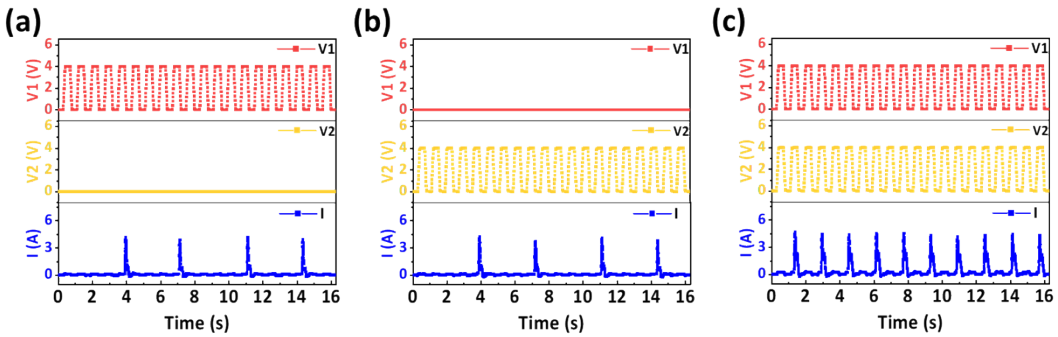

Figure S11. Spatial summation properties of the Pt/V/AlO_x/Pt-based artificial neuron under a specified pulse train condition: Twenty voltage pulses, each with an amplitude of 4V, a pulse width of 3 μs, and an interval of 3 μs, were applied to (a) terminal 1, (b) terminal 2, and (c) both terminal 1 and terminal 2.

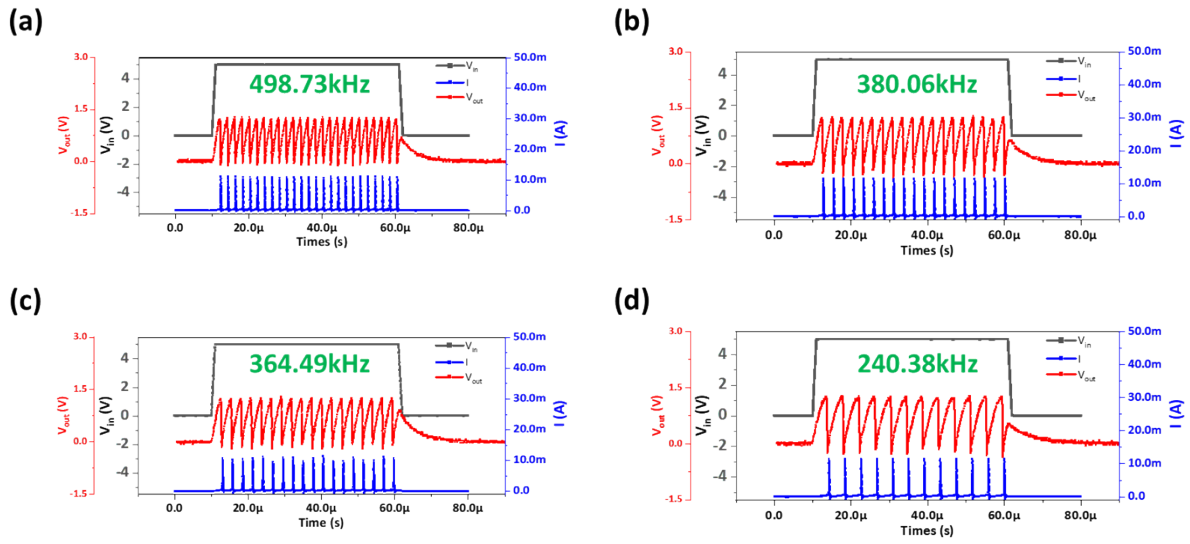

Figure S12. The relationship between the resistance of the series resistor and the output current spike frequency in the Pt/V/AlO_x/Pt-based spike encoder circuit. Series resistors used: (a) 3.9 kΩ, (b) 4.7 kΩ, (c) 5.1 kΩ, and (d) 6.8 kΩ. (Experiments were conducted with single voltage pulse of 5 V amplitude and 50 μs width)

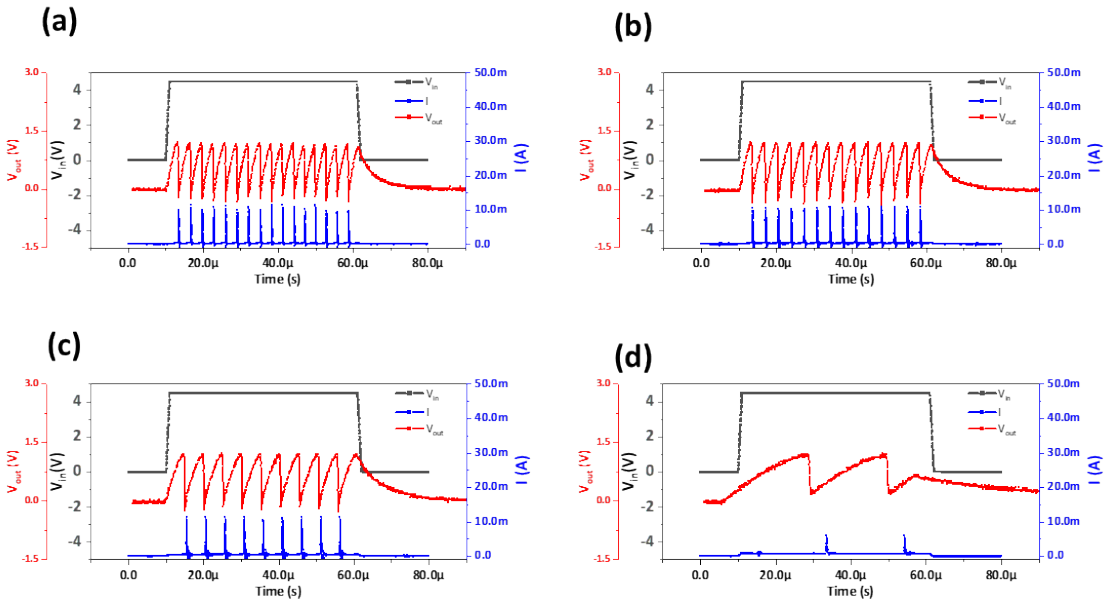

Figure S13. The relationship between the capacitance of the parallel capacitor and the output current spike frequency in the Pt/V/AlO_x/Pt-based spike encoder circuit. Capacitors used: (a) parasitic capacitance (b) 0.1 nF capacitor, (c) 1 nF capacitor, and (d) 10 nF capacitor. (Experiments were conducted with single voltage pulses of 4.5 V amplitude and 50 µs width)

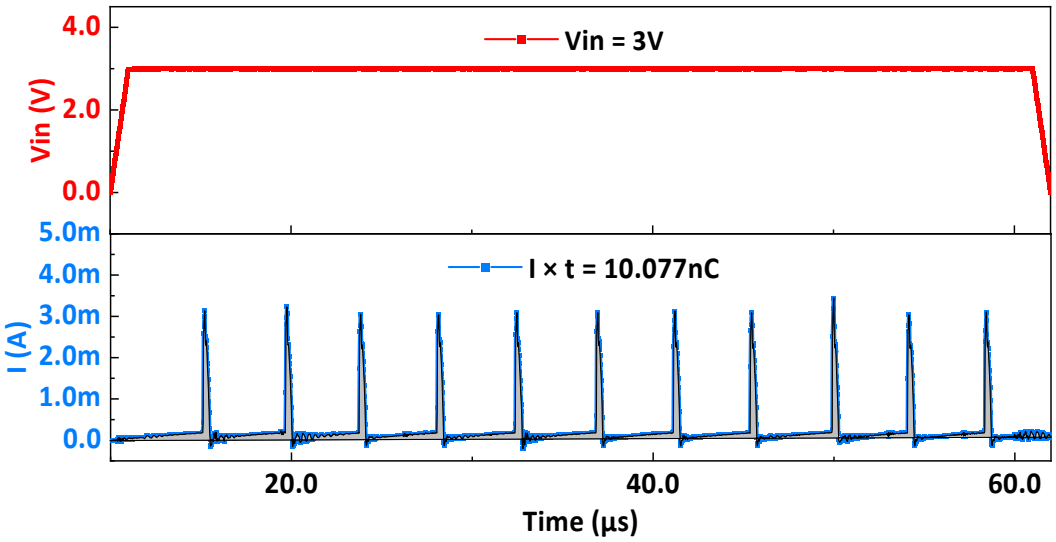

Figure S14. Energy consumption analysis of the Pt/V/AlO_x/Pt TSM-based spike encoder. The transient power was determined by multiplying the applied voltage by the time integral of the output current (I × t). The energy consumption, quantified by dividing the total power consumption by the number of spikes generated, was calculated to be 2.75 nJ. (Input voltage pulse conditions: Pulse amplitude of 3 V and pulse width of 50 µs.)

Supplementary Note

This section will explain the operational mechanism of the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit. This circuit primarily consists of an external resistor (R_S), a capacitor (C_p), which can either be an external capacitor or the parasitic capacitance of the TSM device, and the Pt/V/AlO_X/Pt TSM device. Since the core operation of this circuit is closely related to the charging and discharging of C_p, the following will describe the C_p's charging and discharging paths, as well as the calculation of the accumulated voltage across the C_p and the current flowing through the ground terminal. First, when continuous voltage pulses are applied to the artificial neuron, they charge C_p through the resistor R_S, as illustrated in the middle inset of Figure SN1. The accumulated voltage across C_p is denoted as $V_C(t)$, as shown in the formula below the middle inset of Figure SN1. When a voltage is accumulated across C_p, it continuously discharges through the circuit, with the discharge path depicted in the right inset of Figure SN1. C_p discharges through the TSM device, and the voltage after discharge is calculated as shown in the formula below the right inset of Figure SN1.

During the operation of this artificial neuron, C_p simultaneously charges and discharges. The rates of charging and discharging dictate whether the accumulated voltage across C_p increases or decreases. When the charging rate exceeds the discharging rate, the accumulated voltage increases; conversely, when the charging rate is slower, the accumulated voltage decreases. Additionally, the current measured at the ground terminal corresponds to the discharge current flowing through the TSM device, as illustrated in the formula below the right inset of Figure SN1. Since the capacitor blocks direct current, no current flows into the ground terminal through C_p, so this factor is excluded from the calculation of the current flowing to the ground terminal.

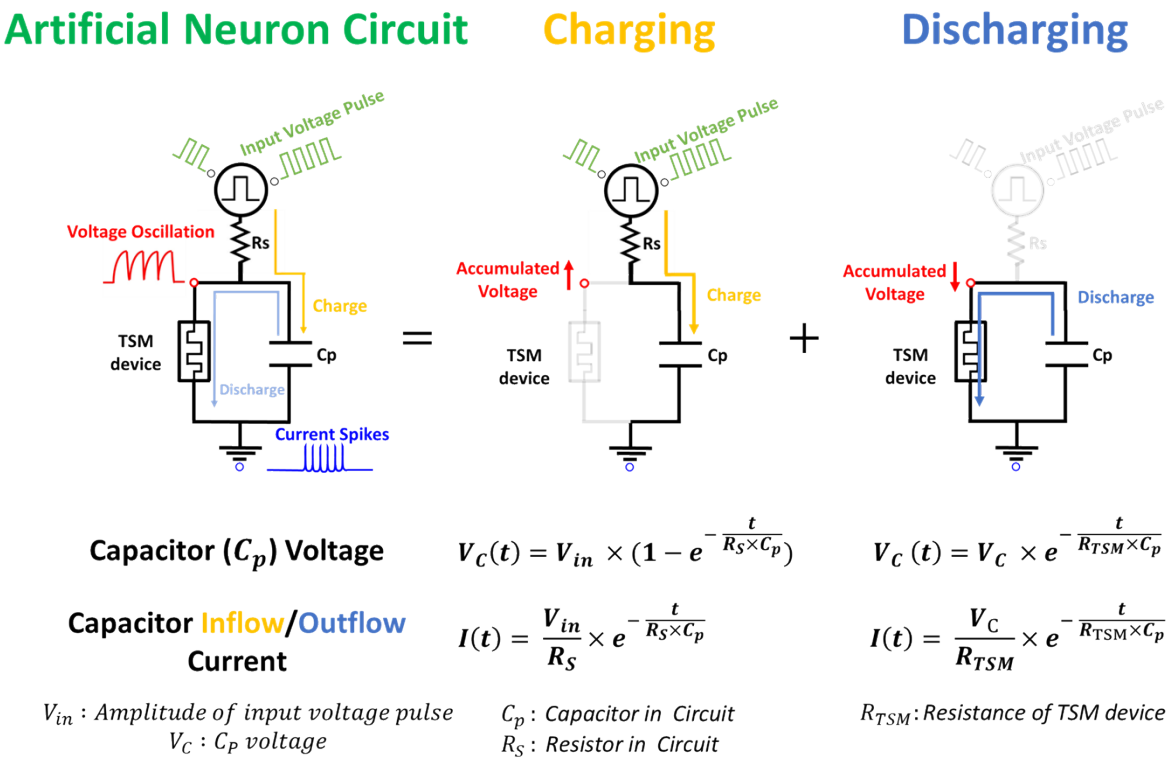

Figure SN1. Schematic of the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit illustrating the charging and discharging paths of C_p, the voltage accumulation across C_p, and the current calculations at the ground terminal.

Following the previous discussion, we will now examine the three key phases in the operation of the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit: (1) when a voltage pulse is applied, (2) during the intervals between pulses or when the pulse has ceased, and (3) when the accumulated voltage across C_p reaches the V_{th} of the TSM device.

As illustrated in Figure SN2, during the first phase, when a voltage pulse is applied to the artificial neuron circuit, careful selection of the input pulse amplitude (V_{in}) and the resistor (R_S) allows for control over the charging speed of C_p, ensuring it exceeds the discharging rate. Consequently, the voltage accumulated during charging surpasses the voltage dissipated during discharge, as depicted by the equation at the bottom of Figure SN2. This initiates the charging process of C_p, causing the accumulated voltage across C_p to increase, as shown in the right inset of Figure SN2. At this stage, the TSM device remains in its high resistance state, represented by R_{HRS} in the equation. As a result, the current flowing through the ground terminal, highlighted in blue in the equation of Figure SN2, remains minimal due to the high resistance state of the TSM device.

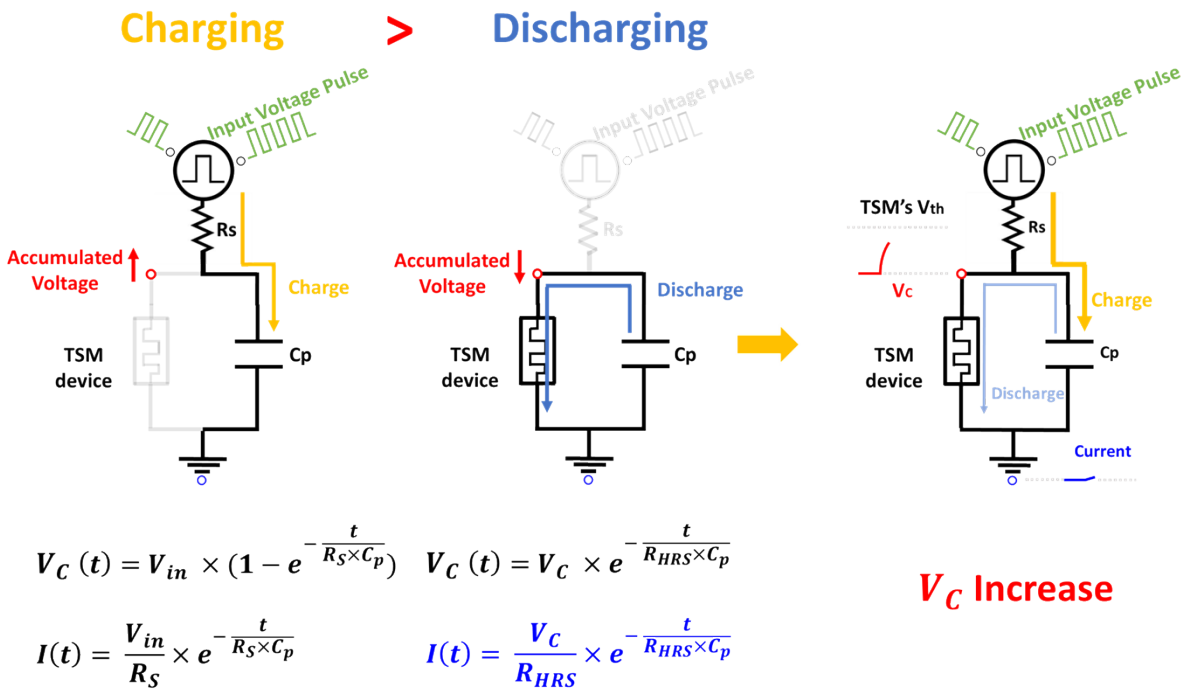

Figure SN2. Charging and discharging behavior of C_p in the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit, along with voltage accumulation across C_p and current at the ground terminal under continuous input voltage pulses.

The second phase occurs when the input voltage ceases or during the intervals between voltage pulses, as depicted in Figure SN3. During this phase, the artificial neuron circuit does not receive any input voltage pulses, resulting in the input voltage amplitude being zero (V_{in} = 0), as indicated by the red text in the formula beneath the left inset of Figure SN3. From the C_p charging voltage formula, $V_c(t)$, it is evident that with Vin at zero, C_p ceases to charge and solely discharges through the circuit. The discharge path, as illustrated in the middle inset of Figure SN3, shows Cp discharging through the TSM device to the ground terminal. Based on the combined charging and discharging effects, it is evident that the discharging process dominates during this phase, leading to a decrease in the voltage across C_P, as shown in the right inset of Figure SN3. The current flowing through the ground terminal continues to be the discharge current from C_P, passing through the TSM device to the ground, as calculated using the blue text formula beneath the right inset of Figure SN3. Since the TSM device remains in its high resistance state, the current reaching the ground terminal remains minimal.

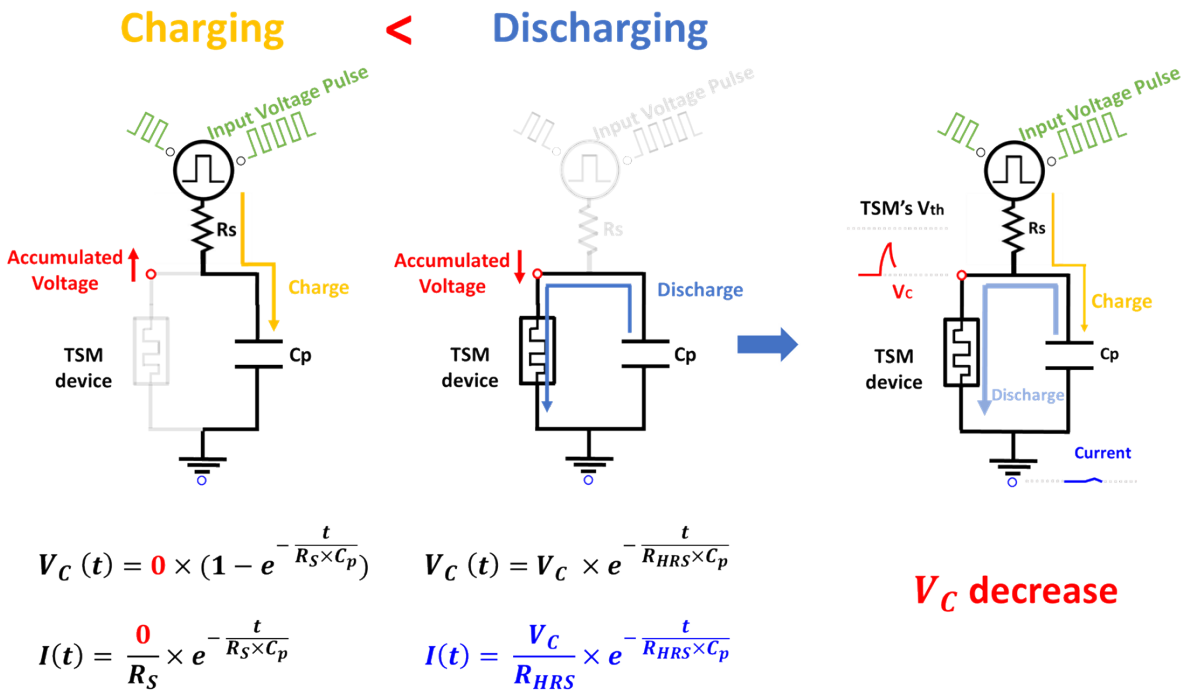

Figure SN3. Charging and discharging behavior of C_P in the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit, along with voltage accumulation across C_p and current at the ground terminal during intervals between voltage pulses or when input voltage pulses cease.

When the artificial neuron circuit continuously receives input voltage pulses, it repeatedly undergoes the charging and discharging processes of C_p described in the first two phases. Once the accumulated voltage across C_p reaches the V_{th} of the TSM device, the equipotential effect causes the voltage across the TSM device to match the accumulated voltage across C_p. At this point, the TSM device transitions from HRS to LRS, initiating the third phase.

As illustrated in Figure SN4, during this phase, the charging rate of C_p remains unaffected by the resistance state transition of the TSM device (as shown by the formula below the left inset of Figure SN4). However, the discharging rate of C_p increases significantly as the TSM device switches to LRS, as indicated by the formula for C_p's discharging voltage V_C (t) in Figure SN4. The discharging rate, expressed as $-dV_C(t)/R_{LRS} \times C_p$, becomes substantially higher than the charging rate, $dV_C(t)/R_S \times C_p$, due to $R_{LRS} \times C_p << R_S \times C_p$. Consequently, the voltage across C_p decreases rapidly, as depicted by the red line in the right inset of Figure SN4.

As the voltage across C_p continues to decrease, it eventually reaches the V_{hold} of the TSM device, causing the TSM device to revert to HRS. During this transition, there is a significant increase in the discharge current flowing from C_p through the TSM device to the ground terminal, as shown by the blue formula below the middle inset of Figure SN4. This surge leads to a transient high current at the ground terminal, as illustrated by the blue line in the right inset of Figure SN4. Once the TSM device returns to HRS, the charging and discharging time constants revert to those observed in the first phase, allowing C_p to resume charging, while the transient high current at the ground terminal diminishes to its initial low value, triggering a current spike.

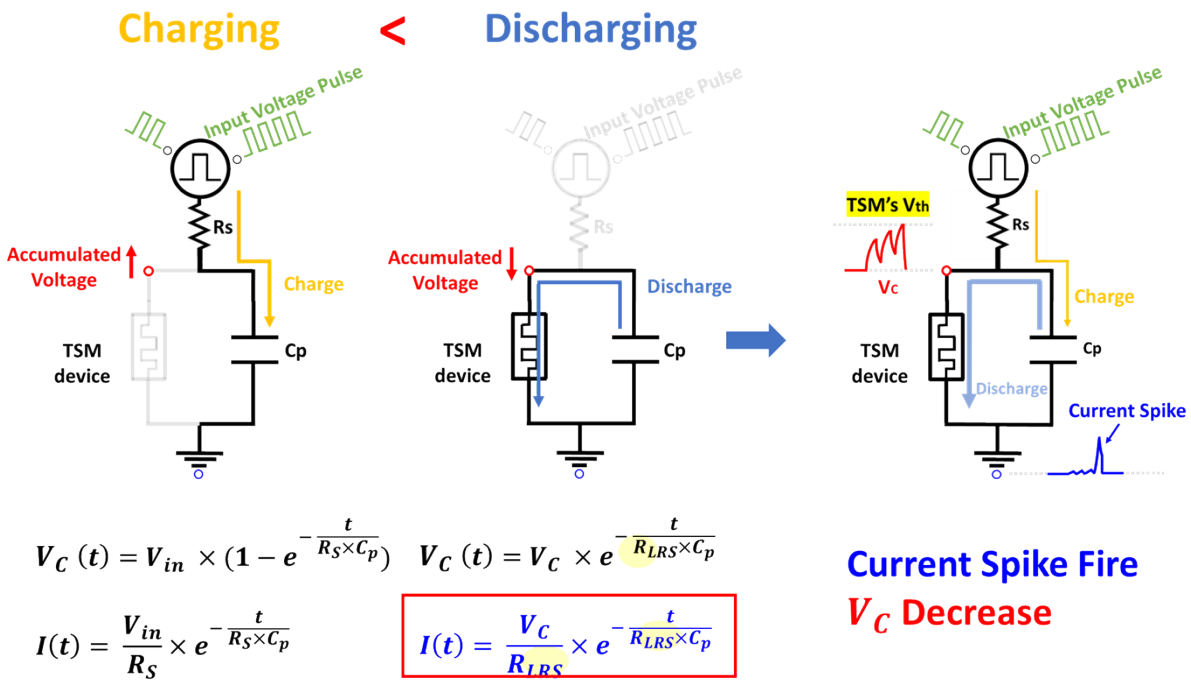

Figure SN4. Charging and discharging behavior of C_p in the Pt/V/AlO_x/Pt TSM-based artificial neuron circuit, along with voltage accumulation across C_p and current at the ground terminal when the voltage across C_p reaches the V_{th} of the TSM device.

Table S1. The comparison of electrical functionalities in different TSM devices.

Device Structure	**V_{th}**	**V_{hold}**	**Energy Consumpation**	**Swithing speed on/off**	**Function**	**Spatial summation**	**Spatial-temporal summation**	**ref**
Pt/V/AlO_X/Pt	0.84V	0.37V	2.75 nJ/spike @ 3V/50us Pulse	~165 ns/310 ns @1V/1us Pulse	Artificial neuron Spike encoder	✓	✓	This work
Au/VO_2/Au	3.4V	1.45V	6.92 nJ/spike	~70 ns/60 ns	Spike encoder	×	×	[r1]
Pt/VO_2/Pt	~1.22V	~0.4V	N/A	N/A	Artificial neuron	×	×	[r2]
Au/VO_2/Au	15V	5V	N/A	N/A	Spike encoder	×	×	[r3]
Pt/Ti/NbO_X/Pt /Ti	0.8V	0.6V	~ 392 μW	~50 ns/25 ns @1V/1us Pulse	Artificial neuron	✓	✓	[r4]
Ti/Pt/VO_2/Pt	~1.7V	~0.6V	N/A	N/A	Spike encoder	×	×	[r5]
Pt/VO_2/Pt	~1.4V	~0.4V	N/A	N/A	Artificial neuron	×	×	[r6]
Au/VO_2/Pt	1.35V	0.85V	2.9 nJ/spike @ 5V/30μs Pulse	~200 ns/75 ns @ 1.5V/1us Pulse	Spike encoder	×	×	[r7]
V/HWOx/Pt	~1.22V	~0.7V	N/A	N/A	Artificial neuron	×	×	[r8]
Pt/NbOx/Pt	2.3V	1.6V	0.9 nJ/spike @ 3.2V/1μs Pulse	~60 ns/100 ns @ 2.3V/1us Triangle Pulse	Artificial neuron	✓	✓	[r9]
ITO/IGZO/Ag /Ta_2O_5/ITO	0.27V	0.04V	210 nW @360 nm 400 pW @405 nm 4.1 pW @532 nm	40ns/55ns @ 2.5V/2μs Pulse	Spike-encoding Color selectivity	×	×	[r10]
Ag/TaO_x/ITO	0.2-0.4V	0.1V	0.25–0.5 μW per spike	10ns/40ns @ 1V/2μS Pulse	photoelectric spiking neuron	✓	×	[r11]

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