# Supporting Information

# Suppression of Surface Optical Phonon Scattering by AlN Interfacial Layers for Mobility Enhancement in $MoS_2$ FETs

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## Figure S1: MOCVD-grown $MoS_2$ thin film

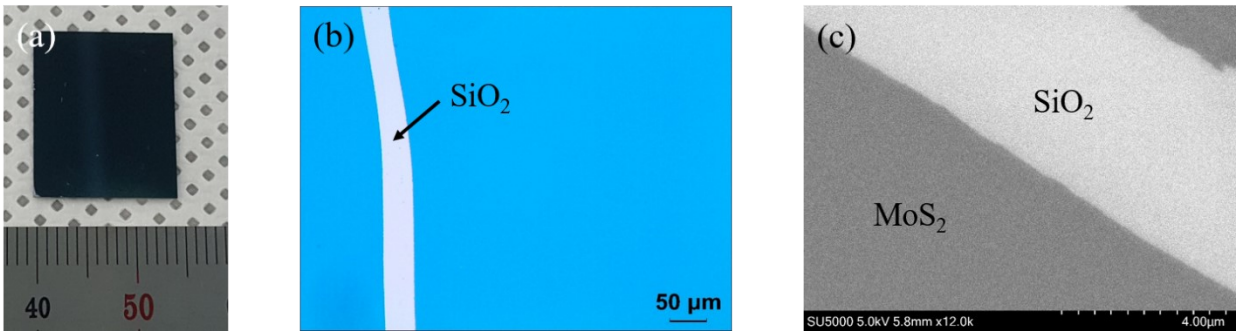


**Figure S1.** (a) Photograph of the $MoS_2$ thin film grown on a $SiO_2$/Si substrate. (b) Optical microscopy (OM) image and (c) scanning electron microscopy (SEM) image of metal-organic chemical vapor deposition (MOCVD)-grown $MoS_2$ thin film.

## Figure S2: XPS analysis for $MoS_2$ thin film

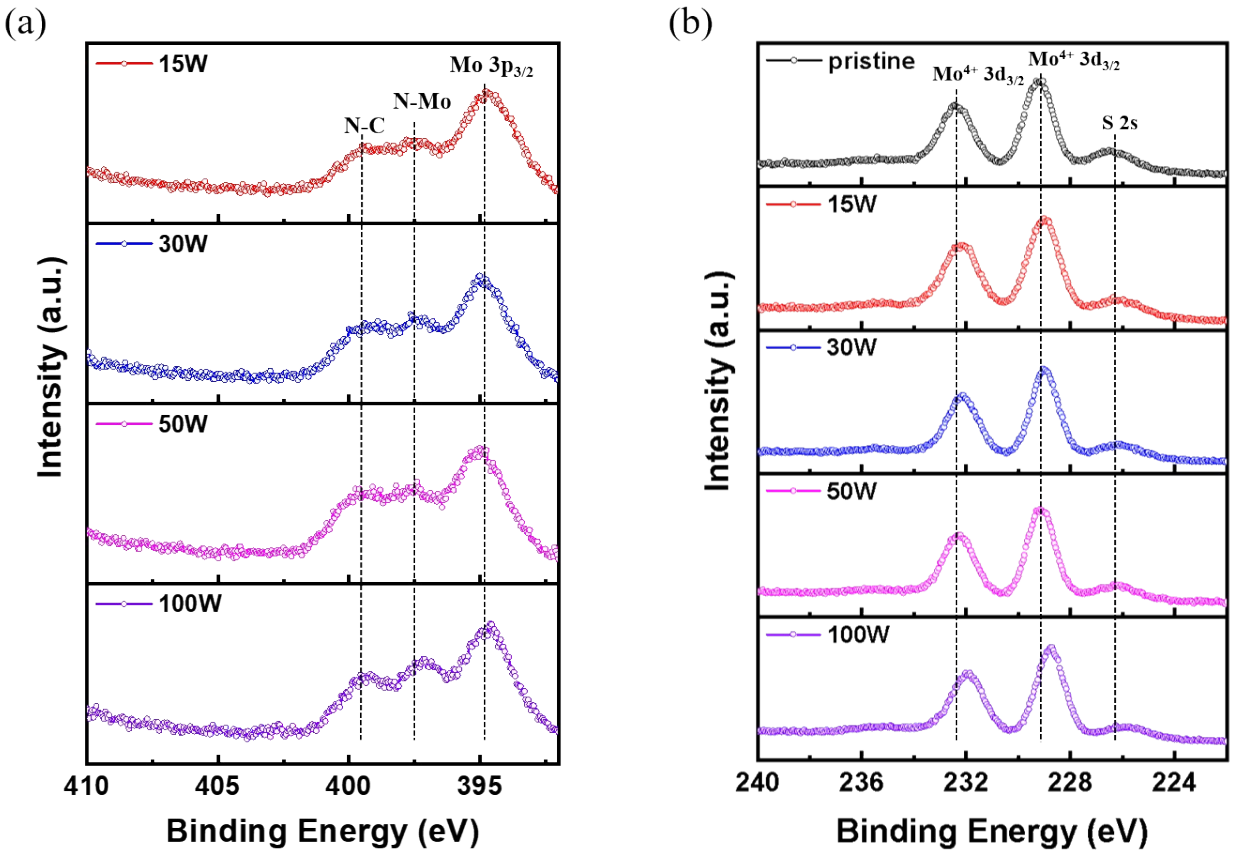


**Figure S2.** XPS spectra of (a) N 1s and (b) Mo 3d in AlN/$MoS_2$ stack corresponding to the plasma power for AlN deposition.

## Figure S3: XPS analysis for AlN film

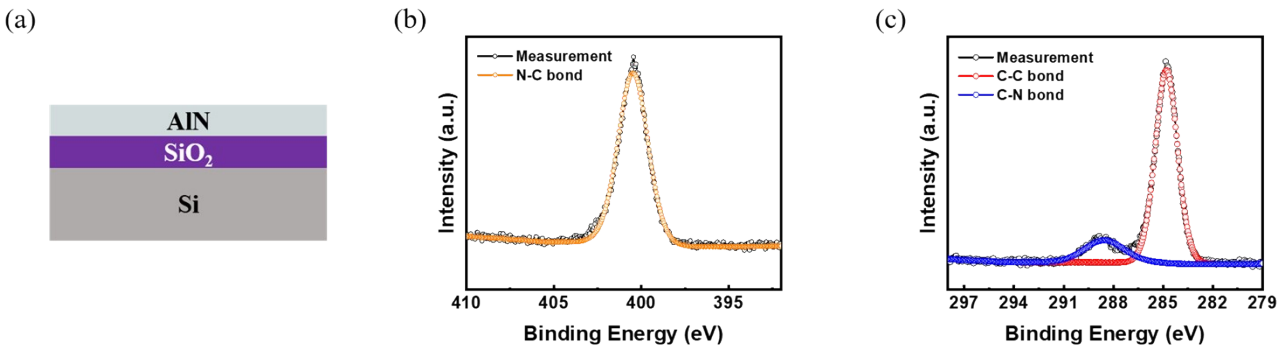


**Figure S3.** (a) AlN deposited on $SiO_2$ and the XPS spectrum with (b) N 1s showing N-C bond and (c) C 1s showing C-N bond.

## Figure S4: $MoS_2$ FETs images

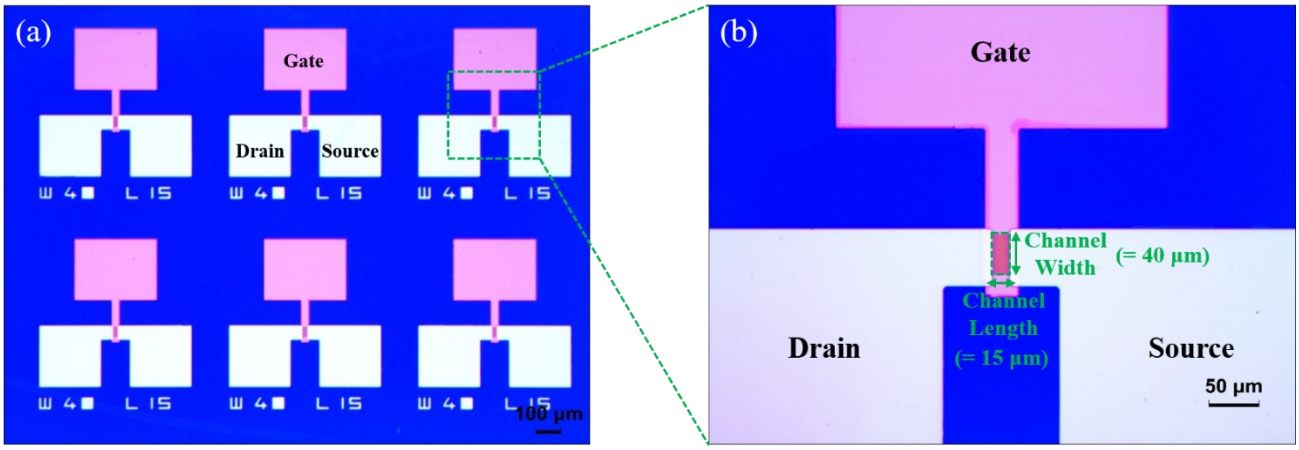


**Figure S4.** (a) OM image of $MoS_2$ FETs with bottom gate-staggered structure and (b) its magnified image.

**Figure S5: TEM analysis for $MoS_2$ thin film sandwiched by AlN interfacial layers**

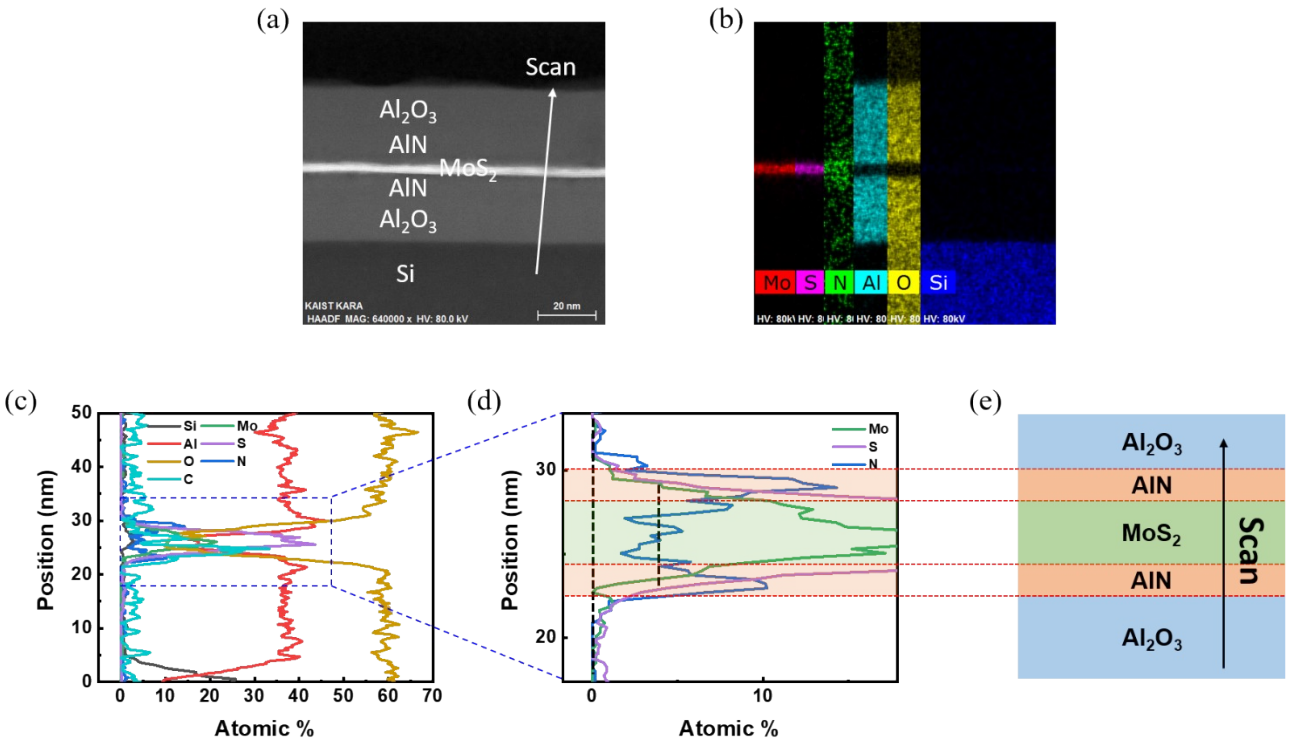


**Figure S5.** (a) Cross-sectional TEM image of $MoS_2$ thin film sandwiched by AlN interfacial layers and (b) its Energy-dispersive X-ray spectroscopy mapping image. (c) Elemental distributions along the scan direction in (a). (d) Elemental distribution around $MoS_2$ thin film and (e) its corresponding stacking structure.

## Figure S6: Energy band diagram depending on the strain

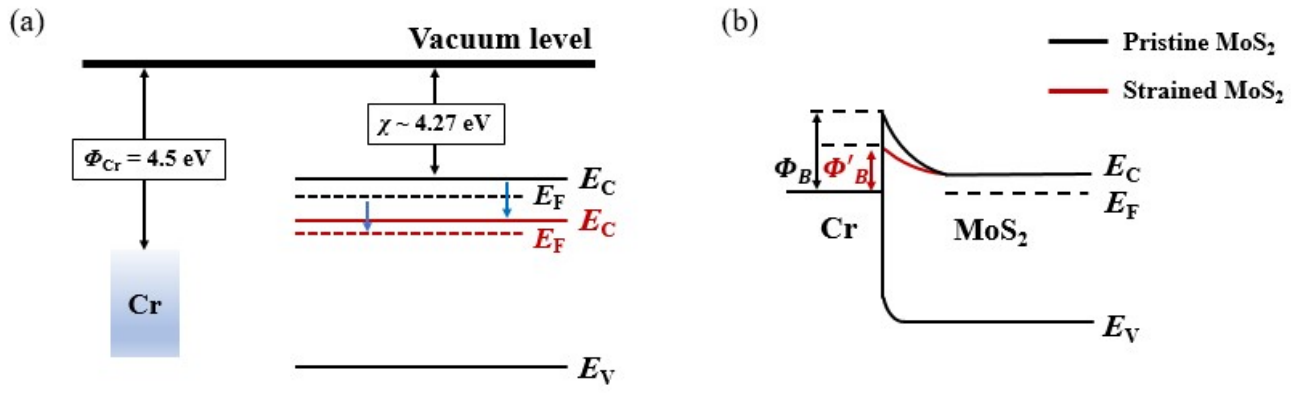


**Figure S6.** (a) Energy band diagram of $MoS_2$ before and after the bandgap reduction by conduction band edge. (b) Schottky barrier height change after the bandgap reduction resulting from strain.

## Figure S7, S8, and S9: Electrical characteristics of $MoS_2$ FETs according to the interface types

Compared with $MoS_2$ FETs with $Al_2O_3$ sandwich structure, $MoS_2$ FETs with AlN TIL (regardless of the BIL types) yield off-current level increases due to the lowering of the Schottky barrier height by strain,[1-3] resulting in the degradations in terms of on/off current ratio and SS, as shown in Figure S9a. As a result of SS change, $V_T$ extracted from $10^{-7}$ A by the constant current method varies accordingly.[4] When $MoS_2$ FETs use AlN as the TIL (regardless of the BIL types), the strain effect caused by incorporating nitrogen atoms into the $MoS_2$ thin film remains similar, resulting in comparable $V_T$ values. However, $MoS_2$ FETs with AlN BIL also yield negative shift trends in $V_T$ compared with the $MoS_2$ FETs with $Al_2O_3$ sandwich structure. It is well known that the AlN/$Al_2O_3$ gate dielectric stack demonstrates an excellent interface quality with $MoS_2$ by reducing the trap density near the interface.[5] Therefore, a steeper slope in the subthreshold region could be achieved

by the rapid transition of the off- to the on-state, showing the negatively shifted $V_T$. From the $n_{2D}$ viewpoint, using plasma for AlN deposition causes nitrogen to penetrate the $MoS_2$ thin film,[6] inducing strain and modifying the band structure at the MS junction, as shown in Figure S6b,[1-3] thereby changing the $n_{2D}$ value. That is, $n_{2D}$ is only affected by the types of TIL. For this reason, $MoS_2$ FETs with AlN TIL always yield higher $n_{2D}$ values than $MoS_2$ FETs with $Al_2O_3$ TIL regardless of the BIL types.

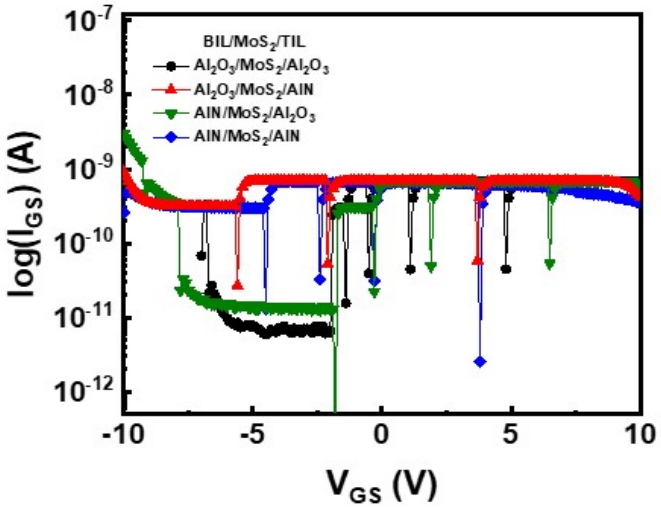


**Figure S7.** Gate leakage current characteristics of $MoS_2$ FETs in log scale according to the interface types

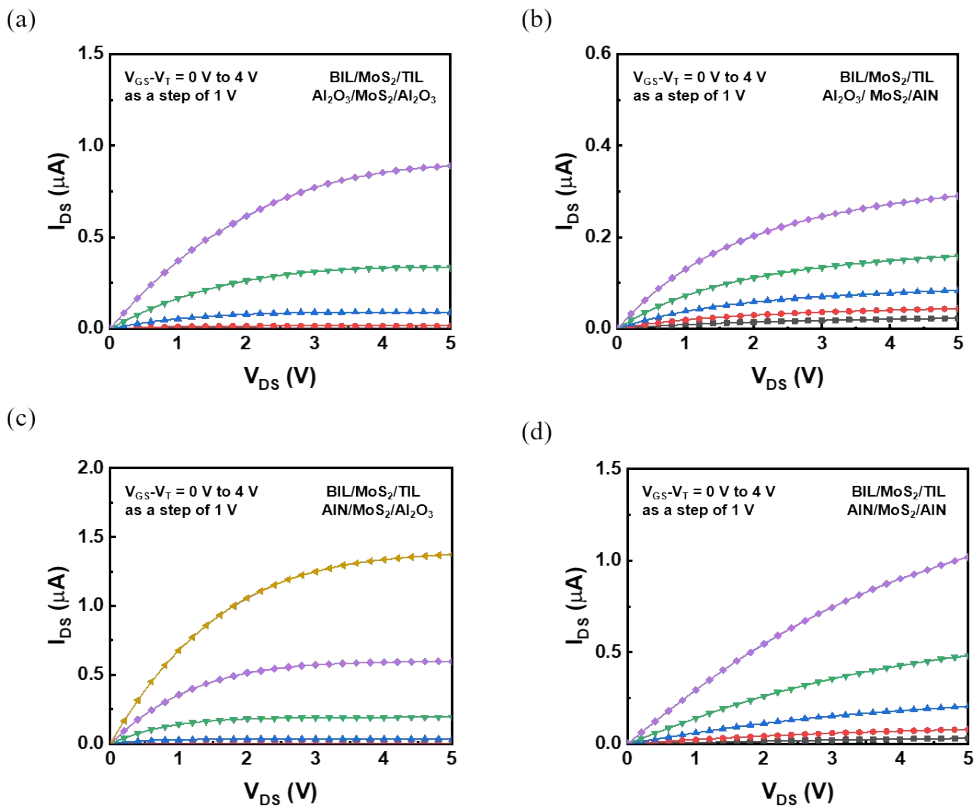


**Figure S8.** Representative output characteristics of $MoS_2$ FETs with different types of interfacial layers ranging from $V_{GS} - V_T = 0$ V to $V_{GS} - V_T = 4$ V (step of 1 V).

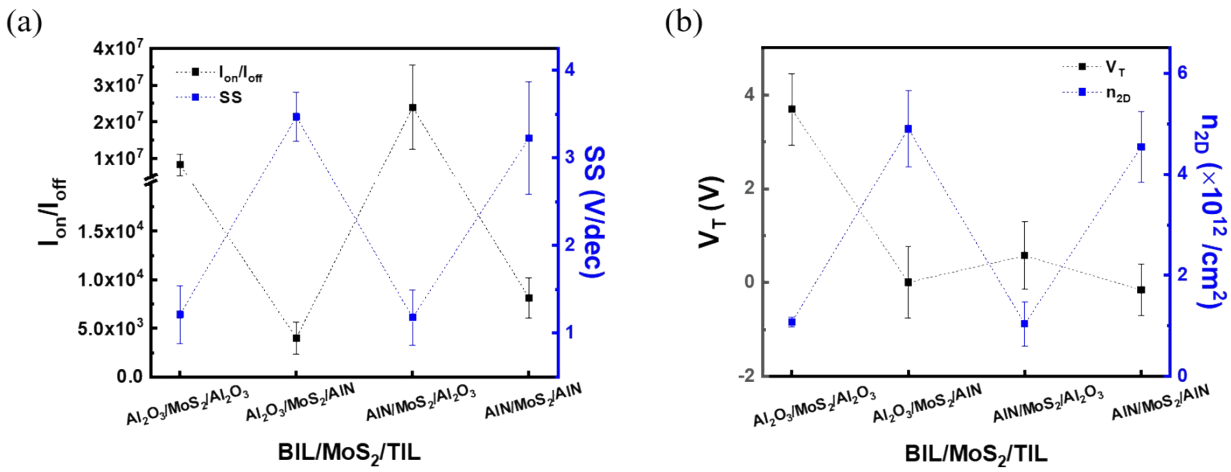


**Figure S9.** Device parameters including (a) $I_{on}/I_{off}$, SS, (b) $V_T$, and $n_{2D}$ extracted from $MoS_2$ FETs with different interfacial layers.

## Figure S10 and S11: Electrical characteristics of graphene FETs with AlN interfacial layers

Graphene exhibits a symmetric energy band structure known as the Dirac cone structure.[7] As graphene has no bandgap, there exists a Dirac point where the electron and hole concentrations are equal, resulting in the smallest current level at this point. In our experimental results, the Dirac point voltage ($V_{Dirac}$) is nearly 0 V, as shown in Figure S10a. However, when the gate bias exceeds the Dirac point voltage, electron conduction is allowed, and when it is below the Dirac point voltage, hole conduction is allowed, with the current increasing in both cases. Figure S11 indicates that $I_{DS}$ increases as the absolute value of $V_{GS} - V_{Dirac}$ increases. However, unlike semiconductor FETs, graphene FETs do not exhibit saturation in the output curves, as shown in Figure S11. As mentioned above, graphene does not exhibit semiconducting properties because there is no bandgap. Consequently, depletion does not occur within the channel near the drain region as in semiconductor FETs, indicating that pinch-off does not occur in the graphene FETs.[8]

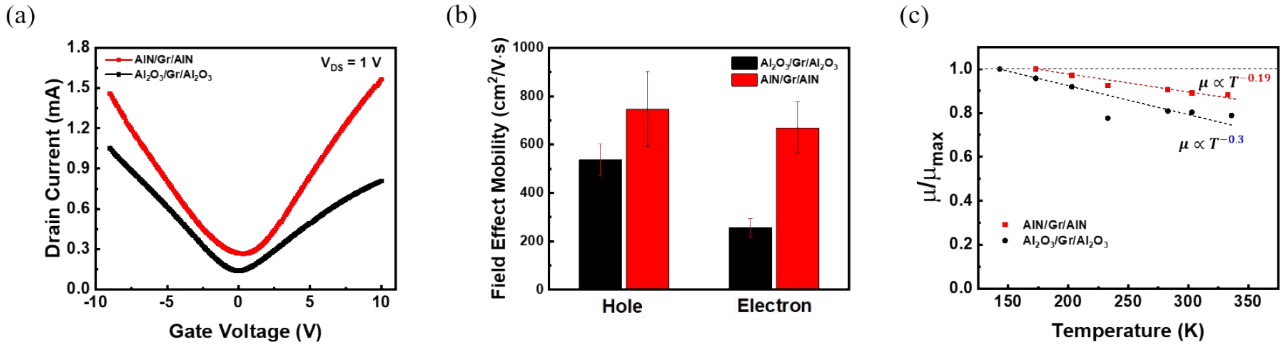


**Figure S10.** (a) Representative transfer curves and (b) field-effect mobility distribution of graphene FETs with AlN sandwich structure and $Al_2O_3$ sandwich structure. (c) Normalized field-effect mobility plots as a function of temperature for $MoS_2$ FETs with different interfacial layers.

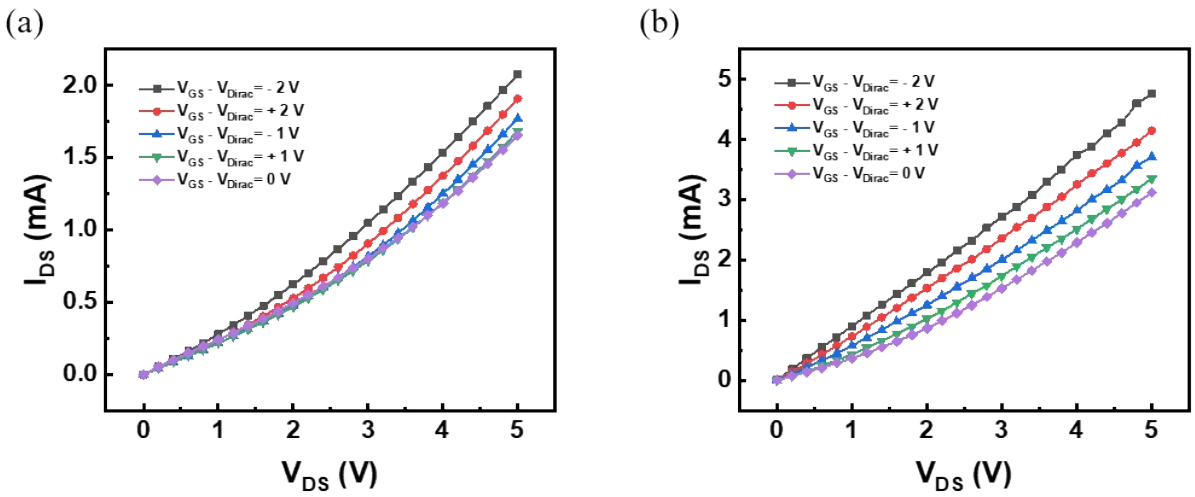


**Figure S11.** Representative output characteristics of graphene FETs with (a) $Al_2O_3$ sandwich structure and (b) AlN sandwich structure ranging from $V_{GS} - V_{Dirac}$ = -2 V to $V_{GS} - V_{Dirac}$ = 2 V (step of 1 V).

# References


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