

## Supporting Information

### **On the grain boundary charge transport in p-type polycrystalline nanoribbon transistors**

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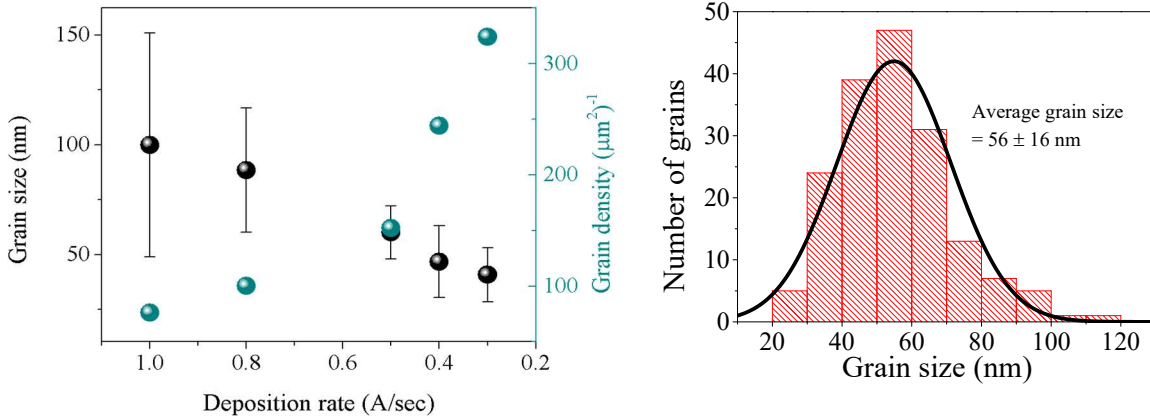
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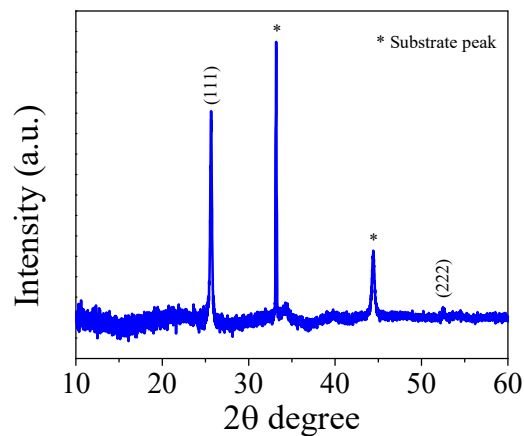
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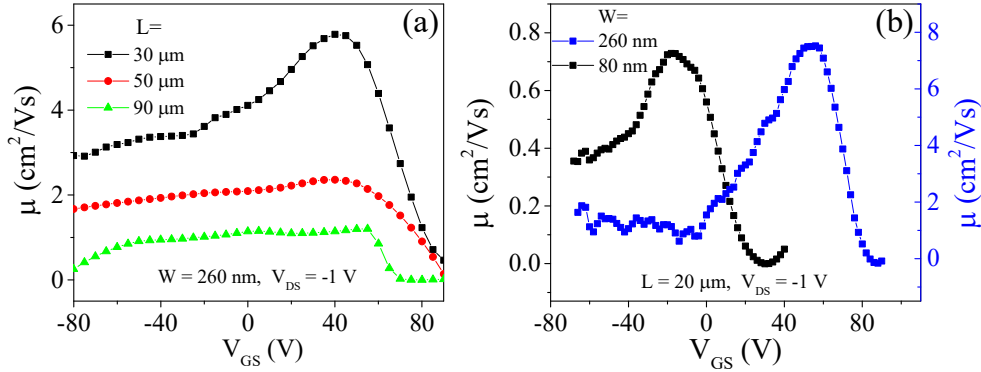
**Figure S1:** (Left) Dependence of grain size on evaporation rate. (Right) Histogram plot of average grain size distribution for CuI PNR.

The Histogram plot is obtained by measuring the average size of each grain using ImageJ software. The average grain size of CuI PNR is  $56 \pm 16$  nm.



**Figure S2:** X-ray diffraction pattern for the CuI PNRs.

The observed diffraction peaks at  $25.65^\circ$  and  $52.48^\circ$  correspond to the (111) and (222) Miller indices of the  $\gamma$ -phase of CuI (JCPDS# 060246), respectively.<sup>1</sup> Additionally, peaks marked with "\*" at  $33.19^\circ$  and  $44.40^\circ$  are attributed to substrate peaks for Si, specifically (200) and (220).

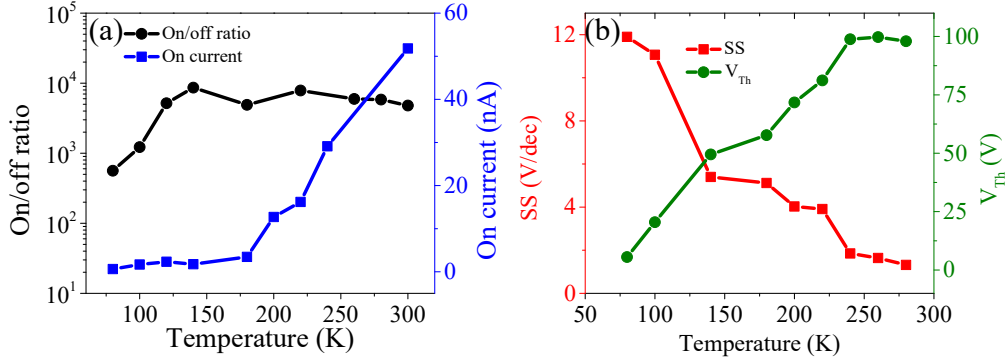


**Figure S3:** Variation of linear mobility over gate voltage for CuI PNR FETs at  $V_{DS} = -1 \text{ V}$ , (a) different channel lengths ( $L$ ) at fixed channel width ( $W$ ), (b) different channel widths ( $W$ ) at fixed channel length.

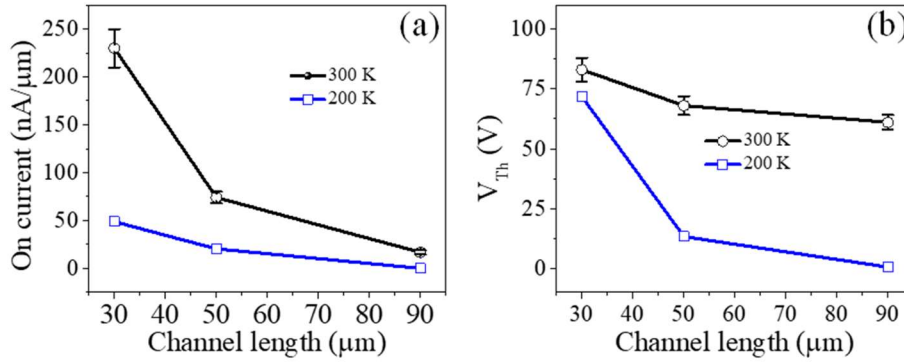
The variation of linear mobility ( $\mu$ ) with channel length ( $L$ ) as a function of gate voltage was investigated, maintaining a fixed channel width of 260 nm and a grain-to-source voltage ( $V_{DS} = -1 \text{ V}$ ) in Figure S3 (a). It is observed that as the channel length decreased, the mobility increased, indicating enhanced trapping carrier transport. In Figure S3 (b), where the channel length is fixed, but the width is varied, the mobility amplitude was higher for a width of 260 nm compared to 80 nm, accompanied by a shift in the threshold voltage ( $V_{th}$ ). This behavior is attributed to the transport characteristics, where the linear mobility variation is higher for shorter channel lengths due to increased carrier trapping, as reported, leading to enhanced conductance in pentacene-based thin film FETs.<sup>2</sup> Conversely, higher channel lengths exhibit reduced mobility as interface traps and charge transfer centers dominate the transport mechanism.<sup>3</sup>

**Table S1:** Electrical characteristics of CuI thin films.

| S. No. | Sample | Resistivity<br>( $\Omega \cdot \text{cm}$ ) | Mobility<br>( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) | Carrier concentrations<br>( $\text{cm}^{-3}$ ) |
|--------|--------|---|---|--|
| 1.     | CuI TF | 0.153                                       | 16.37   | $8.4 \times 10^{17}$                           |

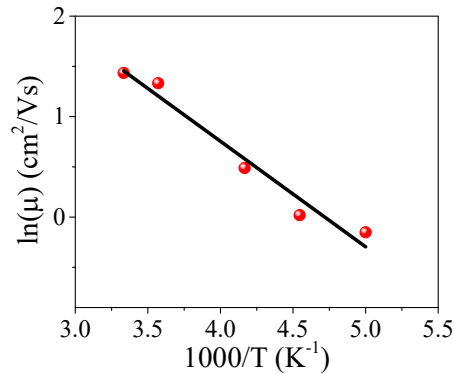


**Figure S4:** Extracted CuI PNR FET parameters variation with temperature for 260 nm width & 30  $\mu\text{m}$  channel at  $V_{DS} = -1V$ , (a) on/off ratio & on current, (b) subthreshold swing & threshold voltage.



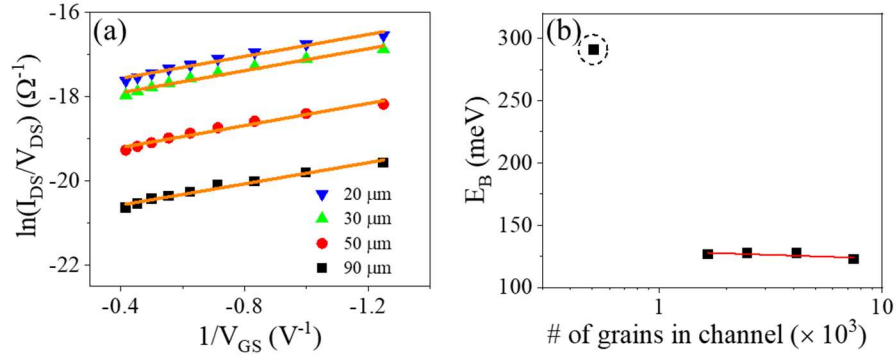
**Figure S5:** CuI PNR FET parameters variation with channel length at different temperatures, (a) on current, (b) threshold voltage at a fixed  $V_{DS} = -1V$ .

The temperature-dependent CuI PNR FETs parameter is shown in Figure S5, with a variation in channel lengths. The on-current, analyzed as a function of channel length at two different temperatures (200K and 300K), exhibits a reduction with increasing channel length in Figure S5 (a). Correspondingly, the threshold voltage ( $V_{Th}$ ), depicted in Figure S5 (b), follows a similar trend.



**Figure S6:** Activation energy extracted from  $\ln(\mu)$  versus  $(1/T)$  for PNR width of 260 nm and length of 30  $\mu\text{m}$ .

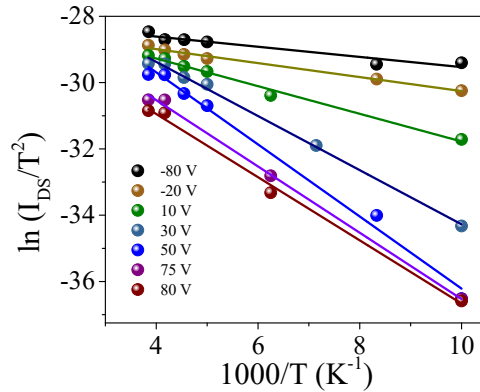
Figure S6 illustrates the calculation procedure for determining the activation energy from the natural logarithm of mobility ( $\ln(\mu)$ ) plotted against the reciprocal of temperature ( $1000/T$ ), specifically for PNRs with a width of 260 nm and a length of 30  $\mu\text{m}$ . This methodology is employed to calculate the activation energy concerning the variation of channel length.



**Figure S7:** (a) Levinson plot of CuI PNR FET at different channel lengths at a  $V_{DS} = -1$  V. (b) Variation of energy barrier height with different number of grains in channel lengths from Levinson's Model.

The Levinson plot, depicting  $\ln(I_{DS}/V_{GS})$  versus  $1/V_{GS}$  for different channel lengths, determines the energy barrier height ( $E_B$ ). Extracted  $E_B$  values and their variation with grains per unit area are presented in Figure S7b.

### Supporting Information Note-1: Temperature-Dependent Analysis of Barrier Height



**Figure S8:**  $\ln(I_{DS}/T^2)$  versus  $1/T$  plot for different gate voltage at fixed  $V_{DS} = -1$  V, for 30  $\mu\text{m}$  channel CuI PNR FET over the temperature range 300-80K.

The barrier height ( $E_B$ ) of CuI PNR FET was analyzed in the temperature range of 80-300 K using the following equation (S1)<sup>4</sup>

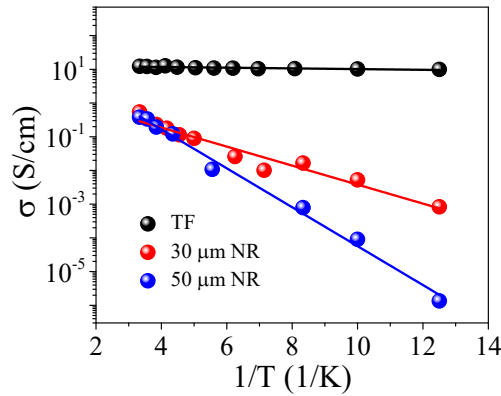
$$I_{DS} = AA^*T^2 \exp\left(-\frac{qE_B}{k_B T} + \frac{qV_{DS}}{k_B T}\right) \quad (S1)$$

Where  $A$  is the device area,  $A^*$  is the modified Richardson constant,  $q$  is the electron charge,  $I_{DS}$  is the drain current,  $k_B$  is the Boltzmann constant,  $T$  is the temperature, and  $V_{DS}$  is the drain voltage. We plotted  $\ln(I_{DS}/T^2)$  versus  $1/T$  at fixed gate voltage and varying drain voltage. Figure S9 shows the plot for 30  $\mu\text{m}$  channel devices at a fixed  $V_{DS} = -1$  V for various gate voltages. From the slope, we derive the barrier height as a function of gate voltage ( $V_{GS}$ ). Furthermore, we converted  $V_{GS}$  into average carrier density according to the relationship in the channel defined by equation (S2)<sup>5</sup>

$$n = C_{OX}(V_{GS} - V_{FB})/q_{ch} \quad (\text{S2})$$

where  $C_{OX}$  is the gate oxide capacitance, and  $V_{FB}$  is the flat band voltage.

### Supporting Information Note-2: Transport Mechanisms in CuI PNRs and Thin Films:



**Figure S9:** Conductivity fitting comparison with respect to the temperature for CuI thin film and PNR at zero gate bias condition.

The Arrhenius plot presented in Figure S9 describes the temperature-dependent conductivity profiles spanning from 300 to 80 K for both CuI thin films and PNRs of various lengths. A noticeable trend emerges, showcasing a more pronounced decline in conductivity for the CuI PNRs compared to the thin film, which indicates different transport mechanisms. Notably, the obtained activation energies are 2, 56, and 115 meV for the CuI thin film, PNR (30  $\mu\text{m}$ ), and PNR (50  $\mu\text{m}$ ), respectively, underscoring a heightened activation energy for electrical conductivity in CuI PNRs.<sup>6,7</sup> Therefore, CuI thin film demonstrates a thermally activated charge transport behavior. Considering the observed interface trap density at grain boundaries from previous analyses, we anticipate the manifestation of a distinctive charge transport mechanism in CuI PNRs.

To elucidate the conductivity mechanism, we employ the temperature dependence of conductivity and apply the 3D-Variable Range Hopping (VRH) model to both CuI PNR and thin film. The 3D-VRH model provides a framework for understanding hopping conductivity, as expressed by Equation (S3):

$$\sigma = \sigma_0 \exp[-(T_0/T)^{1/4}] \quad (\text{S3})$$

Where  $\sigma_0$  represents the pre-exponential factor and  $T_0$  denotes the degree of disorder. These are expressed as follows:

$$\sigma_0 = e^2 a^2 v_{ph} N(E_F) \quad (S4)$$

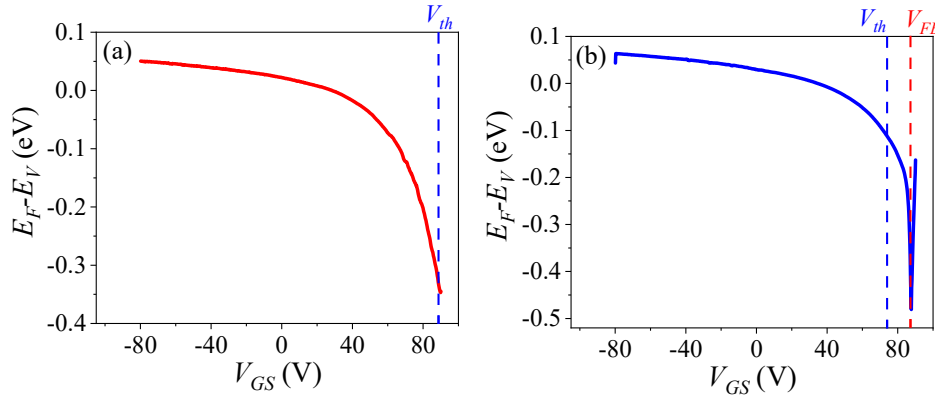
$$\text{and } T_0 = c^4 \gamma^3 / k N(E_F) \quad (S5)$$

In these equations,  $e$  represents the electronic charge,  $a$  is the hopping distance,  $v_{ph}$  is the phonon frequency ( $\sim 10^{13} \text{ sec}^{-1}$ ) obtained from the Debye temperature,  $N(E_F)$  is the localized density of states near the Fermi level,  $k$  is Boltzmann's constant,  $\gamma$  is the inverse of the localization length ( $\zeta$ ), and  $c$  is a dimensional constant based on the percolation parameter. Here,  $N(E_F)$  value is extracted from  $T_0$ . The other two parameters,  $R$  (the hopping distance) and  $W$  (the hopping energy) are determined by the equations:

$$R = [9/8\pi\gamma k T N(E_F)]^{1/4} \quad (S6)$$

$$\text{and } W = [3/4\pi R^3 N(E_F)] \quad (S7)$$

### Supporting Information Note-3: Correlation Between Gate Voltage and Fermi Level in CuI PNR FET:



**Figure S10:** Relation between  $V_{GS}$  and  $E_F - E_V$  of CuI PNR FET for (a) 30  $\mu\text{m}$  and (b) 50  $\mu\text{m}$  channel.

Additionally, the relationship between the gate voltage and the Fermi level of CuI PNR can be correlated using a mapping function equation (S8)<sup>8</sup>

$$E_F - E_V = 2kT \ln \left( \frac{I_D(V_G)}{\sqrt{N_V \epsilon_S k T} \mu (W/L) V_D} \right) \quad (S8)$$

Here,  $T$  is the absolute temperature,  $k$  is the Boltzmann constant,  $\mu$  is the hole mobility, and  $\epsilon_s$  is the permittivity,  $E_V$  valence band maximum, while  $N_V$  denotes the effective density of states for free carriers, defined as  $2(2\pi m_h^* kT/h^2)^{3/2}$ , where  $m_h^*$  is the effective mass of holes, and  $h$  is Plank's constant. For CuI,



the calculated  $N_V$  is  $9.3 \times 10^{19} \text{ cm}^{-3}$ , using  $m_h^* = 2.4m_0$  at  $T=300\text{K}$  ( $m_0$  is the electronic rest mass).<sup>9,10</sup> Equation (S8) indicates that  $E_F - E_V$  as function of the gate voltage, reflecting the extent of band bending. Based on this equation, we calculate the correspondence of  $V_{GS}$  with  $E_F - E_V$  of CuI PNR FET at room temperature (300K), as shown in Figures S11a and S11b for  $L = 30$  and  $50 \mu\text{m}$  channels, respectively.

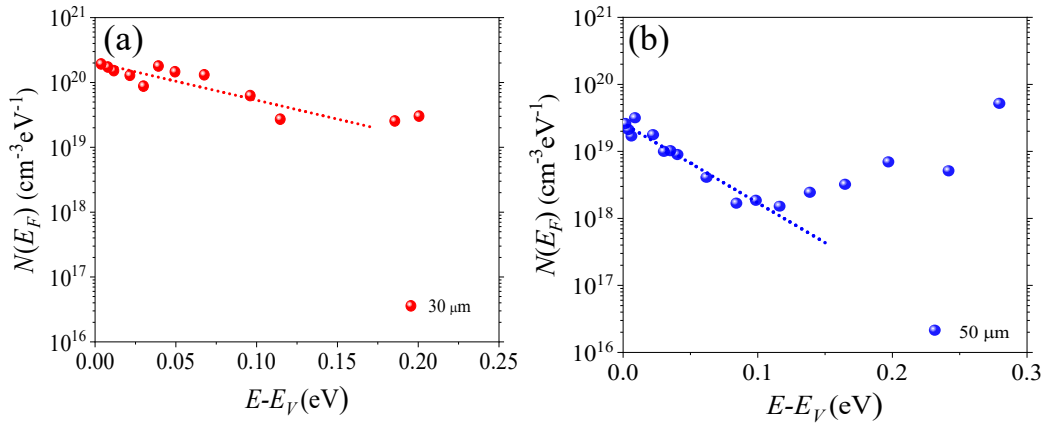
#### Supporting Information Note-4: Analytical Modeling of Carrier Density and Electrical Surface Potential:

The trapping carrier density ( $n_{tr}$ ) and free carrier density ( $n_{fr}$ ) are associated with the electrical surface potential of the semiconductor, which is determined using equation (S9) and Poisson's equation (S10),

$$n_{free}(V_{GS}) = \frac{1}{\epsilon_s kT} \left( \frac{L I_{DS}(V_{GS})}{\mu W V_{DS}} \right) \quad (\text{S9})$$

$$\frac{d^2 \phi_s}{dx^2} = \frac{q}{\epsilon_s} (n_{tr} + n_{fr}) \quad (\text{S10})$$

$$E = \frac{d\phi_s}{dx} \quad (\text{S11})$$



**Figure S11:** The density of the localized states as a function of the Fermi energy level is calculated from the trapping conduction density of the channel (a)  $30 \mu\text{m}$  and (d)  $50 \mu\text{m}$ .

Also, the electrical surface potential of p-type semiconductors ( $\phi_s$ ) is defined as equation (S12),

$$\phi_s = \frac{2kT}{q} \ln \left( \frac{I_{DS}^2(V_{GS})}{\epsilon_s kT \mu^2 \frac{W}{L} V_{DS}} \right) + \left( \frac{E_V - E_{F0}}{q} \right) \quad (\text{S12})$$

where  $E$  represents the electric field,  $\varphi_s$  signifies the surface potential along the depth,  $x$  denotes the distance from the dielectric/semiconductor interface along with the channel depth, and  $E_{F0}$  denotes the intrinsic Fermi level position of CuI.

The relationship between the carrier density and the gate voltage is determined using the charge balance equation  $Q_{ind} = C_{ox}(V_G - V_{TH})$ , where  $V_{TH}$  represents the threshold voltage,  $C_{ox}$  signifies the capacitance of the semiconductor/dielectric interface and  $Q_{ind}$  denotes the total charge density induced at the interface. The induced electric field at  $x=0$ , one of the parameters controlling the charge carrier density by gate voltage, can be computed using equations (S10) and (S11),

$$E(x = 0) = \sqrt{\frac{2q}{\epsilon_s} \int_0^{\varphi_s} (n_{tr} + n_{fr})} \approx \frac{C_{ox}(V_G - V_{TH})}{\epsilon_s} \quad (S13)$$

By taking the first derivative of equation (S13) with respect to  $\varphi_s$ , which is linearly dependent on the total carrier density. The surface potential is defined as  $q\varphi_s = (E_{F0} - E_F)$ , where  $E_{F0}$  is the equilibrium position of the Fermi level.

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