

SUPPLEMENTARY INFORMATION

First demonstration of 2T0C-FeDRAM: a-ITZO FET and double gate a-ITZO/a-IGZO FeFET with record-long multibit retention time of > 4-bit and > 2000 s

Tae Hyeon Noh,^{†a} Simin Chen,^{†a} Hyo-Bae Kim,^b Taewon Jin,^a Seoung min Park,^a Seong Ui An,^a Xinkai Sun,^a Jaekyun Kim,^a Jae-Hoon Han,^d Ji-Hoon Ahn,^{*b} Dae-Hwan Ahn,^{*d} and Younghyun Kim^{*a}

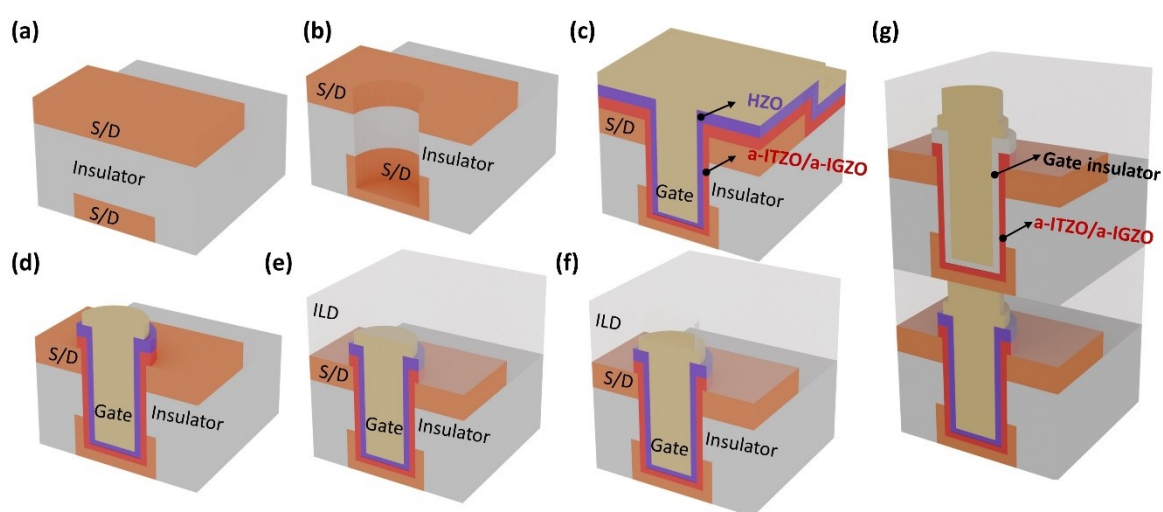


Fig. S1. Process flow of one channel all around (CAA) structure 3D 2T0C-FeDRAM cell (The 3D 2T0C-DRAM process was proposed by Duan *et al.*¹ Here, the main differentiation is the introduction of the ferroelectrics of HZO after channel formation as a gate insulator.) (a) MIM structure deposited by S/D spacer and top electrode in sequence after bottom electrode formation, (b) channel region etching, (c) gate stack deposition by ALD in sequence (R_{1r} gate stack: a-ITZO/a-IGZO/HZO/gate electrode, W_{1r} gate stack: a-ITZO/gate insulator/gate electrode), (d) active region isolation (e) Inter-Layer dielectric (ILD) deposition, (f) ILD etching, (g) After the lower R_{1r} is completed, the upper W_{1r} repeats the same process.

^a Department of Photonics and Nanoelectronics, BK21 FOUR ERICA-ACE Center, Hanyang University, Ansan 15588, Korea.

^b Department of Materials Science and Chemical Engineering, Hanyang University, Ansan, Republic of Korea

^c Korea Institute of Science and Technology, Seoul, Republic of Korea

[†] Both authors equally contributed to this work.

* Corresponding authors

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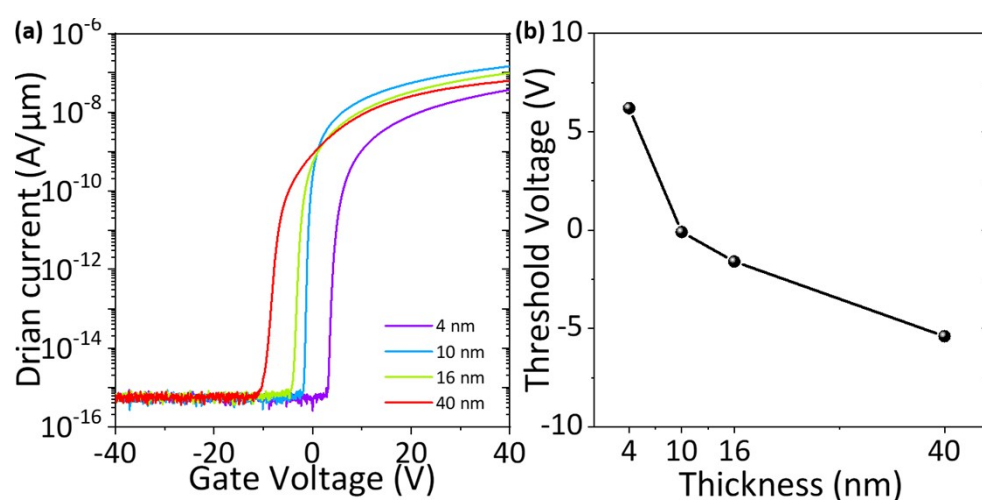


Fig. S2. (a) Transfer characteristics of a-ITZO (4, 10, 16, and 40 nm-thickness) FETs. (b) Thickness dependence of threshold voltage for a-ITZO TFTs.

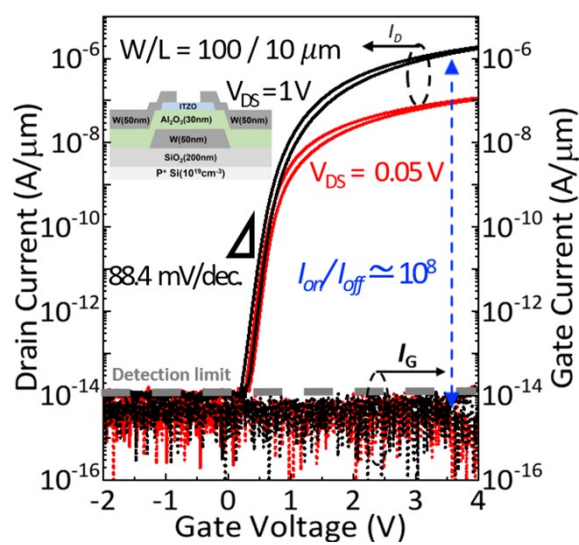


Fig.S3. $I_D - V_G$ characteristics of the write a-ITZO FET. Utilizing high mobility near $25.5 \text{ cm}^2/\text{V s}$ and low leakage current attributes of a-ITZO, a low S.S. value of 88.4 mV/dec. and an off current below $10^{-14} \text{ A}/\mu\text{m}$ were achieved, making it suitable as a write transistor (W_{IT}) for 2T0C-FeDRAM.

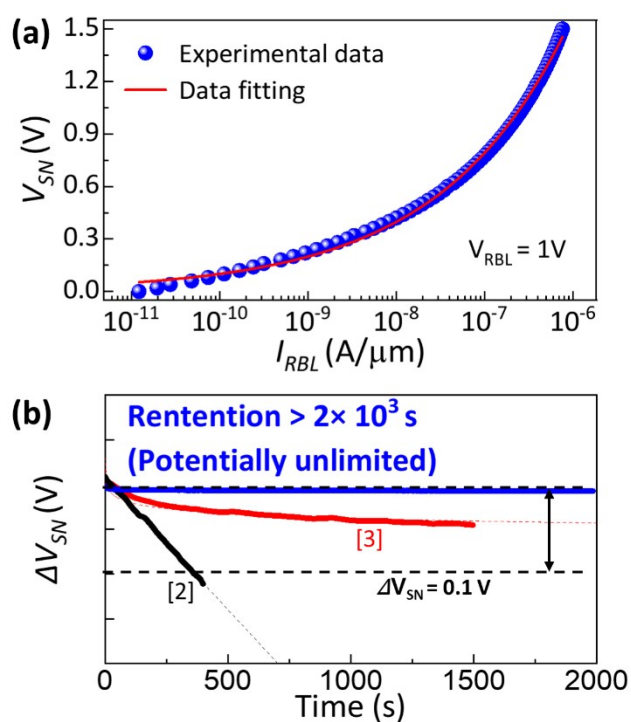


Fig. S4. (a) Data fitting of V_{SN} - I_{RBL} detected during the 2T0C-FEDRAM read operation, V_{SN} can be extracted. (b) V_{SN} changes vs. time, indicating that the excellent retention time. I_{RBL} was maintained almost without the voltage dropping for a period of 2000 s.^{2,3}

Notes and references

1. X. Duan, K. Huang, J. Feng, J. Niu, H. Qin, S. Yin, G. Jiao, D. Leonelli, X. Zhao and Z. Wang, *IEEE Trans. Electron Devices*, 2022, **69**, 2196-2202, DOI: <http://dx.doi.org/10.1109/TEDE.2022.3154693>.
2. A. Belmonte, H. Oh, N. Rassoul, G. Donadio, J. Mitard, H. Dekkers, R. Delhougne, S. Subhechha, A. Chasin and M. Van Setten, presented in part at the 2020 IEEE International Electron Devices Meeting (IEDM), 2020.
3. K. Chen, Z. Zhu, W. Lu, M. Liu, F. Liao, Z. Wu, J. Niu, B.-M. Kang, W. Dan and X.-S. Wu, presented in part at the 2023 International Electron Devices Meeting (IEDM), 2023.

