Supplementary Information (SI) for Nanoscale.
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Supporting Information

DC Field-biased Multibit/Analog Artificial Synapse Featuring an Additional Degree of Freedom for Performance Tuning

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Section S1. The structure of the device

TiO_2 layers are grown on 10 mm × 10 mm × 0.05 mm Ti chips by thermal oxidation at 700 °C in air for 60 min. Top electrodes are 1 mm × 1mm titanium thin film pads made by thermal evaporation of titanium in vacuum using a 4×4 matrix stainless steel mask. The photograph of the resulted Ti/TiO_2/Ti chip, including 16 memory devices, is shown in Figure S1a. Figure S1b shows the schematics of a single cell with plan view (i) and the cross-sectional (ii) SEM micrograph given as insets.

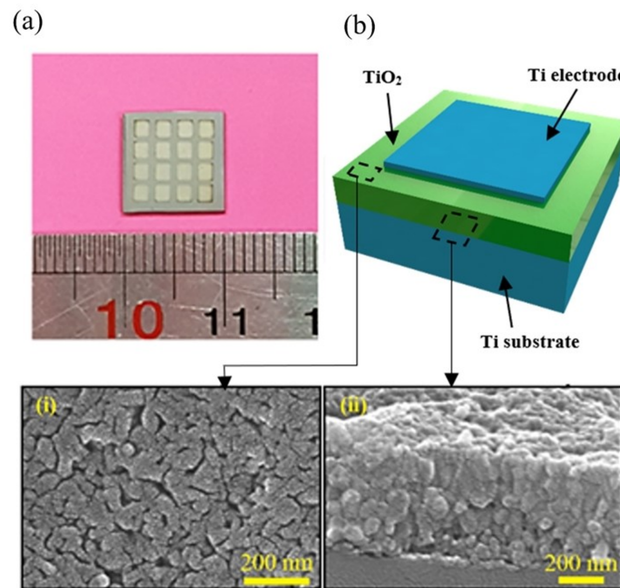

Figure S1. (a) Photograph of the Ti/TiO2/Ti samples fabricated on a thermally oxidized titanium foil, and (b) the schematic diagram of a single memory device; the plan view (i) and the cross-sectional (ii) SEM micrographs of the oxide layer are given as insets.

Section S2. Measurement system used for electrical characterizations

The block diagram of the I-V recording system is shown in Figure S2a. This system is utilized for the electrical characterization of the fabricated memory cells. A photograph of the sample under test is given as Figure S2b.

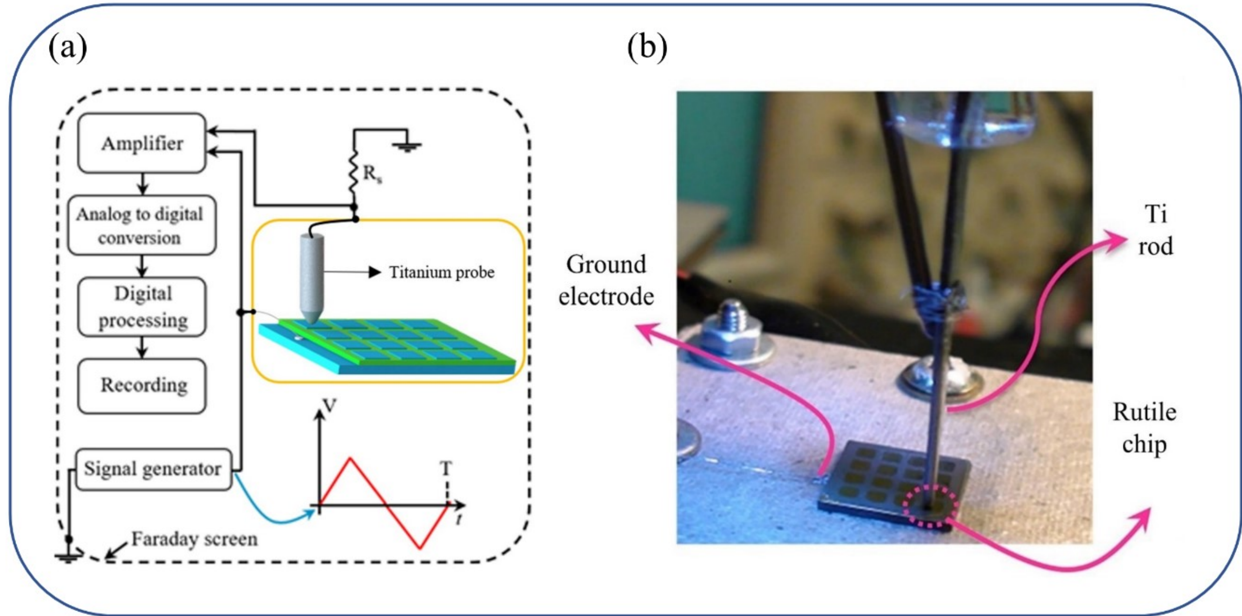

Figure S2. (a) The block diagram of the experimental setup utilized for the I-V measurements, and (b) a photograph of the fabricated device placed on the stage of a x-y-z micromanipulator for electrical characterization.

Section S3. Determining the optimum DC bias range

The optimization process is carried out graphically based on the shape evolution observed on the I-V plots as a result of different DC biasing voltages. The optimum biasing voltage (V_{DC}) for the fabricated Ti/TiO_2/Ti memory cells with the geometrical specifics given in Figure S1b is determined by recording the I-V plots of a device at different biasing voltages. In this method, different V_{DC} are added to the ±1.5 V AC voltages with different frequencies and applied to the device for I-V plotting. The results of this systematic variations are presented in Figures S3 and S4. At f= 40 Hz, the biasing voltage range of 0.7-1.3 V appears to be the most suitable biasing range for the operation of the produced memristive devices; in this condition the device presents its high and low resistance states most distinctly.

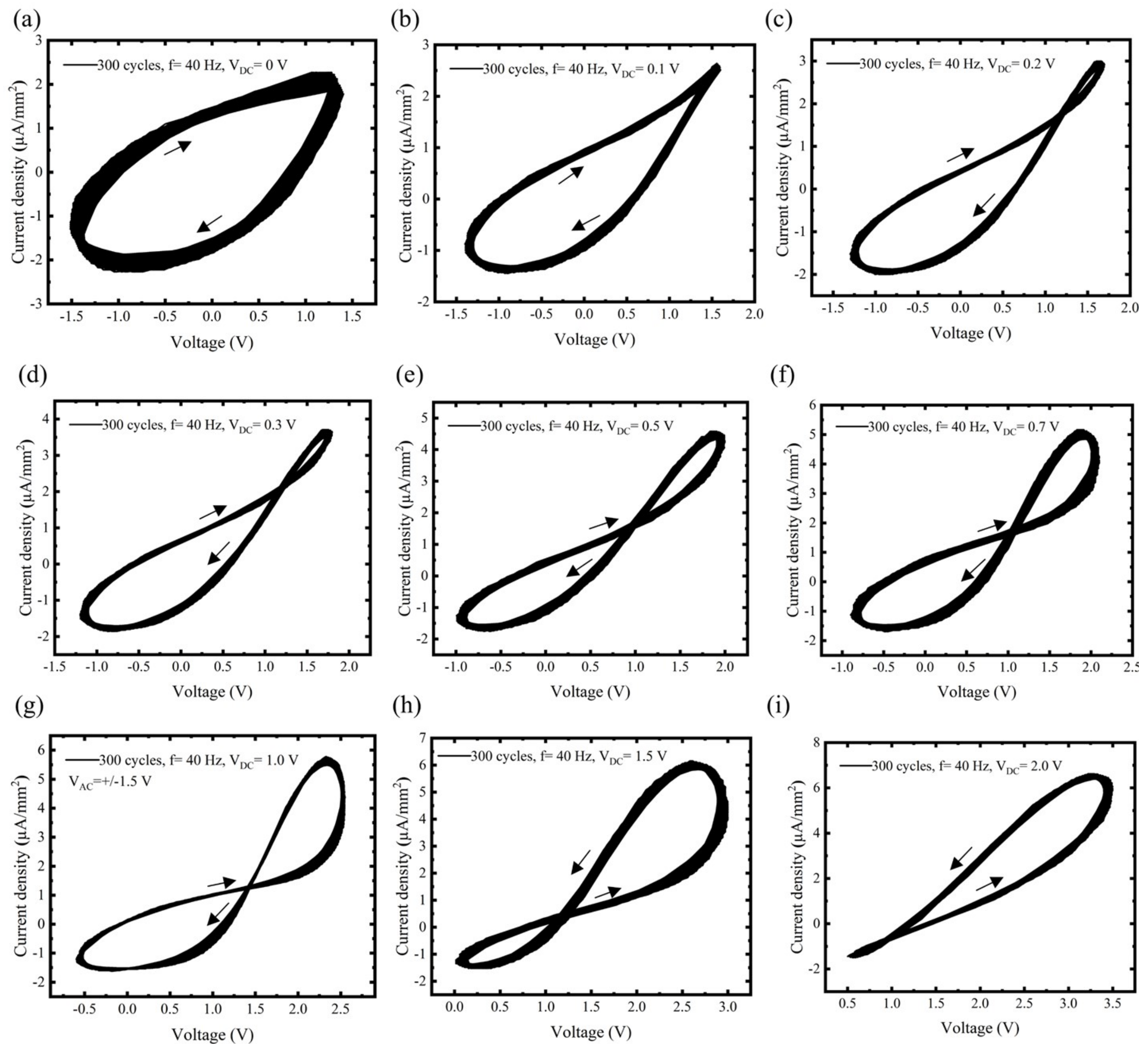

Figure S3. (a)-(i) The I-V plots evolution due to the stated DC biasing voltages, recordings are carried out by utilizing an AC voltage of +/-1.5 V at 40 Hz for voltage sweeping.

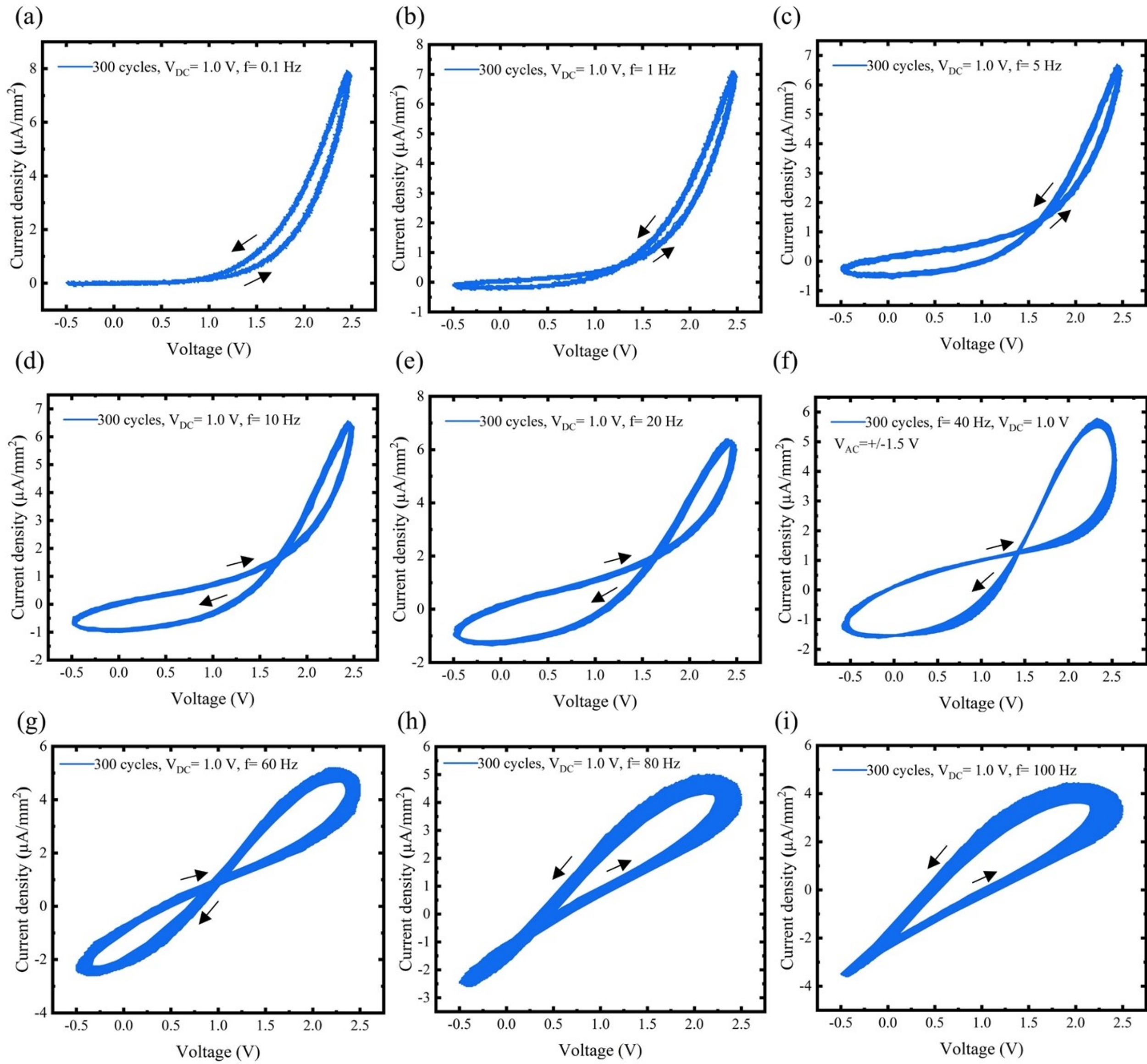

Figure S4. (a)-(i) The deformation of the I-V plots of a 1.0 V biased device due to the variation of the voltage sweeping frequencies; graphically the frequency range of 30 to 60 Hz is determined to be suitable for the device tests.

Section S4. Long-term stability of a fabricated memory cell

The long-term stability of a DC-biased memory cell is examined by monitoring its synaptic weight continuously during 8 h after receiving the write signal. The monitoring process involves reading of the current passing through the device placing no extra load on the synapse. The results (Figure S5) show the stability of the synaptic weight (ΔI in Figure S5) during the monitored period. Similar experiments are carried out for 4 V and 6 V write signals causing, respectively, lower and higher stable synaptic weights than the ΔI shown in Figure S4. These thin film TiO_2 memory cells can retain the level of the applied write voltages for more than 8 h.

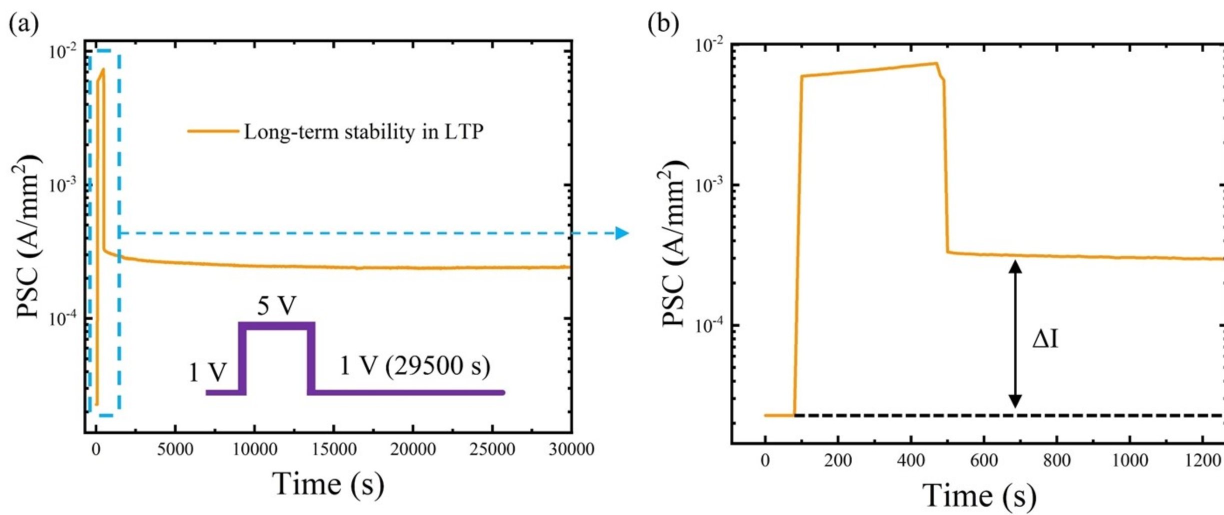

Figure S5. (a) The long-term stability of the device after receiving a write pulse, and (b) demonstrating the current variations just after the write action by utilizing a magnified time scale.

Section S5. LTP and LTD in STDP function

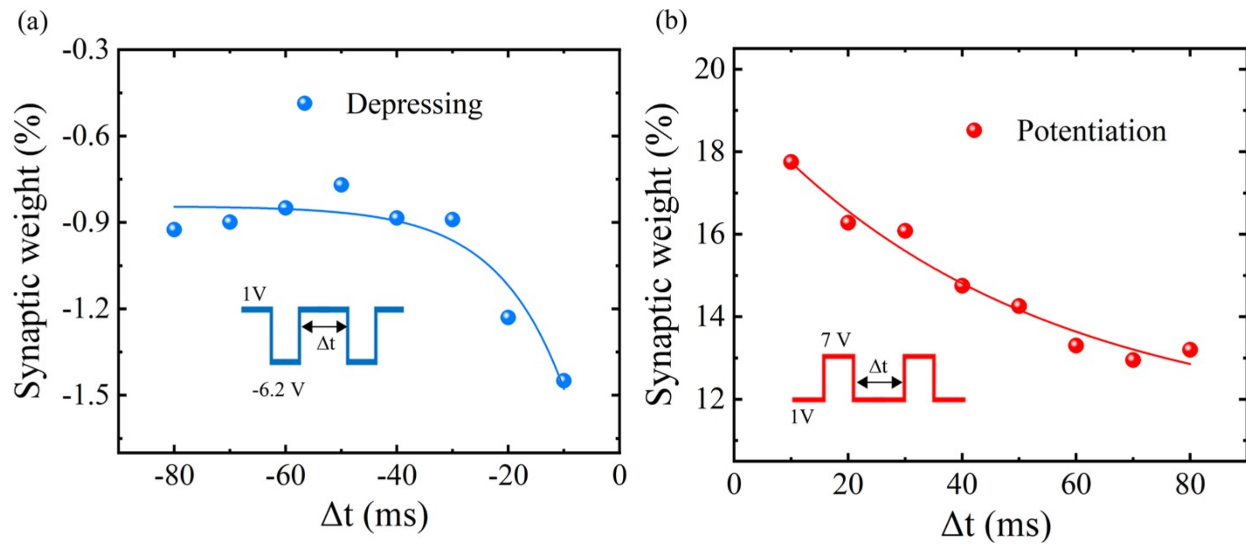

Figure S6. Spike-timing-dependent plasticity obtained experimentally for the fabricated memristor; (a) depressing and (b) potentiation.