Supplementary Information (SI) for Nanoscale.
This journal is © The Royal Society of Chemistry 2024

Supplementary Information

Crystallization Control of Cu(I)-Halide via Thermal Evaporation for Improving Resistive Switching Memory Performance

SangMyeong Lee,[‡a] Bong Ki Hong,[‡a] Sang-Uk Lee,[b] Jong-In Huh,[a] Geon Woo Yoon,[a] Nam-Gyu Park[b,c] and Hyun Suk Jung[*a,c]

[a] School of Advanced Materials Science & Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea

[b] School of Chemical Engineering, Center for Antibonding Regulated Crystals, Sungkyunkwan University, Suwon 16419, Republic of Korea

[c] SKKU Institute of Energy Science and Technology (SIEST), Sungkyunkwan University, Suwon 16419, Republic of Korea

Corresponding Authors

*H. S. Jung E-mail: hsjung1@skku.edu

KEYWORDS: halide materials, physical vapor deposition, crystallization, trap density, resistive switching

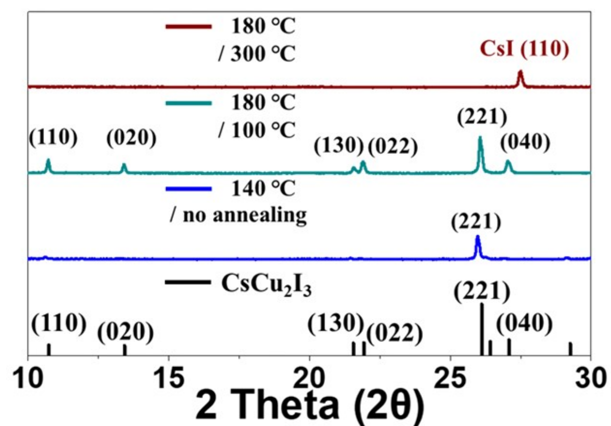

Fig. S1 XRD patterns of $CsCu_2I_3$ thin film as a function of deposited substrate temperature (Black line – $CsCu_2I_3$ PDF#77-0069, blue line - deposited at 140 °C and no annealing, cyan line - deposited at 180 °C then annealed at 100 °C, and wine line - deposited at 180 °C then annealed at 300 °C).

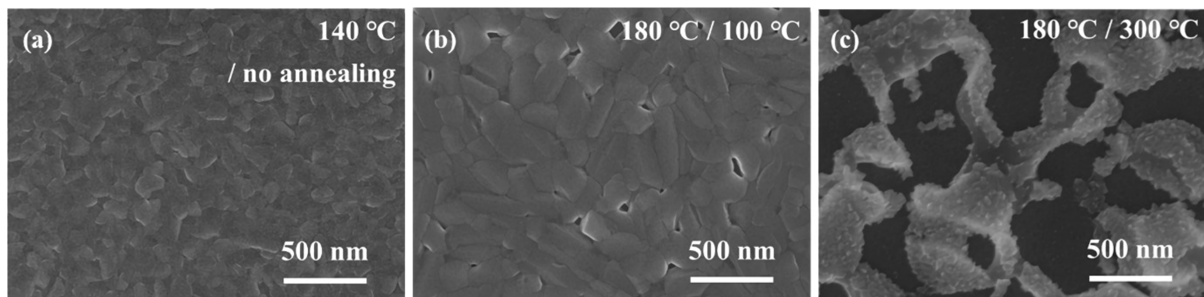

Fig. S2 (a-c) Plane SEM images of $CsCu_2I_3$ thin film as a function of substrate temperature during deposition process and post-annealing temperature. (a) deposited at 140 °C and no annealing, (b) deposited at 180 °C then annealed at 100 °C, and (c) deposited at 180 °C then annealed at 300 °C.

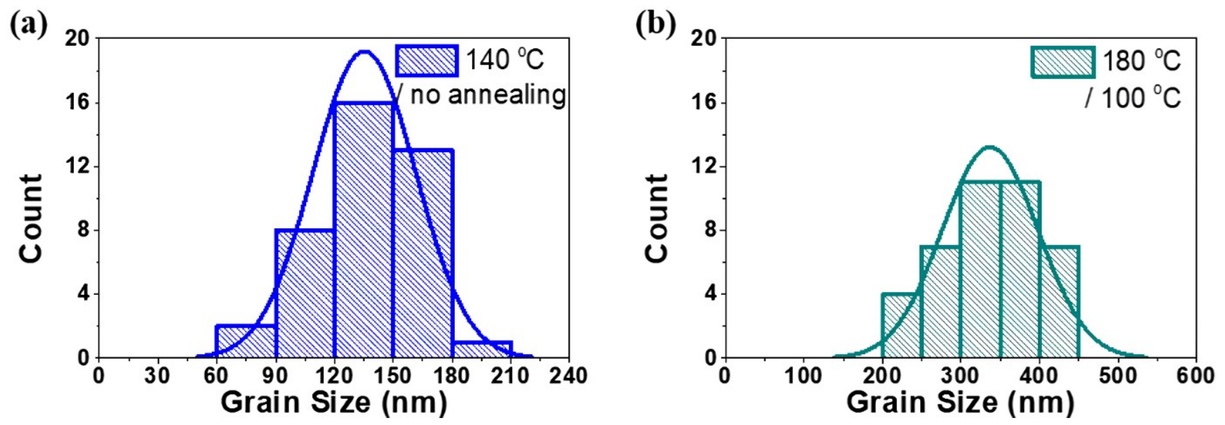

Fig. S3 (a,b) Histogram graph of grain size of $CsCu_2I_3$ thin films a function of substrate temperature during deposition process and post-annealing temperature. (a) deposited at 140 °C and no annealing, and (b) deposited at 180 °C then annealed at 100 °C.

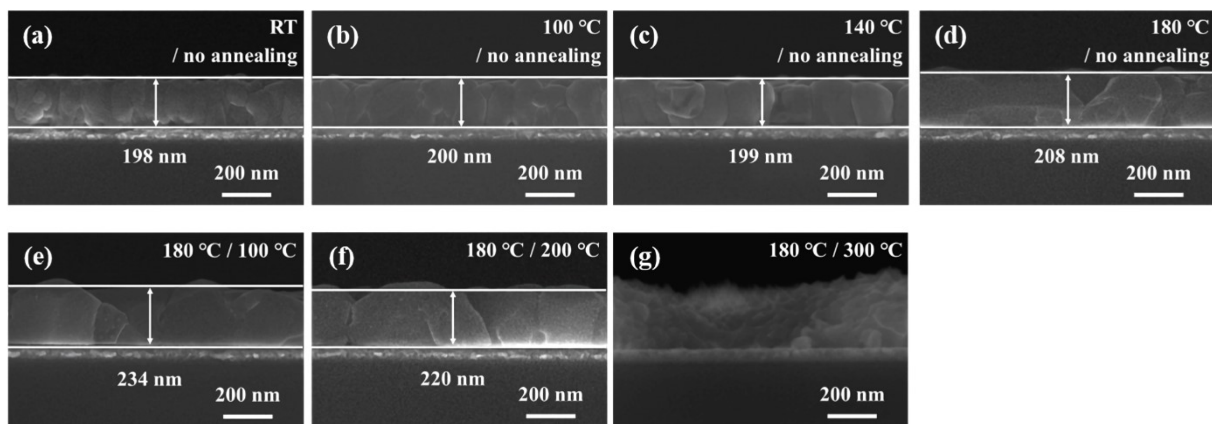

Fig. S4 (a-g) Cross-sectional SEM images of $CsCu_2I_3$ thin film as a function of substrate temperature during deposition process and post-annealing temperature. (a) Deposited at RT and no annealing, (b) deposited at 100 °C and no annealing, (c) deposited at 140 °C and no annealing, (d) deposited at 180 °C and no annealing, (e) deposited at 180 °C then annealed at 100 °C, (f) deposited at 180 °C then annealed at 200 °C, and (g) deposited at 180 °C then annealed at 300 °C.

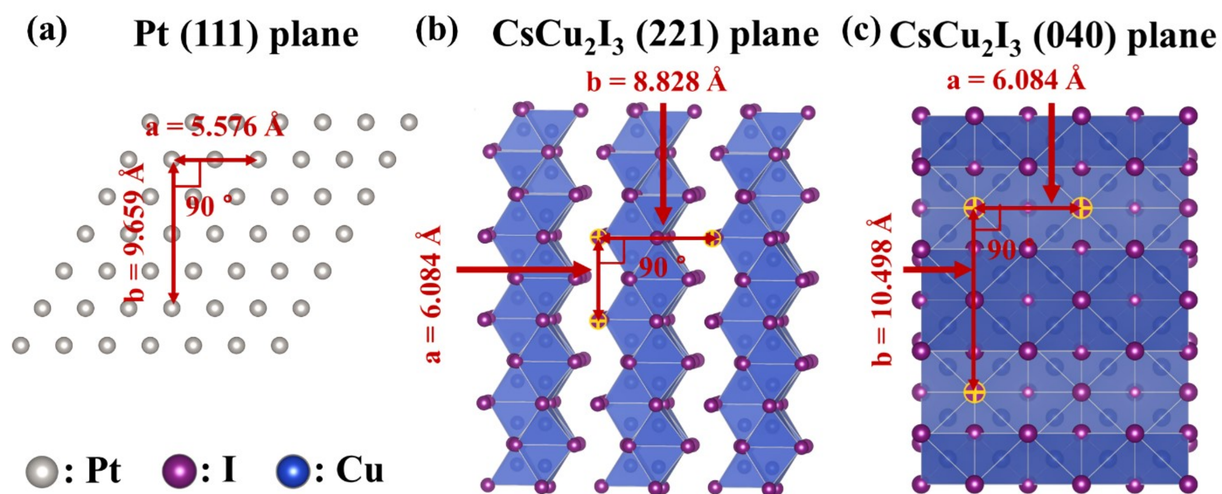

Fig. S5 (a-c) Schematic two-dimensional lattice illustration on (a) the (111) crystal plane of Pt, (b) the (221) crystal plane of $CsCu_2I_3$, and (c) the (040) crystal plane of $CsCu_2I_3$ with Cs^+ hidden for conciseness.

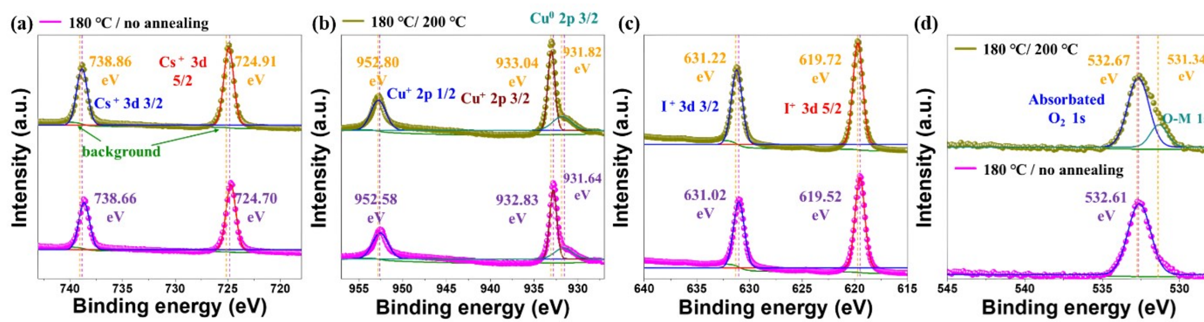

Fig. S6 High-resolution XPS spectra of (a) Cs 3d, (b) Cu 2p, (c) I 3d, and (d) O 1s for $CsCu_2I_3$ thin film under deposited at 180 °C (magenta) and post-heat treated at 200 °C (dark yellow).

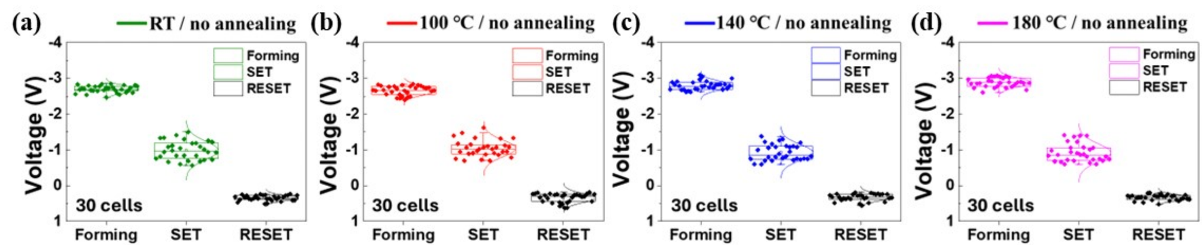

Fig. S7 (a-d) The average forming, set and reset voltages of of $CsCu_2I_3$ thin film measured across 30 samples as a function of deposited substrate temperature. (a) Deposited at RT and no annealing, (b) deposited at 100 °C and no annealing, (c) deposited at 140 °C and no annealing, and (d) deposited at 180 °C and no annealing.

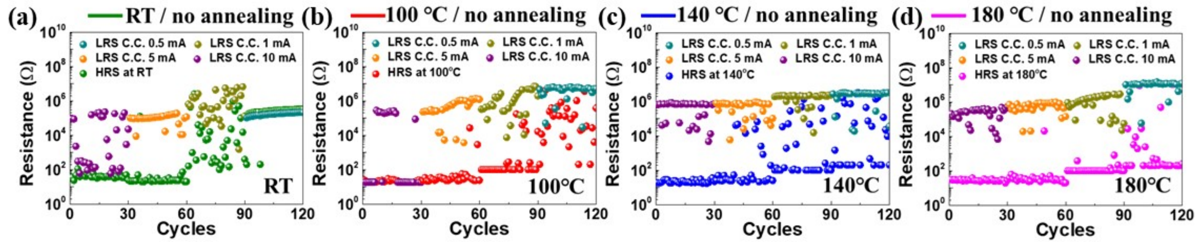

Fig. S8 (a-d) resistive switching multi-level DC endurance property measured with the DC pulses (set pulse voltage -1 V and duration 640 µs, reset pulse voltage 1 V and duration 640 µs and read pulse voltage - 0.1 V and duration 640 µs, purple – 10 mA of C.C., orange – 5 mA, dark yellow – 1 mA, and cyan – 0.5 mA). (a) Deposited at RT and no annealing, (b)- deposited at 100 °C and no annealing, (c) deposited at 140 °C and no annealing, and (d) deposited at 180 °C and no annealing.

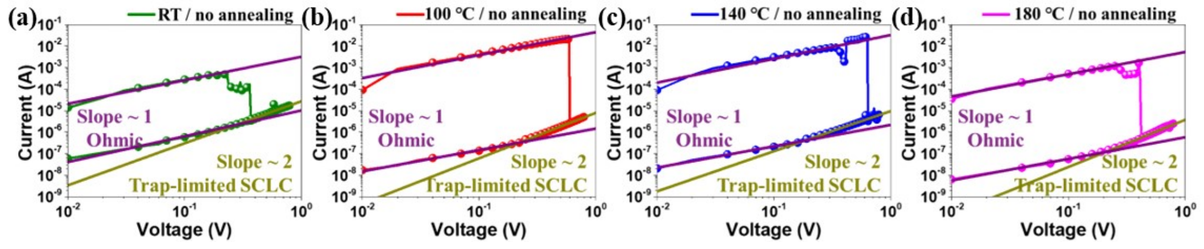

Fig. S9 (a-d) Logarithmic $I-V$ characteristics of $CsCu_2I_3$-based RS devices as a function of deposited tempeature for conduction mechanism at reset process (Purple line is the ohmic region with slope 1, and dark yellow line is the trap-limited SCLC region with slope 2). (a) Deposited at RT and no annealing, (b) deposited at 100 ^oC and no annealing, (c) deposited at 140 ^oC and no annealing, and (d) deposited at 180 ^oC and no annealing.