Supporting Information

Constant voltage driving current oscillation in the artificial graphene ribbon with deterministic chiral edges

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Fabrication processes of the sample

The fabrication processes of sample for the I-V measurement is schematically shown in Fig. S1. Firstly, a 150nm aluminum is deposited on the back of the sample as the bottom-gate electrode after the growth of the Si/GeSi heterostructure. Then two electrodes on the sample surface are fabricated by optical lithography and the subsequent thermal evaporation of 150 nm aluminum, as shown in Fig. S1(i). A rapid thermal annealing at 520 °C for 2 min in the forming gas is performed to realize the ohmic contact between the electrodes and Si. Secondly, a soft mask of PMMA with nanoholes in a honeycomb lattice is obtained by electron beam lithography in the area of 100μm × 40μm between the electrodes on the sample surface. A 10 nm Au layer is deposited by electron beam evaporation. After a lift-off process, Au nano-disks (NDs) in a honeycomb lattice are obtained on the sample surface, as shown in Fig. S1(ii). Thirdly, the Si/GeSi heterostructure beside the Au NDs pattern area and the electrodes is etched away by optical lithography and the plasma etching, as shown in Fig. S1(iii). Finally, the Au NDs pattern area is capped by a 100nm SiO_2 layer via optical lithography and chemical vapor deposition. Then 10 nm Cr and 120 nm Au are deposited on the surface of the SiO_2 layer as a top-gate electrode by optical lithography and the subsequent electron beam evaporation, as shown in Fig. S1(iv).

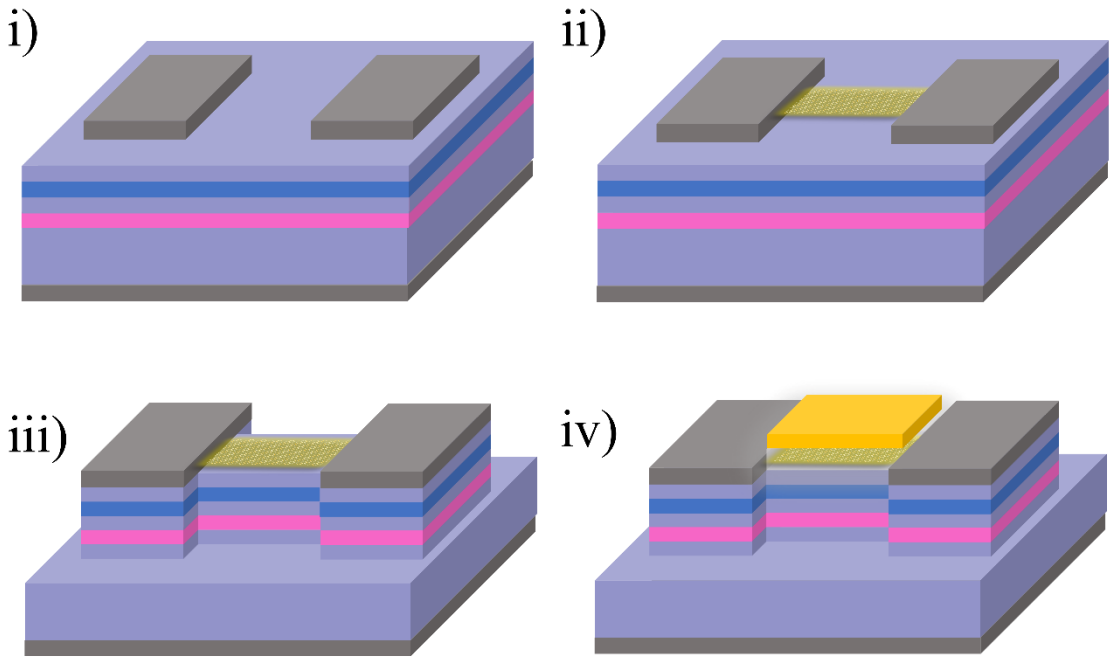

Fig. S1 The schematic diagram of the fabrication processes of sample for the I-V measurement.