Supplementary Information

Silicon nanowire-incorporated efficient and flexible PEDOT:PSS/silicon hybrid solar cells

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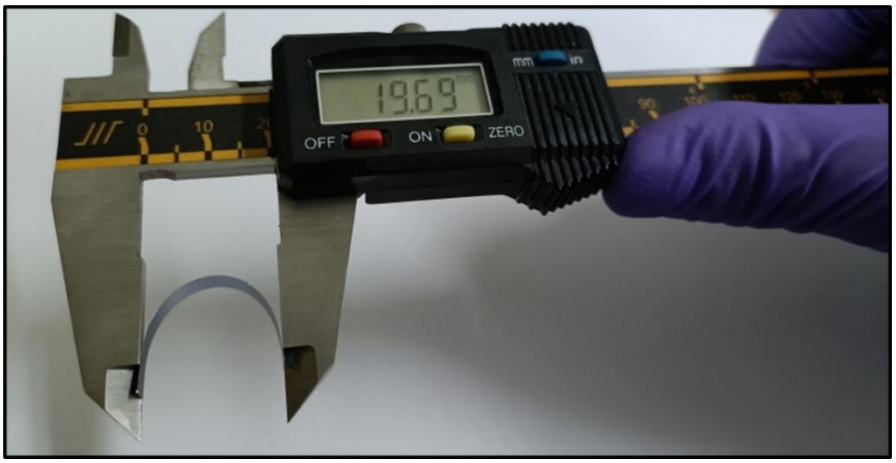

Figure S1. Digital image of 50 μm thin c-Si wafer showing a bending radius of ~10 mm.

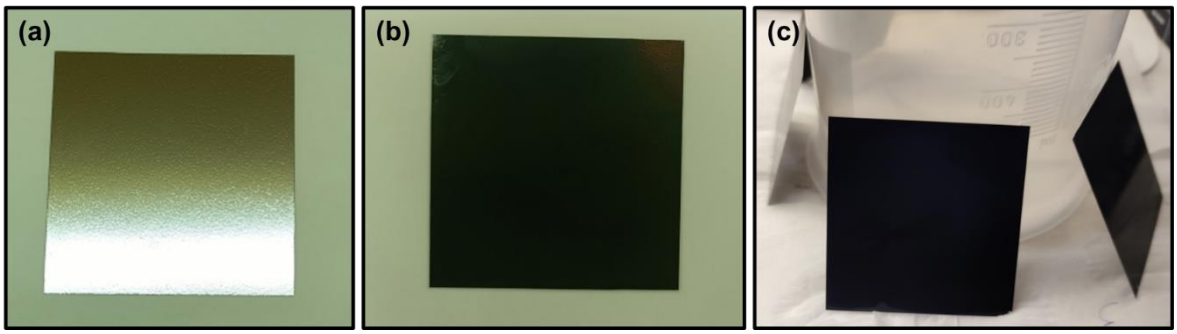

Figure S2. Digital image of thin Si wafers **(a)** planar, **(b)** 90s etched SiNW, **(c)** prepared 4.5 × 4.5 cm^2 black Si wafers for solar cell fabrication.

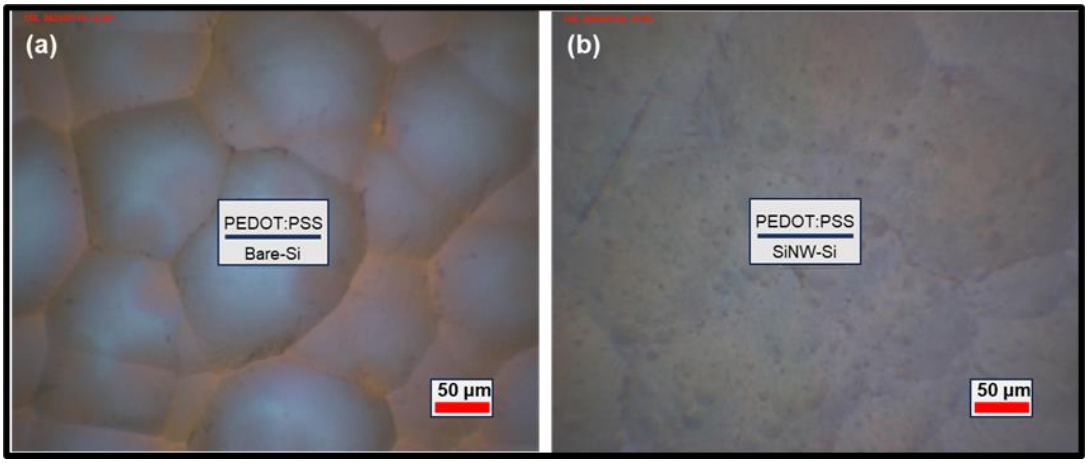

Figure S3. Optical Microscopic images of **(a)** PEDOT:PSS/Si **(b)** PEDOT:PSS/SiNW-Si THSC top surface view.

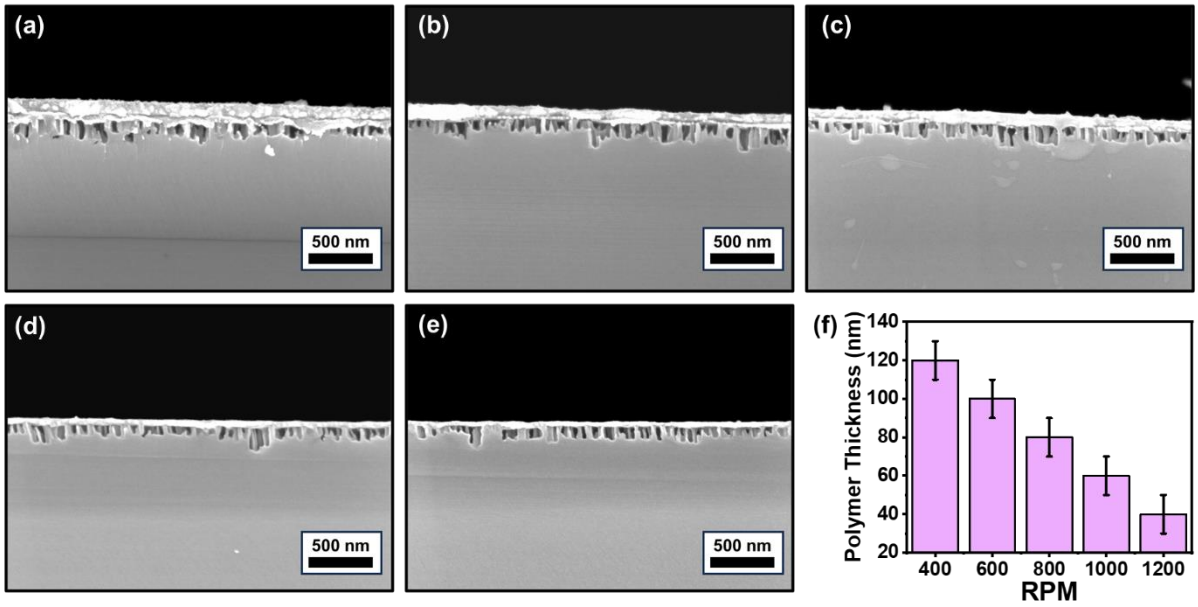

Figure S4. Cross-sectional FESEM images of **(a)** $THSC_{400}$, **(b)** $THSC_{600}$, **(c)** $THSC_{800}$, **(d)** $THSC_{1000}$, **(e)** $THSC_{1200}$; **(f)** Plot illustrating the thickness of polymer PEDOT:PSS layer for respective spin speed parameter (rpm).

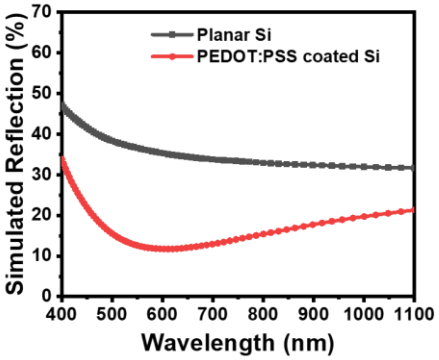

Figure S5. Simulated reflection of planar Si with and without PEDOT:PSS layer coating.

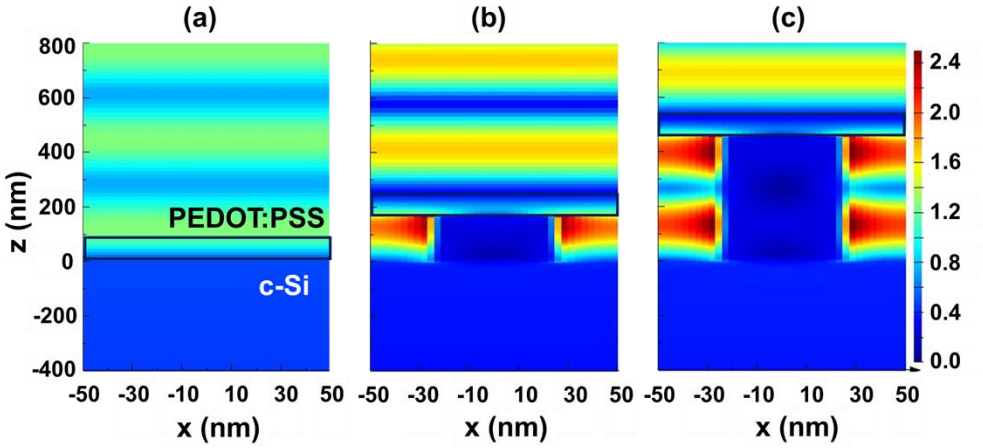

Figure S6. Normalized electric field distribution profiles of PEDOT:PSS coated **(a)** planar Si, and SiNW arrays of length **(b)** 170 nm and **(c)** 560 nm for incident light of λ = 650 nm using FDTD simulation.

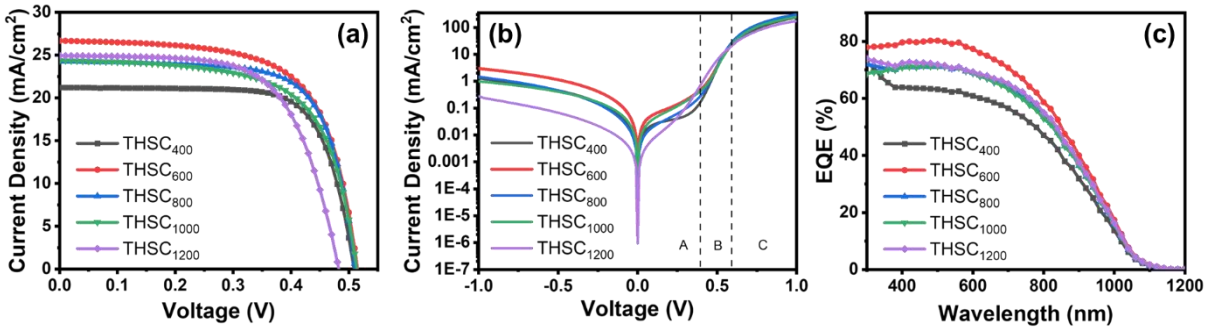

Figure S7. J-V characteristics **(a)** Illuminated, **(b)** Dark; and **(c)** EQE of the SiNW-based THSCs with spin speed variation.

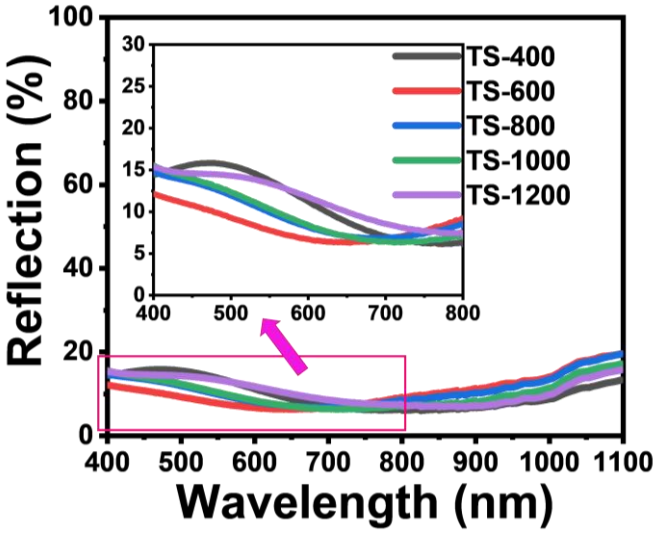

Figure S8. Reflection plots for the PEDOT:PSS coated thin Si wafers with varying PEDOT:PSS thickness (rpm variation). 'TS-x', where x represents their respective rpm. The inset in the figure shows that the TS-600 has minimum reflection.

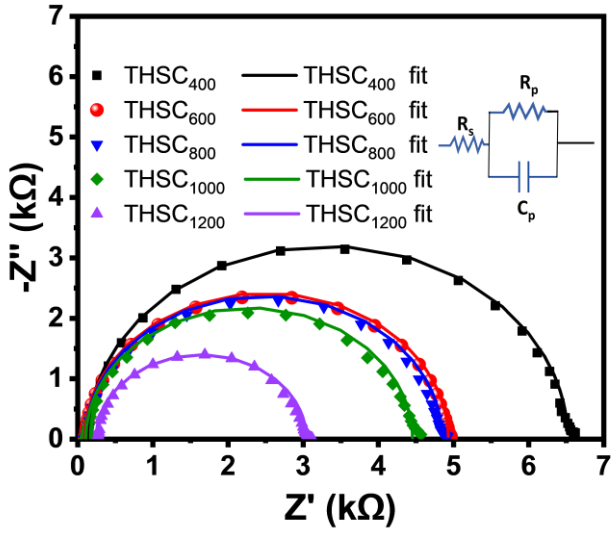

Figure S9. Nyquist plots at 0 bias voltage for SiNW-based THSCs with spin speed variation and the equivalent circuit model used for fitting, shown in the inset.

Table S1. Summary of SiNW-based research works on thin-flexible HHSCs.

Reference	Wafer Thickness	Device Structure	Efficiency	Comment
[35]	8.6 μm	• 2.1 μm long SiNW • Ag/PEDOT:PSS/SiNW/c-Si/Ag-NS/Al_2O_3/Ni-Ag	6.62%	Longer SiNW, Complex Structure with Al_2O_3 and Ag NS
[36]	20 μm	• 180 nm nanopores structure followed by TMAH treatment	8.7%	Active area is just 0.25 cm^2
[37]	60 μm	• Si nanoholes on microtextured surface • Heavily doped N^+ BSF layer • ITO/PEDOT:PSS/SiNH-μT Si/N^+/Ti/Ag	12%	Lacks flexibility due to ITO substrate
[38]	20 μm	• Si nanopores	8.47%	Procedure became excessively prolonged and involved a high thermal budget process, potentially deviating from the fundamental objective of the low-temperature, cost-effective HHSCs concept
		• Highly doped N^+ BSF layer	12.1%	
		• MACE reconstruction • Ag/PEDOT:PSS/SiNP/Si/N^+/Ag	13.6%	
[39]	65 μm	• 900 nm SiNW on a textured polyimide substrate (to avoid transmission loss in thin Si) • Ag/PEDOT:PSS/SiNW/Si/Ag/PI substrate	2.58%	Very Low PCE reported
[40]	45 μm	• SiNW fabricated via nanosphere lithography followed by MACE • Ag/PEDOT:PSS/SiNW/Si/Al	7.79%	Active area is just 0.5 cm^2
	23 μm		7.29%	
[41]	14 μm	• SiNW with TMAH treatment	9.1%	Highest for SiNW-based thin HHSCs. The device area is just 0.8 cm^2
		• SiNW without TMAH treatment	6.6%	

Table S2. Device performance parameters[#] for THSCs fabricated on thin SiNW textured wafers with spin speed variation for polymer coating.

Device Set	*Illuminated J-V*				*Dark J-V*			*EQE*
	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	PCE (%)	J_0 (A/cm^2)	n	ϕ_{bi} (eV)	$J_{sc,EQE}$ (mA/cm^2)
THSC$_{400}$	0.507 ± 0.003	20.61 ± 0.81	69.22 ± 2.90	7.26 ± 0.61	5.15×10^{-9}	1.47	0.92	20.01
	0.509	**21.21**	**72.66**	**7.85**				
THSC$_{600}$	0.514 ± 0.004	24.93 ± 1.65	67.05 ± 2.50	8.40 ± 0.65	1.92×10^{-8}	1.59	0.89	25.14
	0.515	**26.68**	**65.49**	**9.00**				
THSC$_{800}$	0.510 ± 0.001	23.32 ± 1.68	68.15 ± 3.72	8.11 ± 0.59	9.46×10^{-9}	1.51	0.90	22.63
	0.511	**24.28**	**70.63**	**8.77**				
THSC$_{1000}$	0.510 ± 0.002	22.34 ± 1.89	67.13 ± 3.77	7.64 ± 0.47	3.79×10^{-8}	1.71	0.87	22.59
	0.513	**24.38**	**65.20**	**8.16**				
THSC$_{1200}$	0.482 ± 0.004	23.29 ± 1.54	63.91 ± 3.25	7.17 ± 0.46	1.64×10^{-7}	1.82	0.83	23.00
	0.483	**24.94**	**64.51**	**7.77**				

The data in bold correspond to each set's 'champion cell' parameters. The statistics present the mean with S.D. of four cells of each set processed under identical conditions on the same Si wafer.

Table S3. Device performance parameters of the $THSC_0$, $THSC_{90}$ and $THSC_{300}$ solar cells (new set) and change in parameters after 10 bending cycles.

Solar cell and performance parameters		Before Bending	After Bending	% Change* (±)
$THSC_0$	V_{oc} (V)	0.502	0.501	0.2%
	J_{sc} (mA/cm^2)	21.01	20.92	0.4%
	FF (%)	72.03	71.45	0.8%
	PCE (%)	7.62	7.56	0.8%
$THSC_{90}$	V_{oc} (V)	0.518	0.516	0.4%
	J_{sc} (mA/cm^2)	24.05	23.98	0.3%
	FF (%)	69.87	69.35	0.7%
	PCE (%)	8.72	8.69	0.3%
$THSC_{300}$	V_{oc} (V)	0.481	0.478	0.6%
	J_{sc} (mA/cm^2)	22.22	21.99	1.0%
	FF (%)	68.00	67.28	1.0%
	PCE (%)	7.25	7.18	0.9%

$$* \% \text{ change} = \frac{|After\ bending - Before\ bending|}{Before\ bending} \times 100\%$$