Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

Supporting information:

Synthesis of Air-Stable 1T-CrS_2 Thin Films and Their Application in High-Performance Floating-Gate Memory

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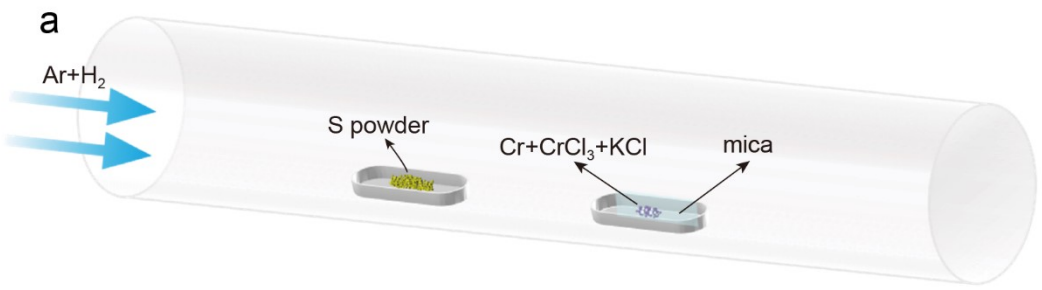


Figure S1. (a) Schematic diagram of the synthesis of CrS_2 thin layer by chemical vapor deposition (CVD) .

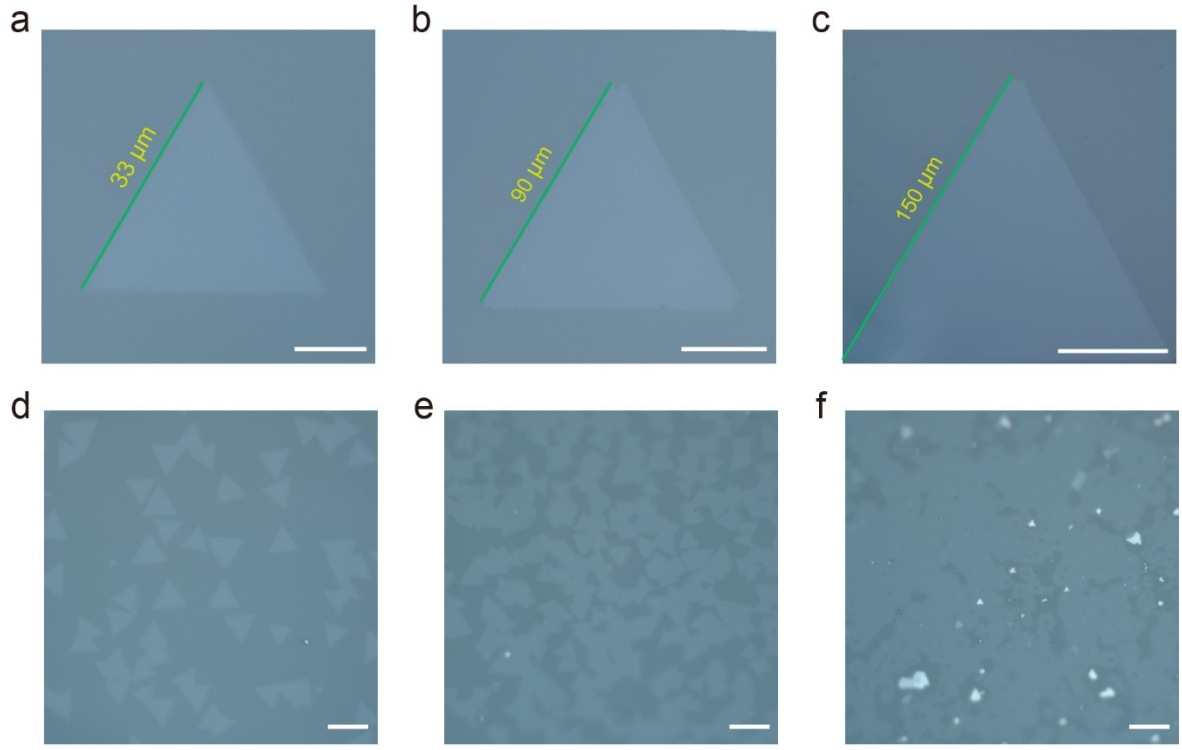
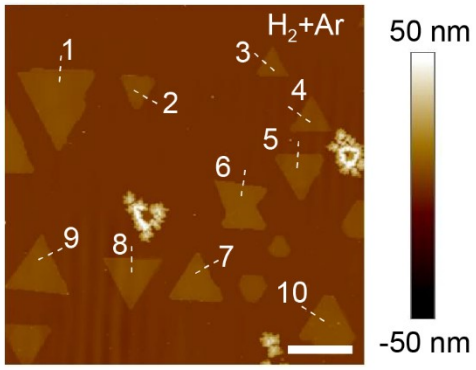


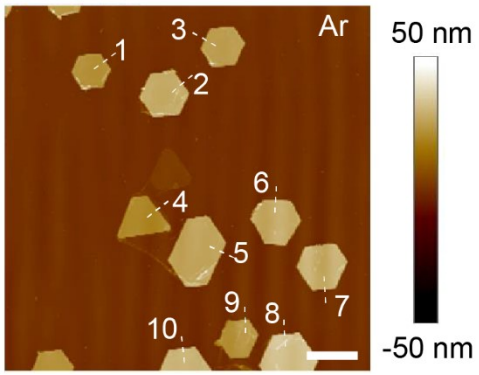
Figure S2. (a, b, c) OM images displaying the growth-time dependency of CrS_2 flakes synthesized at a consistent temperature of 720°C on mica substrates. The domain sizes of single CrS_2 crystals increase with growth times, reaching dimensions of approximately 33 μm in 5 minutes (a), 90 μm in 15 minutes (b), and 150 μm in 20 minutes (c). The scale bars are 10 μm (a), 30 μm (b), and 50 μm (c), respectively. (d, e, f) OM images illustrating the dependence of growth on temperature for CrS_2 flakes on mica, synthesized under identical conditions for a duration of 10 minutes. The coverage percentages are approximately 50% at 700°C (d), 70% at 720°C (e), and 90% at 740°C (f). The scale bars are 25 μm for each.

a



Position	Thickness	Position	Thickness
1	5.262 nm	6	6.993 nm
2	5.718 nm	7	6.714 nm
3	5.004 nm	8	5.822 nm
4	5.291 nm	9	5.910 nm
5	5.542 nm	10	6.522 nm
Range	5.004-6.993 nm	Average	5.878 nm

b



Position	Thickness	Position	Thickness
1	22.312 nm	6	28.407 nm
2	28.428 nm	7	28.172 nm
3	25.056 nm	8	33.924 nm
4	20.613 nm	9	25.347 nm
5	26.287 nm	10	29.950 nm
Range	20.613-33.924 nm	Average	26.845 nm

Figure S3. (a) Representative AFM images of CrS_2 nanosheets on mica substrates (grown with H_2 and Ar) through measuring their thicknesses by AFM height profiles. The scale bar is 10 μm (b) AFM schematic diagram and planing height statistical data of CrS_2 nanosheets grown on mica substrate under Ar atmosphere only.

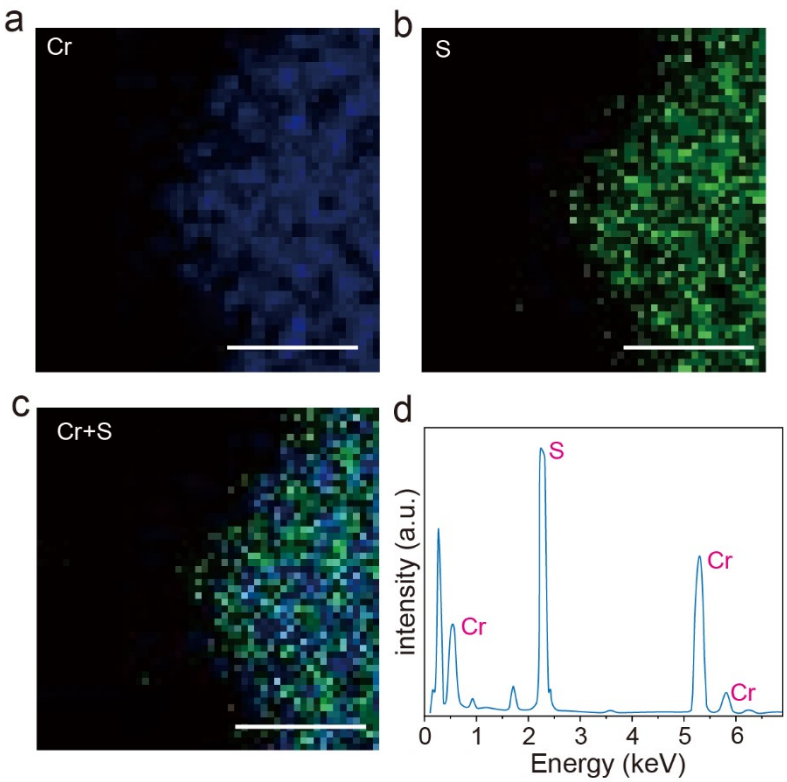


Figure S4. (a, b, c) EDS map of chromium and sulfur elements enlarged ten times. The scale bar is 50 nm). (d) EDS elemental analysis of a CrS_2 flake on a TEM grid showing an atomic ratio of Cr and S around 1:1.93.

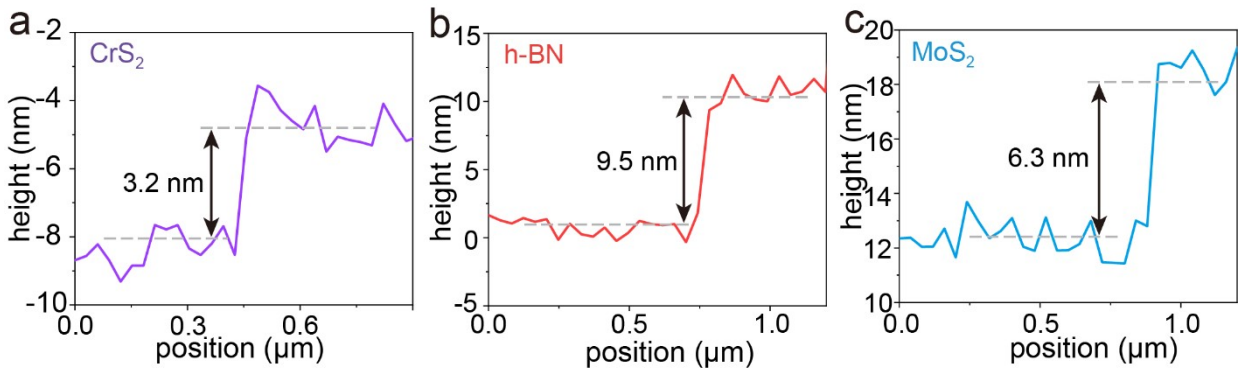


Figure S5. (a) The cross-sectional line profiles of thin CrS_2 sheets. (b, c) The thickness of the channel layer (MoS_2) and tunneling layer (*h*-BN) in the memory devices.

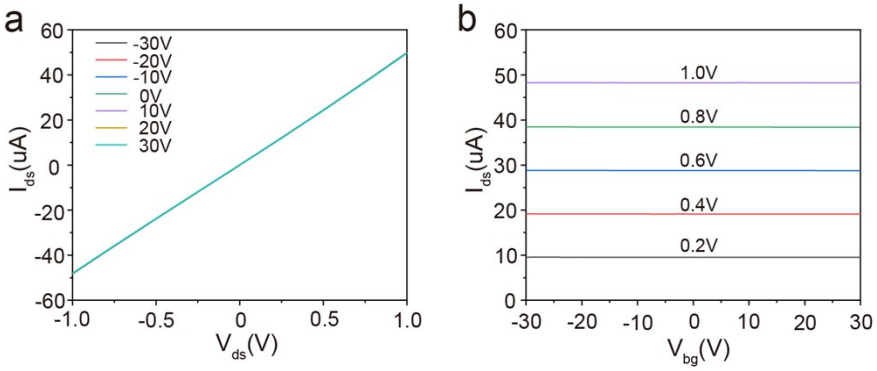


Figure S6. (a, b) Typical output and transfer curves of the CrS_2-based FET. There is no significant change in electrical properties compared with a month ago.

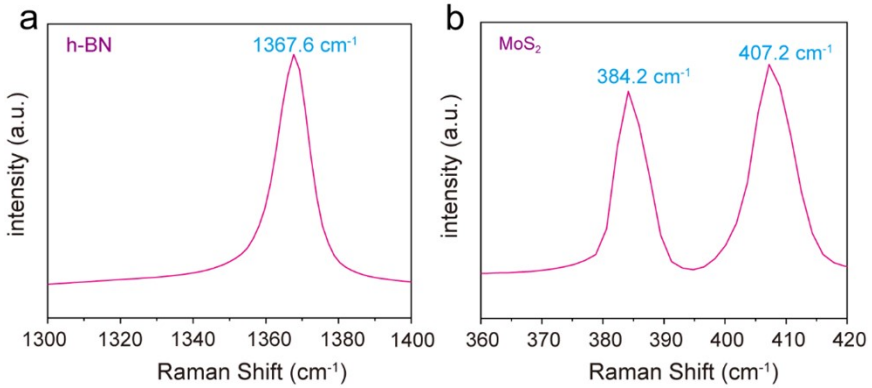


Figure S7. (a, b) The thickness of the channel layer (*h*-BN) and tunneling layer (MoS_2) Raman Spectra in FG memory.

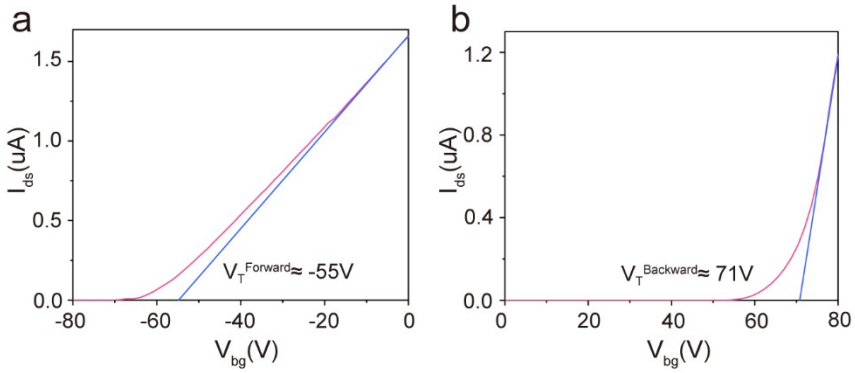


Figure S8. Extraction of the memory window under the control gate voltage range of 80 V. (a) The x-intercept of the linear fit indicates $V_T^{Forward} \approx -55$ V. (b) The x-intercept of the linear fit indicates $V_T^{Backward} \approx 71$ V.

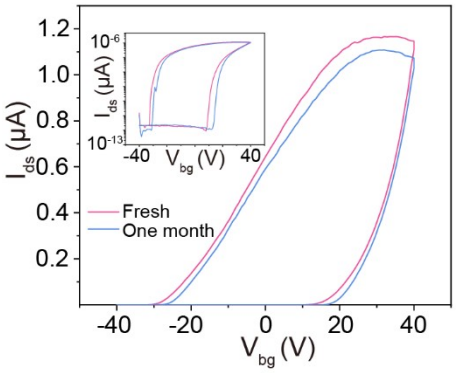
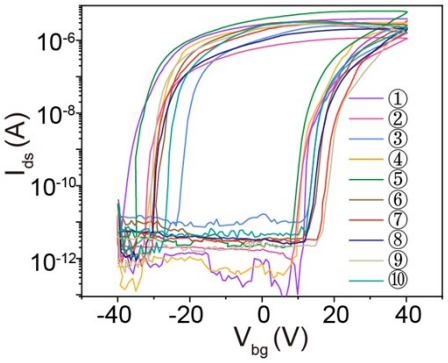


Figure S9. Device output curve after being placed in indoor environment for one month.



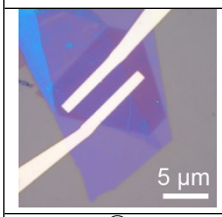
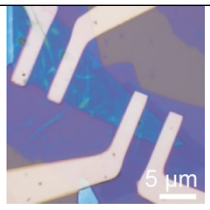
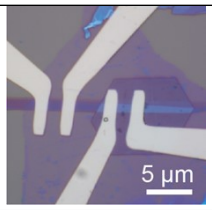
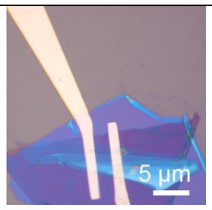
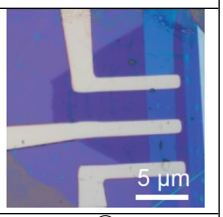
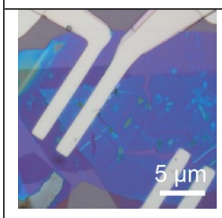
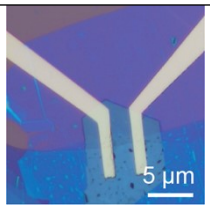
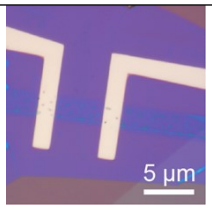
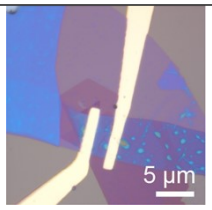
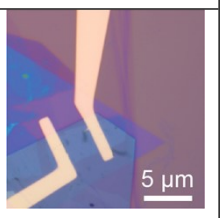
The window ratio of the memory device and the thickness of h-BN and MoS_2				
□ Window ratio ≈ 68% h-BN：10.5 nm MoS_2：2.3 nm	② Window ratio ≈ 56% h-BN：9.5 nm MoS_2：6.3 nm	③ Window ratio ≈ 48% h-BN：9.4 nm MoS_2：7.3 nm	④ Window ratio ≈ 53% h-BN：10.2 nm MoS_2：8.2 nm	⑤ Window ratio ≈ 57% h-BN：11.0 nm MoS_2：5.8 nm
				
⑥ Window ratio ≈ 56% h-BN：9.8 nm MoS_2：7.2 nm	⑦ Window ratio ≈ 63% h-BN：11.5 nm MoS_2：7.1 nm	⑧ Window ratio ≈ 54% h-BN：10.0 nm MoS_2：3.1 nm	⑨ Window ratio ≈ 64% h-BN：9.1 nm MoS_2：5.6 nm	⑩ Window ratio ≈52% h-BN：9.3 nm MoS_2：4.6 nm
				

Figure S10. Transfer curve (I_{ds}-V_{bg}) of ten different floating gate memories at a fixed source-drain voltage V_{ds} of 0.1 V. Corresponding OM images of ten FG device, the thickness range of h-BN is approx 9.1 nm - 11.0 nm and the thickness range of MoS_2 is approx 2.3 nm – 7.3 nm. The window ratio fluctuates within a smaller range, around 48% to 68%.

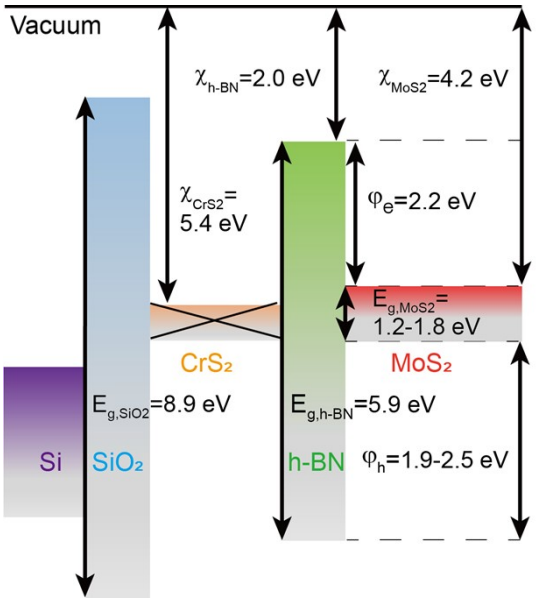


Figure S11. Schematic of the energy band diagram of memory. Calculate from DFT, the electron affinities of CrS_2 are 5.4 eV. The electron affinities of MoS_2 and h-BN are 4.2 eV and 2.0 eV respectively. The band gaps of multilayer MoS_2 and h-BN are 1.2 eV-1.8 eV and 5.9 eV respectively,[1,2] so the potential barriers at the MoS_2/h-BN interface are φ_e=2.2 eV and φ_h =1.9 eV-2.5 eV. The potential barriers at the CrS_2/h-BN interface are φ_e=3.4 eV and φ_h =2.5 eV, respectively. Enough to block carriers stored in the floating gate.[2,3]

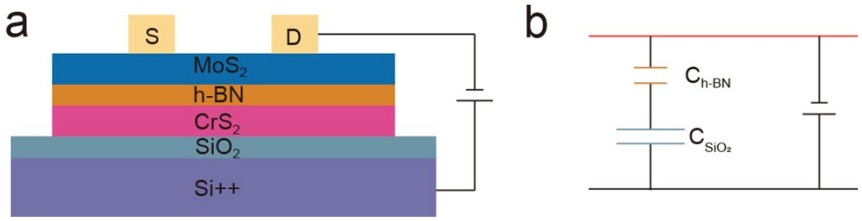


Figure S12. (a) Schematic illustration of the FG device. (b) The equivalent circuit diagram of the FG memory device.

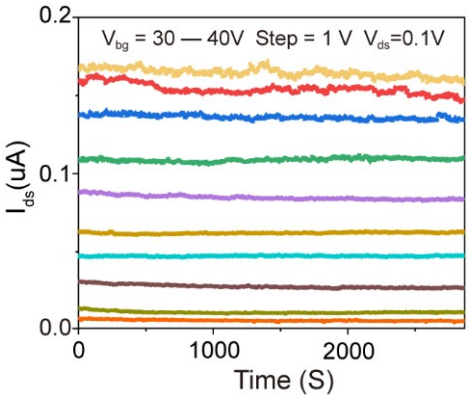


Figure S13. I–t curves of the memory device at ten distinct conductive levels for ≈3000 s. back gate pulses increased from 30 to 40 V with gate pulse of 10 ms.

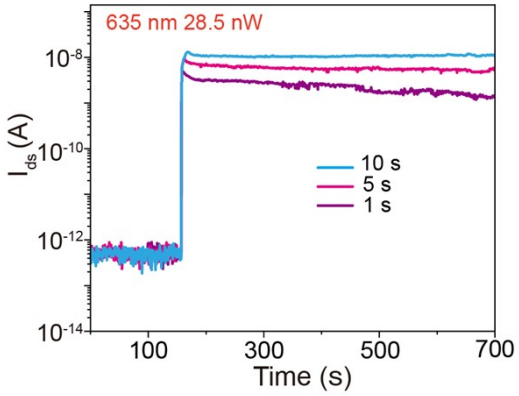


Figure S14. Photoresponse memory properties as a function of exposure time. Time dependent I_{ds} under the 635 nm illumination with a light power of 28.25 nW at V_{ds} = 0.1 V.

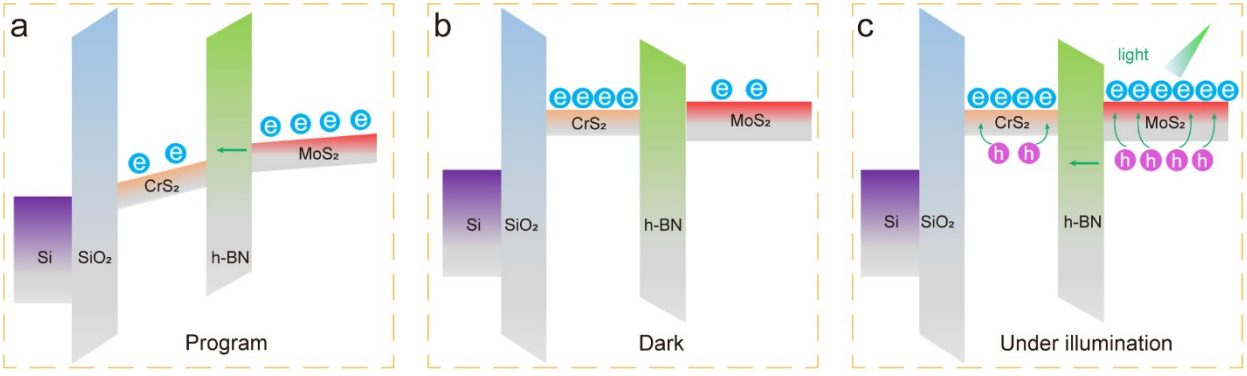


Figure S15. Energy band diagram of the FG memory device in different optoelectronic memory

Table S1. Comparison of the performance of our floating-gate memory devices based on metal materials with other devices partially based on 2D metal floating-gate materials.

Device structure	Window ratio(%)	On/off	Reference
$MoS_2/HfO_2/Al/HfO_2$	~25%	$\sim10^6$	4
$MoS_2/HfO_2/Ag/HfO_2$	~30%	$\sim10^6$	4
$MoS_2/HfO_2/Co/HfO_2$	~27%	$\sim10^7$	4
$MoS_2/HfO_2/Au/HfO_2$	~50%	$\sim10^7$	4
MoS_2/h-BN/Au/SiO_2	~42%	$\sim10^7$	5
SnS_2/h-BN/Au/SiO_2	~58%	$\sim10^7$	5
Au/h-BN/MoS_2/h-BN/SiO_2	~50%	$\sim10^6$	6
MoS_2/h-BN/CrS_2/SiO_2	~79%	$\sim10^7$	This Work

Supplementary Notes

Equivalent circuit diagram of the memory is shown in the FigureS12. The electric field intensity in h-BN (E_{h-BN}) and SiO_2 (E_{SiO_2}) dielectric can be given by the following formula based on the principle of superstition of electric potential and charge conversation law. [7]

$$E_{h-BN}d_{h-BN} + E_{SiO_2}d_{SiO_2} = V_{cg} \quad (1)$$

$$C_{h-BN} = \varepsilon_{h-BN}d_{h-BN}/S_1 \quad (2)$$

$$C_{SiO_2} = \varepsilon_{SiO_2}d_{SiO_2}/S_2 \quad (3)$$

where d_{h-BN}, d_{SiO_2}, V_{cg}, ε_{h-BN}, ε_{SiO_2}, S_1,and S_2 are the thicknesses of h-BN tunnel dielectric and SiO_2 oxide dielectric, control gate voltage, relative dielectric constants of h-BN and SiO_2, contact areas of MoS_2/ CrS_2 and CrS_2/control gate, and the amount of electrons tunneling through h-BN dielectric per unit area, respectively. According to the above formula, the V_{cg} increases with the increase of SiO_2 thickness.

References

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